Burr-Brown Products from Texas Instruments

ADS8322

16-Bit, 500kHz, MicroPower Sampling
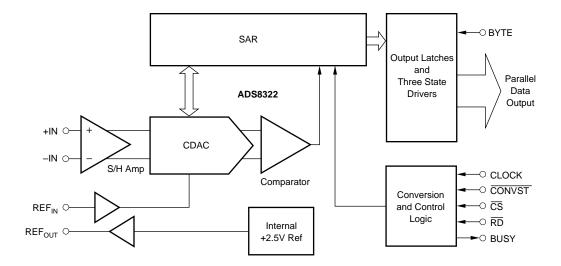# ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HIGH-SPEED PARALLEL INTERFACE**
- **500kHz SAMPLING RATE**
- **LOW POWER: 85mW at 500kHz**
- **INTERNAL 2.5V REFERENCE**
- **UNIPOLAR INPUT RANGE**
- **TQFP-32 PACKAGE**

APPLICATIONS

- **CT SCANNERS**
- **HIGH SPEED DATA ACQUISITION**
- **TEST AND INSTRUMENTATION**
- **MEDICAL EQUIPMENT**

DESCRIPTION

The ADS8322 is a 16-bit, 500kHz Analog-to-Digital (A/D) converter with an internal 2.5V reference. The device includes a 16-bit capacitor-based Successive Approximation Register (SAR) A/D converter with inherent sample-and-hold. The ADS8322 offers a full 16-bit interface, or an 8-bit option where data is read using two read cycles and 8 pins.

The ADS8322 is available in a TQFP-32 package and is guaranteed over the industrial –40°C to +85°C temperature range.

TEXAS INSTRUMENTS

www.ti.com

ABSOLUTE MAXIMUM RATINGS[1]

+IN to GND .... V_A + 0.1V
−IN to GND .... +0.5V
V_A to GND .... −0.3V to +7V
Digital Input Voltage to GND .... −0.3V to (V_A + 0.3V)
V_{OUT} to GND .... −0.3V to (V_A + 0.3V)
Operating Temperature Range .... −40°C to +105°C
Storage Temperature Range .... −65°C to +150°C
Junction Temperature (T_J max) .... +150°C
TQFP Package:
　Power Dissipation .... (T_J max − T_A) / θ_{JA}
　θ_{JA} Thermal Impedance .... 240°C/W
Lead Temperature:
　Vapor Phase (soldering, 60s) .... +215°C
　Infrared (soldering, 15s) .... +220°C
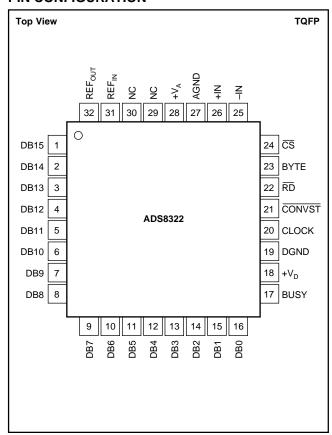
NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	DB15	Data Bit 15 (MSB)	20	CLOCK	An external CMOS compatible clock can be applied to the CLOCK input to synchronize the conversion process to an external source.
2	DB14	Data Bit 14			
3	DB13	Data Bit 13			
4	DB12	Data Bit 12	21	$\overline{\text{CONVST}}$	Convert Start
5	DB11	Data Bit 11	22	$\overline{\text{RD}}$	Synchronization pulse for the parallel output.
6	DB10	Data Bit 10	23	BYTE	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH). Data valid on pins 9-16.
3	DB9	Data Bit 9			
8	DB8	Data Bit 8	24	$\overline{\text{CS}}$	Chip Select
9	DB7	Data Bit 7	25	−IN	Inverting Input Channel
10	DB6	Data Bit 6	26	+IN	Noninverting Input Channel
11	DB5	Data Bit 5	27	AGND	Analog Ground
12	DB4	Data Bit 4	28	+V_A	Analog Power Supply, +5VDC.
13	DB3	Data Bit 3	29	NC	No Connect
14	DB2	Data Bit 2	30	NC	No Connect
15	DB1	Data Bit 1	31	REF$_{IN}$	Reference Input. When using the internal 2.5V reference tie this pin directly to REF$_{OUT}$.
16	DB0	Data Bit 0 (LSB)			
17	BUSY	High when a conversion is in progress.	32	REF$_{OUT}$	Reference Output. A 0.1µF capacitor should be connected to this pin when the internal reference is used.
18	+V_D	Digital Power Supply, +5VDC.			
19	DGND	Digital Ground			

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[1]	TRANSPORT MEDIA
ADS8322Y	±8	14	TQFP-32	351	−40°C to 85°C	ADS8322Y/250	Tape and Reel
"	"	"	"	"	"	ADS8322Y/2K	Tape and Reel
ADS8322YB	±6	15	TQFP-32	351	−40°C to 85°C	ADS8322YB/250	Tape and Reel
"	"	"	"	"	"	ADS8322YB/2K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "ADS8322Y/2K" will get a single 2000-piece Tape and Reel.

TEXAS INSTRUMENTS

ADS8322
SBAS215

ELECTRICAL CHARACTERISTICS: +V$_A$ = +5V

At −40°C to +85°C, +V$_A$ = +5V, V$_{REF}$ = +2.5V, f$_{SAMPLE}$ = 500kHz, and f$_{CLK}$ = 20 • f$_{SAMPLE}$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS8322Y			ADS8322YB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			16			∗		Bits
ANALOG INPUT								
Full-Scale Input Span[1]	+IN − (−IN)	0		+2V$_{REF}$	∗		∗	V
Absolute Input Range	+IN	−0.1		V$_A$ + 0.1	∗		∗	V
	−IN	−0.1		+0.5	∗		∗	V
Capacitance			25			∗		pF
Leakage Current			±1			∗		nA
SYSTEM PERFORMANCE								
No Missing Codes		14			15			Bits
Integral Linearity Error			±4	±8		±3	±6	LSBs[2]
Offset Error			±1.0	±2		±0.5	±1	mV
Gain Error[3]			±0.25	±0.50		±0.12	±0.25	% of FSR
Common-Mode Rejection Ratio	At DC		70			∗		dB
Noise			60			∗		µVrms
Power Supply Rejection Ratio	At FFFF$_H$ Output Code		±3			∗		LSBs
SAMPLING DYNAMICS								
Conversion Time				1.6			∗	µs
Acquisition Time				0.4			∗	µs
Throughput Rate				500			∗	kHz
Aperture Delay			50			∗		ns
Aperture Jitter			30			∗		ps
Small-Signal Bandwidth			20			∗		MHz
Step Response			100			∗		ns
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[4]	V$_{IN}$ = 5Vp-p at 100kHz		−90			−93		dB
SINAD	V$_{IN}$ = 5Vp-p at 100kHz		81			83		dB
Spurious Free Dynamic Range	V$_{IN}$ = 5Vp-p at 100kHz		94			96		dB
REFERENCE OUTPUT								
Voltage	I$_{OUT}$ = 0	2.475	2.50	2.525	2.48	∗	2.52	V
Source Current	Static Load			10			∗	µA
Drift	I$_{OUT}$ = 0		20			∗		pp[/°C
Line Regulation	4.75V ≤ V$_{CC}$ ≤ 5.25V		0.6			∗		mV
REFERENCE INPUT								
Range		1.5		2.55	∗		∗	V
Resistance[5]	to Internal Reference Voltage		10			∗		kΩ
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			∗		
Logic Levels:								
V$_{IH}$	I$_{IH}$ ≤ +5µA	3.0		+V$_A$	∗		∗	V
V$_{IL}$	I$_{IL}$ ≤ +5µA	−0.3		0.8	∗		∗	V
V$_{OH}$	I$_{OH}$ = 2 TTL Loads	4.0			∗			V
V$_{OL}$	I$_{OL}$ = 2 TTL Loads			0.4			∗	V
Data Format		Straight Binary				∗		
POWER-SUPPLY REQUIREMENT								
Logic Family			CMOS			∗		
+V$_A$		4.75	5	5.25	∗	∗	∗	V
+V$_D$		4.75	5	5.25	∗	∗	∗	V
Supply Current	f$_{SAMPLE}$ = 500kHz		17	25		∗	∗	mA
Power Dissipation	f$_{SAMPLE}$ = 500kHz		85	125		∗	∗	mW
TEMPERATURE RANGE								
Specified Performance		−40		+85	∗		∗	°C

∗ Specifications same as ADS8322Y.

NOTES: (1) Ideal input span; does not include gain or offset error. (2) LSB means Least Significant Bit, with V$_{REF}$ equal to +2.5V; 1LSB = 76µV. (3) Measured relative to an ideal, full-scale input (+In − (−In)) of 4.9999V. Thus, gain error includes the error of the internal voltage reference. (4) Calculated on the first nine harmonics of the input frequency. (5) Can vary ±30%.

TIMING DIAGRAM

TIMING CHARACTERISTICS(1)(2)

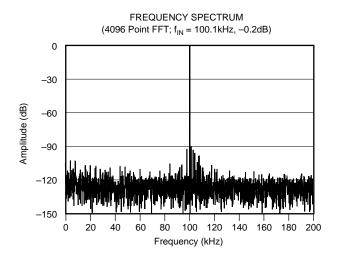All specifications typical at $-40°C$ to $+85°C$, $+V_D = +5V$.

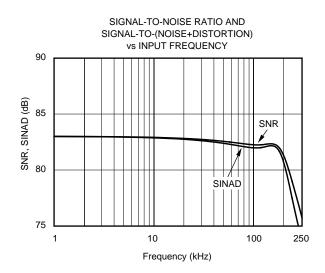| PARAMETER	SYMBOL	ADS8322A			ADS8322B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Conversion Time	t_{CONV}			1.6			*	µs
Acquisition Time	t_{ACQ}			0.4			*	µs
CLOCK Period	t_1	100			*			ns
CLOCK High Time	t_2	40			*			ns
CLOCK Low Time	t_3	40			*			ns
$\overline{CONVST}$ Low to Clock High	t_4	10			*			ns
CLOCK High to $\overline{CONVST}$ High	t_5	5			*			ns
$\overline{CONVST}$ Low Time	t_6	20			*			ns
$\overline{CONVST}$ Low to BUSY High	t_7			25			*	ns
$\overline{CS}$ Low to $\overline{CONVST}$ Low	t_8	0			*			ns
$\overline{CONVST}$ High	t_9	20			*			ns
CLOCK Low to $\overline{CONVST}$ Low	t_{10}	0			*			ns
CLOCK High to BUSY Low	t_{11}			25			*	ns
$\overline{CS}$ High	t_{12}	0			*			ns
$\overline{CS}$ Low to $\overline{RD}$ Low	t_{13}	0			*			ns
$\overline{RD}$ High to $\overline{CS}$ High	t_{14}	0			*			ns
$\overline{RD}$ Low Time	t_{15}	50			*			ns
$\overline{RD}$ Low to Data Valid	t_{16}	40			*			ns
Data Hold from $\overline{RD}$ High	t_{17}	5			*			ns
BYTE Change to $\overline{RD}$ Low(3)	t_{18}	0			*			ns
$\overline{RD}$ High Time	t_{19}	20			*			ns

NOTES: (1) All input signals are specified with $t_R = t_F = 5ns$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (2) See timing diagram, above. (3) BYTE is asynchronous; when BYTE is 0, bits 15 through 0 appear at DB15-DB0. When BUSY is 1, bits 15 through 8 appear on DB7-DB0. $\overline{RD}$ may remain low between changes in BYTE.
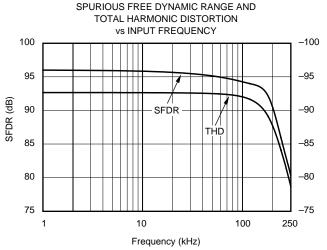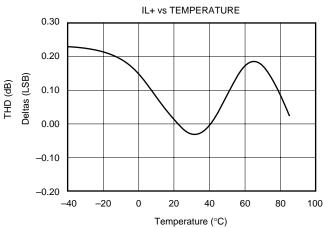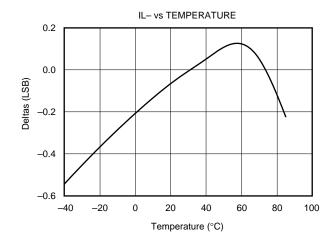
TEXAS INSTRUMENTS

ADS8322
SBAS215

TYPICAL CHARACTERISTICS

At –40°C to +85°C, +V$_A$ = +5V, V$_{REF}$ = +2.5V, f$_{SAMPLE}$ = 500kHz, and f$_{CLK}$ = 20 • f$_{SAMPLE}$, unless otherwise specified.
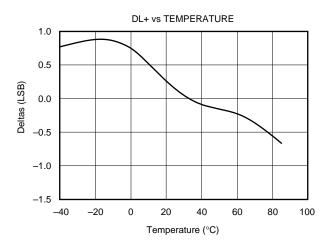
FREQUENCY SPECTRUM
(4096 Point FFT; f$_{IN}$ = 100.1kHz, –0.2dB)

SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT FREQUENCY

SPURIOUS FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY

IL+ vs TEMPERATURE

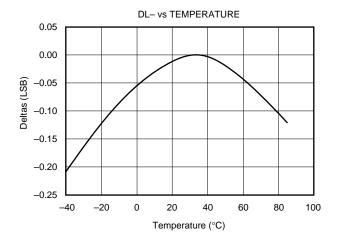IL– vs TEMPERATURE

DL+ vs TEMPERATURE

ADS8322

SBAS215

TEXAS INSTRUMENTS

5

TYPICAL CHARACTERISTICS (Cont.)

At −40°C to +85°C, +V_A = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 500kHz, and f_{CLK} = 20 • f_{SAMPLE}, unless otherwise specified.

DL− vs TEMPERATURE
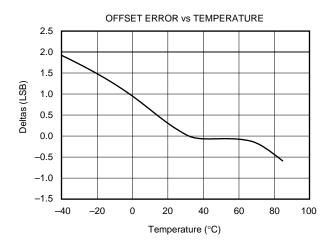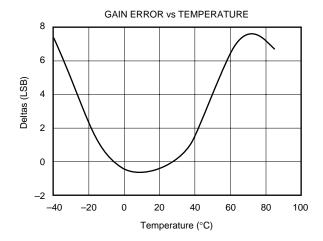
OFFSET ERROR vs TEMPERATURE

GAIN ERROR vs TEMPERATURE

V_{REF} vs TEMPERATURE

I_Q vs TEMPERATURE

TEXAS INSTRUMENTS

ADS8322

SBAS215

THEORY OF OPERATION

The ADS8322 is a high-speed Successive Approximation Register (SAR) A/D converter with an internal 2.5V bandgap reference. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The basic operating circuit for the ADS8322 is shown in Figure 1.

The ADS8322 requires an external clock to run the conversion process. The clock can be run continuously or it can be gated to conserve power between conversions. This clock can vary between 25kHz (1.25kHz throughput) and 10MHz (500kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 40ns and the clock period is at least 100ns. The minimum clock frequency is governed by the parasitic leakage of the Capacitive Digital-to-Analog (CDAC) capacitors internal to the ADS8322.

The analog input is provided to two input pins, +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

Under normal operation, the REF_{OUT} pin should be directly connected to the REF_{IN} pin to provide an internal +2.5V reference to the ADS8322. The ADS8322 can operate, however, with an external reference in the range of 1.5V to 2.6V for a corresponding full-scale range of 3.0V to 5.2V.

The internal reference of the ADS8322 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to the REF_{OUT} pin (the internal reference can typically source and sink 10μA of current). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the CDAC capacitors during conversion.

ANALOG INPUT

When the converter enters Hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is
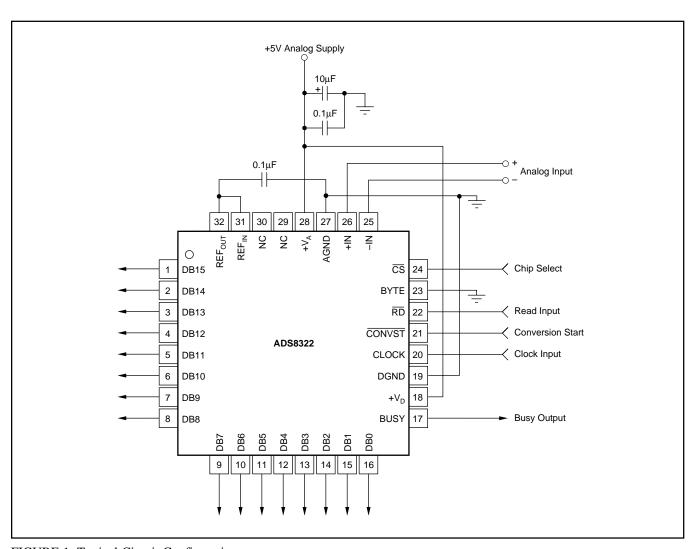

FIGURE 1. Typical Circuit Configuration.

limited between –0.1V and 0.5V, allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of –0.1V to $+V_A + 0.1V$.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8322 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 16-bit settling level within the acquisition time (400ns) of the device. When the converter goes into Hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –IN input should not drop below GND – 100mV or exceed GND + 0.5V. The +IN input should always remain within the range of GND – 100mV to $V_A + 100mV$. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low-bandwidth input signals with lowpass filters should be used.

DIGITAL INTERFACE

TIMING AND CONTROL

See the timing diagram in the Timing Characteristics section for detailed information on timing signals and their requirement.

The ADS8322 uses an external clock (CLOCK) which controls the conversion rate of the CDAC. With a 10MHz external clock, the A/D converter sampling rate is 500kHz, which corresponds to a 2μs maximum throughput time.

Conversions are initiated by bringing the $\overline{CONVST}$ pin LOW for a minimum of 20ns (after the 20ns minimum requirement has been met, the $\overline{CONVST}$ pin can be brought HIGH), while $\overline{CS}$ is LOW. The ADS8322 will switch from Sample-to-Hold mode on the falling edge of the $\overline{CONVST}$ command. Following the first rising edge of the external clock after a $\overline{CONVST}$ LOW, the ADS8322 will begin conversion (this first rising edge of the external clock represents the start of clock cycle one; the ADS8322 requires 16 rising clock edges to complete a conversion). The BUSY output will go HIGH immediately following $\overline{CONVST}$ going LOW. BUSY will stay HIGH through the conversion process and return LOW when the conversion has ended.

Both $\overline{RD}$ and $\overline{CS}$ can be HIGH during and before a conversion (although $\overline{CS}$ must be LOW when $\overline{CONVST}$ goes LOW to initiate a conversion). Both the $\overline{RD}$ and $\overline{CS}$ pins are brought LOW in order to enable the parallel output bus with the conversion.

READING DATA

The ADS8322 outputs full parallel data in Straight Binary format, as shown in Table I. The parallel output will be active when $\overline{CS}$ and $\overline{RD}$ are both LOW. The output data should not be read 125ns prior to the falling edge of $\overline{CONVST}$ and 10ns after the falling edge. Any other combination of $\overline{CS}$ and $\overline{RD}$ will tri-state the parallel output. Refer to Table I for ideal output codes.

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
Full-Scale Range	$2 \cdot V_{REF}$		
Least Significant Bit (LSB)	$2 \cdot V_{REF}/65535$	BINARY CODE	HEX CODE
+Full Scale	$2V_{REF} - 1$ LSB	1111 1111 1111 1111	FFFF
Midscale	V_{REF}	1000 0000 0000 0000	8000
Midscale – 1LSB	$V_{REF} - 1$ LSB	0111 1111 1111 1111	7FFF
Zero	0V	0000 0000 0000 0000	0000

TABLE I. Ideal Input Voltages and Output Codes.

BYTE

The output data will appear as a full 16-bit word on DB15-DB0 (MSB-LSB), if BYTE is LOW. The result may also be read on an 8-bit bus by using only DB7-DB0. In this case two reads are necessary. The first, as before, leaving BYTE LOW and reading the 8 least significant bits on DB7-DB0, then bringing BYTE HIGH. When BYTE is HIGH, the upper 8 bits (D15-D8) will appear on DB7-DB0.

NOISE

Figure 2 shows the transition noise of the ADS8322. A low-level DC input was applied to the analog-input pins and the converter was put through 8,192 conversions. The digital output of the A/D converter will vary in output code due to the internal noise of the ADS8322. This is true for all 16-bit SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped
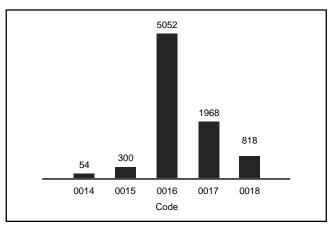

FIGURE 2. Histogram of 8,192 Conversions of a Low Level DC Input.

TEXAS INSTRUMENTS

with the peak of the bell curve representing the nominal code for the input value. The $\pm1\sigma$, $\pm2\sigma$, and $\pm3\sigma$ distributions will respectively represent the 68.3%, 95.5%, and 99.7% of all codes. The transition noise can be calculated by dividing the number of codes measured by six and this will yield the $\pm3\sigma$ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1,000 conversions. The ADS8322, with five output codes for the $\pm3\sigma$ distribution, will yield a $< \pm0.8$LSB transition noise at 5V operation. Remember that to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be $< 50\mu V$.

AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging 4 conversion results will reduce the transition noise by 1/2 to ±0.25 LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging: for every decimation by 2, the signal-to-noise ratio will improve 3dB.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8322 circuitry. This is particularly true if the CLOCK input is approaching the maximum throughput rate.

As the ADS8322 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, or nearby digital logic or high-power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. Their error can change if the external event changes in time with respect to the CLOCK input.

On average, the ADS8322 draws very little current from an external reference, as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation.

The AGND and DGND pins should be connected to a clean ground point. In all cases, this should be the "analog" ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

As with the GND connections, V_{DD} should be connected to a +5V power supply plane, or trace, that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8322 should be clean and well bypassed. A 0.1μF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1μF to 10μF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply. In some situations, additional bypassing may be required, such as a 100μF electrolytic capacitor, or even a "Pi" filter made up of inductors and capacitors—all designed to essentially lowpass filter the +5V supply, removing the high-frequency noise.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS8322Y/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8322Y/250G4	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8322Y/2K	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8322Y/2KG4	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8322YB/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8322YB/250G4	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8322YB/2K	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8322YB/2KG4	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated