ADS548xEVM

User's Guide

Literature Number: SLAU207
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1 Overview

This ADS548x evaluation module (EVM) user's guide gives an overview of the EVM and provides a general description of the features and functions to be considered while using this module.

1.1 Purpose

The ADS548xEVM provides a platform for evaluating the analog-to-digital converter (ADC) under various signal, reference, and supply conditions. Use this document in combination with the EVM schematic diagram supplied.

1.2 EVM Quick-Start Procedure

Power Supply

Power connections to the EVM are supplied by banana jack sockets. Separate banana jack sockets are provided for the ADC supplies and for the differential amplifier power supply.

Clock

The EVM provides an external SMA connector for input of the ADC clock. The single-ended input is converted into a differential signal at the input of the device. The clock also can be provided by onboard VCXO and CDCE72010.

Analog Inputs

The analog input to the ADC is provided by a external SMA connector. The input can be supplied to the ADC through two paths: one input path uses a THS4509 amplifier, whereas the other input is ac-coupled. In both cases, the user supplies a single-ended input or differential input(SMA connector which is not populated in the EVM). If the single-ended configuration is used, the signal is converted into the differential signal before the ADC.

1.3 Power Requirements

The EVM can be powered directly from 5 V for the ADC analog supply, or EVM jumper settings can be modified to use the onboard power solution from Texas Instruments (TI). The input power supply voltage range for the EVM can be 6 V to 36 V, only if the onboard TI power solution is used.

CAUTION

Voltage Limits: Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 ADS548xEVM Operational Procedure

The ADS548xEVM provides a flexible means of evaluating the ADS548x in various modes of operation. A quick-setup procedure follows.

1. Verify all jumper settings against the schematic jumper list in Table 1.

Table 1. Jumper List

Jumper	Function	Jumper Setting
Interface Circuit Operational Amplifier THS4509		
SJP1	AMP_OUT+	2-3
SJP2	AMP_OUT–	2-3
JP3	$\overline{PD}$	2-3
SJP4	AMPIN-	1-2
ADC Circuit		
JP4	PWRDWN_FAST	2-3
JP5	PWRDWN_SLOW	2-3
JP6	DITHER_ENABLE	2-3
Clock Interface circuit		
SJP6	CLOCKIN	1-2
SJP7	CLOCKIN, Y0, Y1P SELECT	1-2
SJP8	Y1N SELECT	1-2
J14	PWRDWN CDC	1-2
Power Supply		
JP12	3.3VA_IN	1-2
JP13	3.3VD_IN	1-2
JP14	5V_IN	1-2
JP15	TPS79501 INPUT SELECT	1-2
JP16	5V_AUX	2-3
JP17	TPS5420 INPUT SELECT	NO SHUNT

2. Connect the 5-V supply between J5 and J6 (GND), If you are using the TSW1200 for capture, it can also be used to source 5 V for the EVM. On the TSW1200, configure JP8 to short 1-2 and J22 to short 1-2 and jumper over 5 V from the banana jacks on the TSW1200 to J5 on the ADC EVM. Do not connect voltage source greater than 5.5 V.
3. Switch on power supplies.
4. Using a function generator with 50-Ω output impedance, generate a 0-V offset, 1.5-Vpp sine-wave clock into J12. The frequency of the clock must be within the specification for the device speed grade.
5. Use a frequency generator with a 50-Ω output impedance to provide a 0-V offset, –1-dBFS-amplitude sine-wave signal into J1. This provides a transformer-coupled differential input signal to the ADC.
6. Connect the TSW1200 or suitable logic analyzer to J4 to capture the resulting digital data. If you connect a TSW1200 to capture data, follow the additional alphabetically labeled steps. For more information, see Section 3.
   a. After installing the TSW1200 software and connecting the TSW1200 to the USB port, open the TSW1200 software.
   b. Depending on the ADC under evaluation, select from the “TI ADC Selection” pulldown.
   c. Change the “ADC Sample Rate” and “ADC Input Frequency” to match those of the signal generator.
   d. After selecting a Single Tone FFT test, press the “Capture Data” button.

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for this EVM is attached at the end of this document. See the schematic before changing any jumpers.

2.2 Circuit Function

The following sections describe the function of individual circuits. See the relevant data sheet for device operating characteristics.

2.2.1 Power

Power is supplied to the EVM through a TI power solution. Although various power options are available on this EVM, care should be taken while applying power on J5 as different options have different voltage ranges specified. Table 2 displays the general jumper setting information; Table 3 displays the various power option settings. Prior to making any jumper settings, see the Figure 12 schematic.

Table 2. EVM Power Supply Jumper Description

EVM Banana Jack	Description	Jumper setting
J5	Input	6-V to 36-V power supply; default - apply just 5 V
JP12	3.3VA_IN	1-2 → Connect 3.3-V AVdd to TPS79633 output; 2-3 → Ground
JP13	3.3VD_IN	1-2 → Connect 3.3-V DVdd to TPS79633 output; 2-3 → Ground
JP14	5V_IN	1-2 → Connect 5-V AVdd to 5V_Aux; 2-3 → Ground
JP15	TPS79501 INPUT SELECT	1-2 → Connects 5.3 V to ip of TPS79501; 2-3 → TPS79501 ip connected to J5
JP16	5V_AUX	1-2 → TPS79501 op as 5v_Aux rails; 2-3 → 5V_aux rail connected to J5
JP17	TS5420 INPUT SELECT	Shunt → J5 connected to TPS5420D

Table 3. EVM Power Supply Options

EVM Option	Evaluation Goal	Jumper Changes Required	Voltage on J5	Comments
1	Evaluate ADC performance using a cascaded switching power supply (TPS5420D) and LDO solution (TPS79501DCQ)	JP12 → 1-2; JP13 → 1-2; JP14 → 1-2; JP15 → 1-2; JP16 → 1-2; JP17 → 1-2;	6-36V	Maximum performance and efficiency.
2	Evaluate ADC performance using a LDO-based solution.	JP12 → 1-2; JP13 → 1-2; JP14 → 1-2; JP15 → 1-2; JP16 → 2-3, JP17 → No shunt;	5.1-5.5V	Max performance.
3	Evaluate ADC performance using an isolated ADC AVDD and DVDD for current consumption measurements	JP12 → connect 3.3V to pin 2 of Jumper; JP13 →connect 3.3V to pin 2 of Jumper; JP14 → connect 5.5V to pin 2 of Jumper and ground to J6; JP15 →No shunt ; JP16 →No shunt ; JP17 → No shunt;	Do not apply power on J5.	Isolated power supply for current consumption measurements

2.2.1.1 Power Supply Option 1

Option 1 supplies the power to the ADC using cascaded topology of the TPS5420D and the TPS79501DCQ. The TPS5420 is a step-down converter which works with the input voltage in the range 6 V to 36 V. The switching supply increases efficiency for higher input voltages but does create noise on the

voltage supplies. To reduce the noise, an ultralow-noise, high-PSSR LDO TPS79501DCQ is used to clean the power supply. The TPS5420D is designed for output of 5.3 V, which acts as input for TPS79501. The TPS79501 is designed to output a 5-V output, which is the AVDD for the ADC. This voltage rail is input to the LDO TPS79633, which outputs 3.3 V, used for DVDD for the ADC. A separate TPS79633 is designed to output 3.3 V for the CDCE72010 power supply rail. This solution adds two features to the EVM: one is to increase the range of the power supply on jumper J5 from 6 V to 36 V, allowing the user to choose any power supply source in the specified range without causing significant power dissipation. The other feature is that the output voltage rail has a much lower ripple, ensuring the better performance of the part even when the power source is fluctuating.

2.2.1.2 Power Supply Option 2

Option 2 supplies power to the ADC using the LDOs TPS79633DCQ and TPS79601DCQ. The LDOs limits the power supply on J5 to be in the range 5.1 V to 5.5 V only. This option again has the output voltage much cleaner as the LDOs chosen have high PSSR and low noise. Care must be taken while powering up the EVM using this option, as higher voltage or reverse polarity may damage the EVM.

2.2.1.3 Power Supply Option 3

Option 3 is used to evaluate ADC performance using an isolated AVDD and DVDD power supply for current consumption measurements. This option must be used with caution as reversing the power supply or connecting to the wrong connector can result in damage to the EVM.

2.2.2 Clock Input

The clock can be supplied to the ADC in two ways: one is from J12 directly, and the other by using the onboard VCXO and CDCE72010. Also, the clock supply to the ADC from CDCE72010 can be configured for a single-output clock from the CDCE72010 with a crystal filter, or one can use the differential LVPECL clock output. For better performance, the clock through a crystal output is recommended. Prior to making any jumper settings, see the Figure 13 schematic. Table 5 displays the various clock option settings.

Table 4. Clock Input Jumper Description

EVM Banana Jack	Description	Jumper setting
J11	ENABLE VCXO1 TC0-2111	1-2 → VCXO enabled 2-3 → VCXO Disabled
J12	Clock supply	
J14	CDCE72010 power down	1-2 → CDCE72010 is power Down; Open → CDCE72010 is On
J15	CDCE72010 Reset	1-2 → Reset , Open → Normal operation. (Default)
SJP6	Clock In or CDC Ref. Jumper	1-2 → J12 supplies clock directly to ADC; 2-3 → Reference clock for CDCE72010
SJP7	Clock input to +ve terminal of T4 for ADC clock	1-2 → Connects J12 to ADC; 3-4 → Connects Y0 output of CDCE72010 (This path has crystal filter) to ADC; 5-6 → Connects Y1P (Differential LVPECL clock output of CDCE72010) to ADC
SJP8	Clock input to -ve terminal of T4 for ADC clock	1-2 → Connects to ground (Default); 2-3 → Connects to Y1N (Differential clock output of CDCE72010) only to be used with Y1P.
SJP9	Mode select pin for CDCE72010	1-2 → High (default), see data sheet of CDCE72010; 2-3 → Ground
SJP10	PLLOCK LED	1-2 → Connects to D1 diode; 2-3 → Ground through 10-nF capacitor
SJP11	Aux_sel pin for CDCE72010	1-2 → High, see data sheet of CDCE72010; 2-3 → Ground (Default)

Table 5. EVM Clock Input Options

EVM Option	Evaluation Goal	Jumper Changes Required	Frequency input on J12	CDC configuration description	Comments
1	Evaluate ADC performance using a sinusoid clock.	J11 → 2-3; SJP6 → 1-2; SJP7 → 1-2; SJP8 → 1-2; J14 → 1-2; J15 → No shunt;	ADC's Sampling Frequency	NA	default
2	Evaluate ADC performance using a crystal filtered LVCMOS clock derived from CDCE72010	J11 → 1-2; SJP6 → 2-3; SJP7 → 3-4; SJP8 → 1-2; J14 → No shunt; J15 → No shunt;	10M for VCXO@491.52Mhz	Divide VCXO frequency by 4, output on Y0	Max performance.
3	Evaluate ADC performance using a differential LVPECL clock	J11 → 1-2; SJP6 → 2-3; SJP7 → 5-6; SJP8 → 2-3; J14 → No shunt; J15 → No shunt;	10M for VCXO@491.52Mhz	Divide VCXO frequency by 4,differential LVPECL Clock output on Y1P and Y1N	Not recommended for most applications

2.2.2.1 Clock Option 1

The Clock Option 1 provides a clock to ADC directly from an external source. For the direct supply of the clock to the ADC, a single-ended square or sinusoidal clock input must be applied to J12. The clock frequency must be within the maximum frequency specified for the ADC. The clock input is converted to a differential signal by a Mini-Circuits™ ADT4-1WT, which has an impedance ratio of 4, implying that voltage applied on J12 is stepped up by a factor of 2. ADC performance in this case depends on the clock source quality. This option is also the default configuration on the EVM, when it is shipped from the factory. The test result using this option is shown in Figure 3.

2.2.2.2 Clock Option 2

Option 2 uses the onboard VCXO and CDCE72010 to provide a clock to the ADC. The CDCE72010 is used in SPI mode which uses the internal EEPROM to configure the CDCE72010. The EEPROM is programmed in the factory for a divide-by-4 configuration. The EEPROM configuration is shown in Figure 1. The clock at J12 is the reference clock for CDCE72010. The VCXO frequency can be calculated as Fvcxo = Fout x 4 (Fout is the frequency output U0 and U1). The reference clock for CDCE72010 is calculated from Ref Clock = (Fvcxo x 125)/(48 x 128). (This is the clock-to-M divider.) When VCXO of frequency 491.52 MHz is used, the calculation results in a reference clock of 10 MHz; the clock output on

Y0 pin of CDCE72010 is 122.88 MHz. This clock is filtered using the crystal filter with center frequency of 122.88 MHz. By default, the VCXO and the crystal filter are not populated on the EVM, so that the user can populate the components depending on the end application and sampling rate. This configuration is recommended for applications requiring an onboard clock generation scheme. The test result using this option is shown in Figure 4.

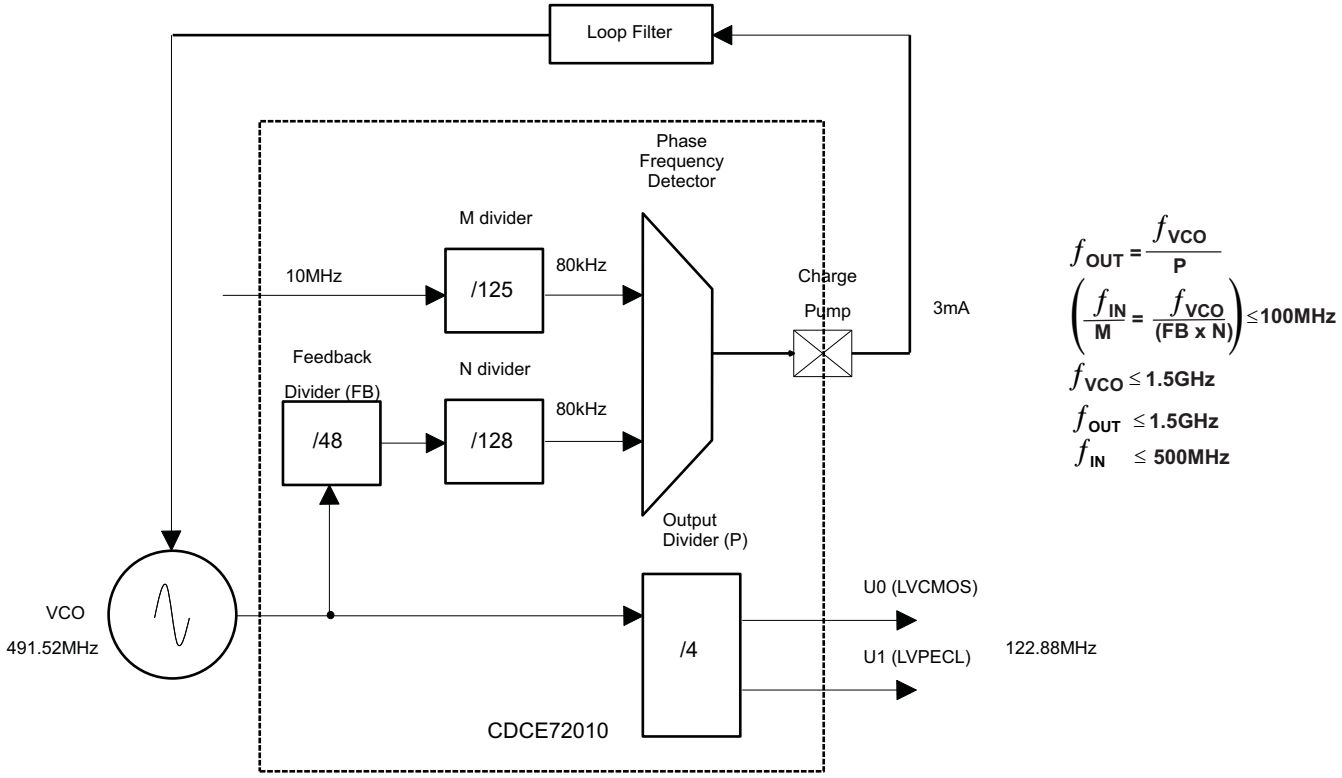

Figure 1. CDCE72010 EEPROM Configuration Block Diagram

2.2.2.3 Clock Option 3

Option 3 is used for a differential LVPECL clock. This configuration eliminates the need for a crystal filter. It uses the same EEPROM configuration as Option 2, but in this case, the ADC clock pins are connected to Y1N and Y1P. The jumper setting uses the clock output Y1P and Y1N from CDCE72010, to clock ADC. This configuration is not recommended for SNR critical applications. Notice that the clock frequency does not change. The frequency remains the same as in Clock Option 2. The test result using this option is shown in Figure 5.

2.2.3 Analog Inputs

The EVM can be configured to use either a transformer-coupled input or a TH4509 amplifier input, both from a single-ended source. The SMA connector J1 provides the inputs. The SMA connector J2 provides an option for a differential input, which is not populated. To set up for one of these options, the EVM must be configured as per the options listed in Table 7. See the Figure 9 schematic prior to making any jumper changes .

Table 6. Analog Input Jumper description

EVM Banana Jack	Description	Jumper setting
J1	Analog input Single ended.	

Table 6. Analog Input Jumper description (continued)

EVM Banana Jack	Description	Jumper setting
J2	Analog input, can be used with J1 for differential input	Not populated
J7	Power supply +	Apply 5V
J9	Power Supply -	Ground.
SJP1	AMP OUT+, +v terminal of T1	1-2 → Amp out+ is selected as the source of input to ADC; 2-3 → Use Analog input from J1 as signal source to ADC (Use with appropriate SJP4 setting)
SJP2	AMP OUT—, –v terminal of T1	1-2 → Amp out+ is selected as the source of input to ADC; 2-3 → Ground, (Default) Also can be used to connect J2 as a differential input along with SJP1 and SJP3 setting.
SJP3	INPUT –ve select	1-2 → J2 supplies the analog signal to ADC; 2-3 → +ve Input to amplifier. DEFAULT is No Shunt
SJP4	INPUT +ve select	1-2 → J1 supplies the analog signal to ADC. 2-3 → –ve Input to amplifier.
JP3	Power down for amplifier THS4509	1-2 → Pulls up the pin (Normal operation or amplifier is ON); 2-3 → Grounds the pin (Low-power mode or amplifier is off)

Table 7. EVM Analog Input Options

EVM Option	Evaluation Goal	Jumper Changes Required	Voltage on J7 and J9	Analog signal to ADC	Comments
1	Evaluate ADC performance using direct input to ADC.	SJP1 → 2-3; SJP2 → 2-3; SJP3 → No shunt; SJP4 → 1-2; JP3 → 2-3;	Do not connect	From J1	default
2	Evaluate ADC performance using input through THS4509	SJP1 → 1-2; SJP2 → 1-2; SJP3 → No shunt; SJP4 → 2-3; JP3 → 1-2;	J7 → 5V, J9 → GND	Signal from J1 is amplified by THS4509	Used if input signal requires amplification.

2.2.3.1 *Analog Input Option 1*

Option 1 supplies the transformer coupled input from J1 to ADC. This configuration is the default on the EVM. The test result using this option is shown in Figure 3.

2.2.3.2 *Analog Input Option 2*

Option 2 allows the use of an amplifier to provide input to the ADC. TI has a range of wideband operational amplifiers such as THS4508/09/11/13/20. On this EVM, THS4509 is used as an example to amplify the input from J1. The THS4509 is powered up by applying 5 V to J7 and GND to J9. You can also use a differential power supply to power up the amplifier; see the THS4509 data sheet (SLOS547). The output of the THS4509 is filtered through a band-pass filter before ADC input. The band-pass filter can be designed depending on the end application. By default, the band-pass filter components are not populated as the filter design depends on the end application. The TI schematic provides an example of a filter that is designed for the frequency band of 10 MHz to 58 MHz. When using the suggested filter, be sure to change the R2 and R6 resistors to 200 Ω. A key point when designing a filter is to design it for proper load termination. Care must be taken when supplying the input to the board, and ensure that the source impedance is 50 Ω. Results may vary due to mismatching of the various source and termination impedances. The evaluation result for the ADC5483 using THS4509 is shown in Figure 8.

2.2.4 Digital Outputs

The LVDS digital outputs can be accessed through the J4 output connector. A parallel 100-Ω termination resistor must be placed at the receiver to properly terminate each LVDS data pair. These resistors are required if the user wants to analyze the signals on an oscilloscope or a logic analyzer. The ADC performance also can be quickly evaluated using the TSW1200 boards as explained in next section.

3 Evaluation

3.1 TSW1200 Capture Board

The TSW1200 board can be used to analyze the performance of the EVM. The TSW1200EVM is a circuit board that assists designers in prototyping and evaluating the performance of high-speed ADCs that feature parallel or serialized LVDS outputs. The TSW1200 has the LVDS 100-Ω termination resistor on the input interface for ADC outputs.

To start the TSW1200 software, note the following points.

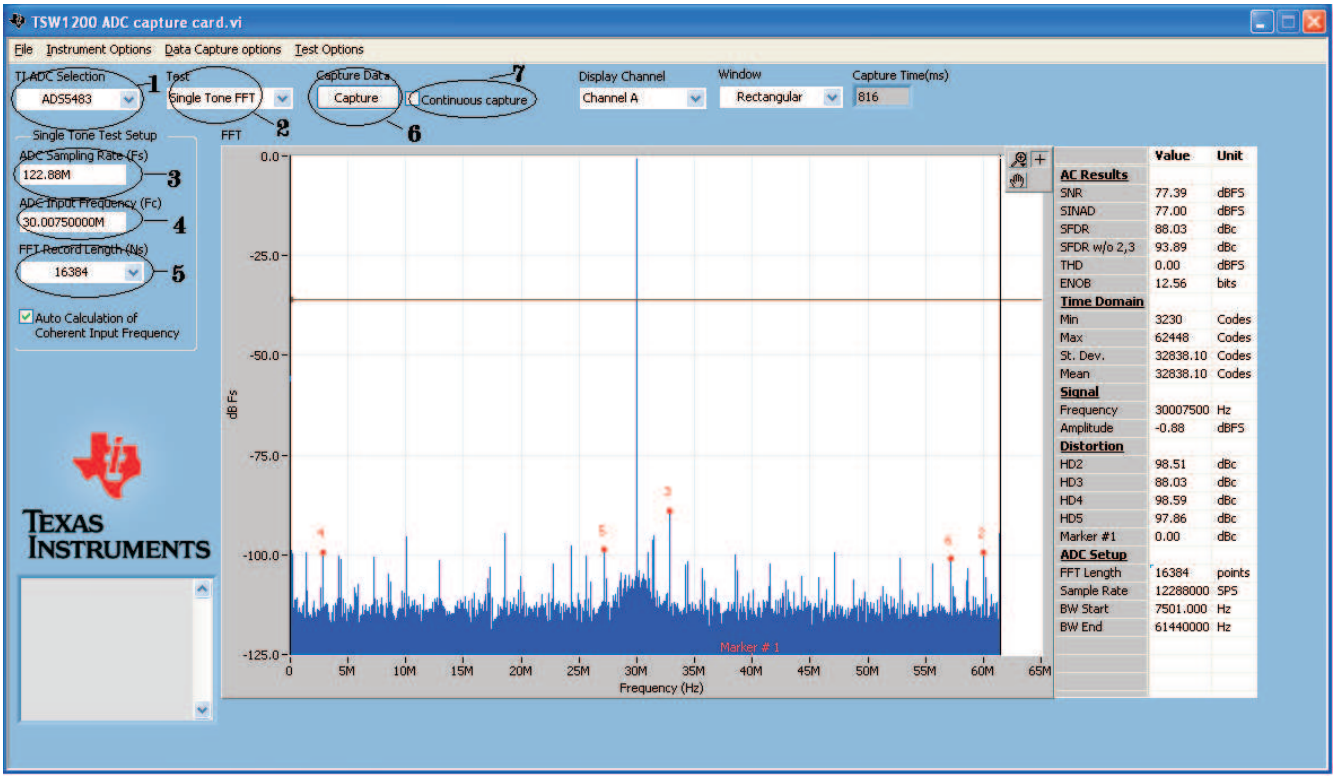

Figure 2. TSW1200 GUI Introduction

1. Select the ADC type to be used before capturing.
2. For test, select Single Tone FFT plot.
3. For the ADC Sampling Rate, type in the value.
4. Type in the ADC Input Frequency. Auto calculation of the input frequency depends on the FFT record length. As soon as the number is entered, the software calculates the coherent input frequency corresponding to that FFT length. This frequency signal must be supplied through the signal generator.
5. Select the FFT Record Length.
6. Select Capture to obtain the plot
7. The Continuous Capture option is used if the user wants to continuously capture the FFT.

Be sure to adjust the input level signal to attain the dBFs of approximately -1.

3.2 Quick-Test Results

The user can make the jumper setting as mentioned in Table 1. In this configuration, the EVM uses an external clock source from J12 and a direct input signal J1 to the ADC. This setup uses Power Option 2 (Table 3), Clock Option 1 (Table 5) and Analog Input Option 1 (Table 7), which is the default on the EVM. Figure 3 shows the ADC performance capture using TSW1200 with the input signal of a 100-MHz frequency and clock frequency of 122.88 MHz with ADS5483.

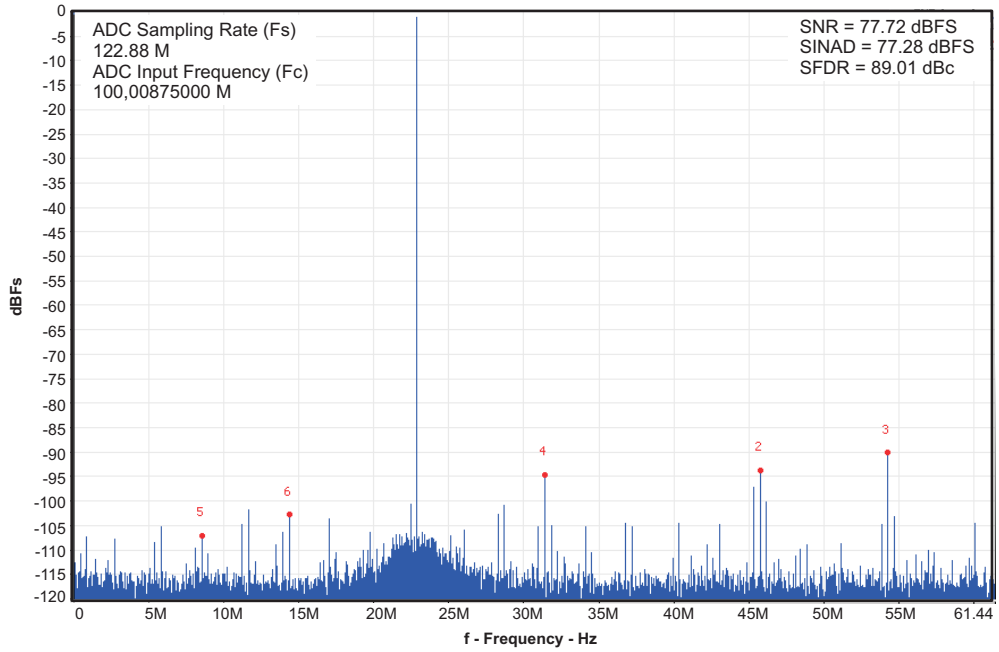

Figure 3. Quick-Setup Test Result.

3.3 Test Result With Onboard VCXO and Clock Through Crystal Filter

This test uses the VCXO of frequency 491.52 MHz. This setup uses the Power Option 2 (Table 3), Clock Option 2 (Table 5) and Analog Input Option 1 (Table 7). For this test, the CDCE72010 crystal filter path was chosen to provide the clock to the ADC. The CDCE72010 provides a single-ended clock through output Y0 (Table 5), which is passed through a crystal filter of center frequency 122.88 MHz. This was the example setup; the VCXO and the crystal filter are not populated on the EVM as the values depend on the end application sampling rate. The capture result for ADS5483 is as shown in Figure 4.

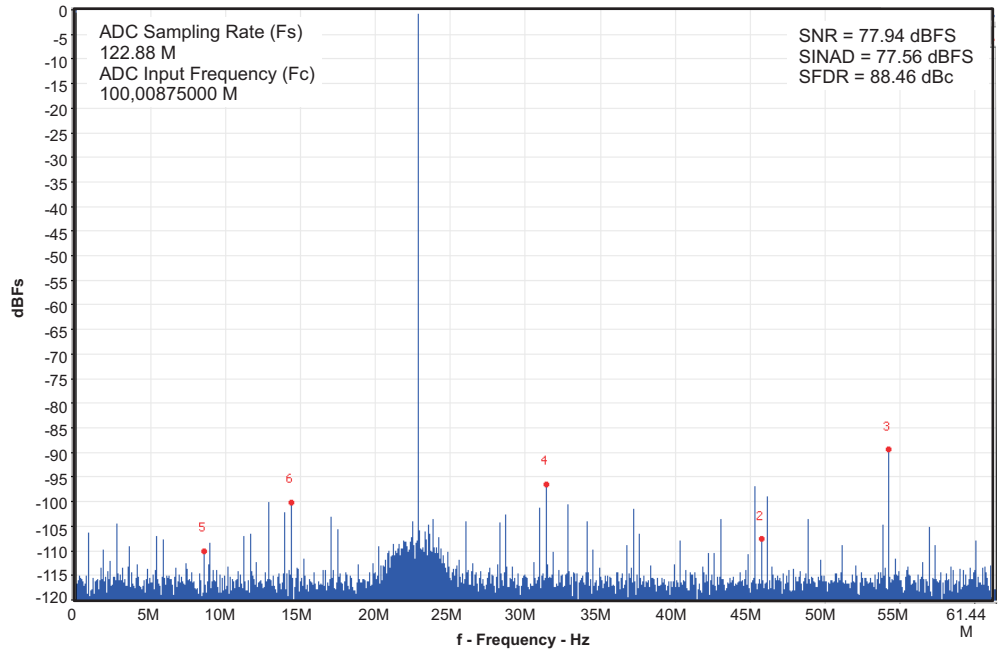

Figure 4. ADC Performance With Clock Through Onboard VCXO, CDCE72010, and Crystal Filter

3.4 Test Result With Onboard VCXO and Differential LVPECL Clock

For the same setup as explained in the previous section, when Clock Option 3 (Table 5) was used, the FFT was captured as shown in Figure 5. The test results with Clock Option 2 are better than with Clock Option 3. That is why Option 2 (clock with crystal filter) is recommended over the differential LVPECL output.

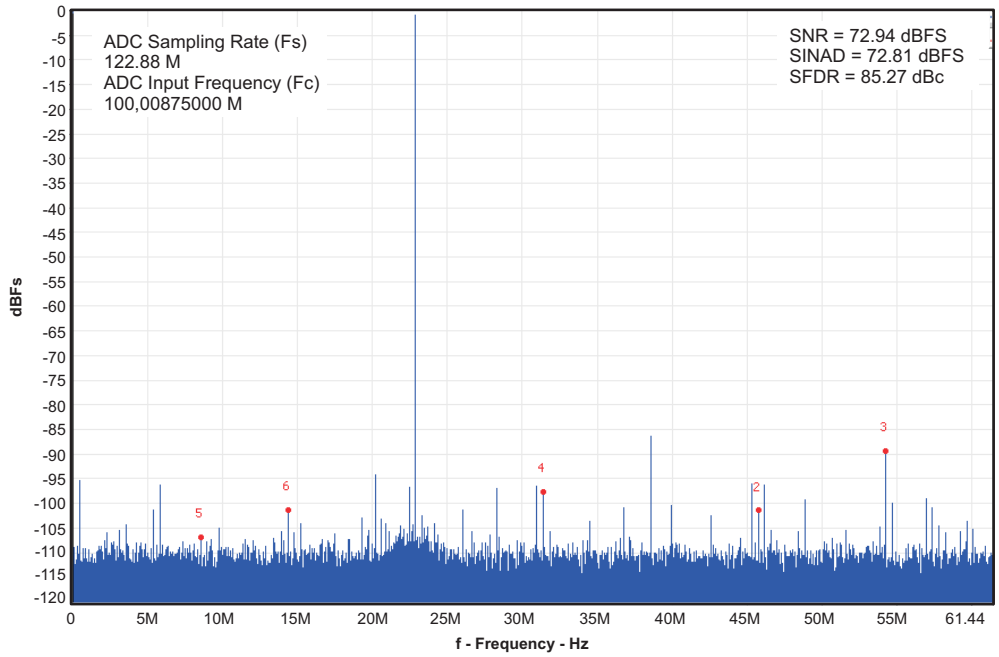

Figure 5. ADC Performance With Clock Through Onboard VCXO, CDCE72010 Configured for Differential LVPECL Output

3.5 Using THS4509

The THS4509 can be used to interface between the input signal on J1 to the input of ADC. In this setup, Power Option 2 (Table 3), Clock Option 1 (Table 5), and Analog Input Option 2 (Table 7) are used. The bandpass filter on the output of the THS4509 can be designed for the range of input frequencies. In this case, it is designed for 10 MHz to 58 MHz; the TI schematic contains the suggested values for the same bandwidth.

The bandpass-filter responses with the THS4509 were simulated using TINA-TI™. Figure 6 shows the simulated filter response.

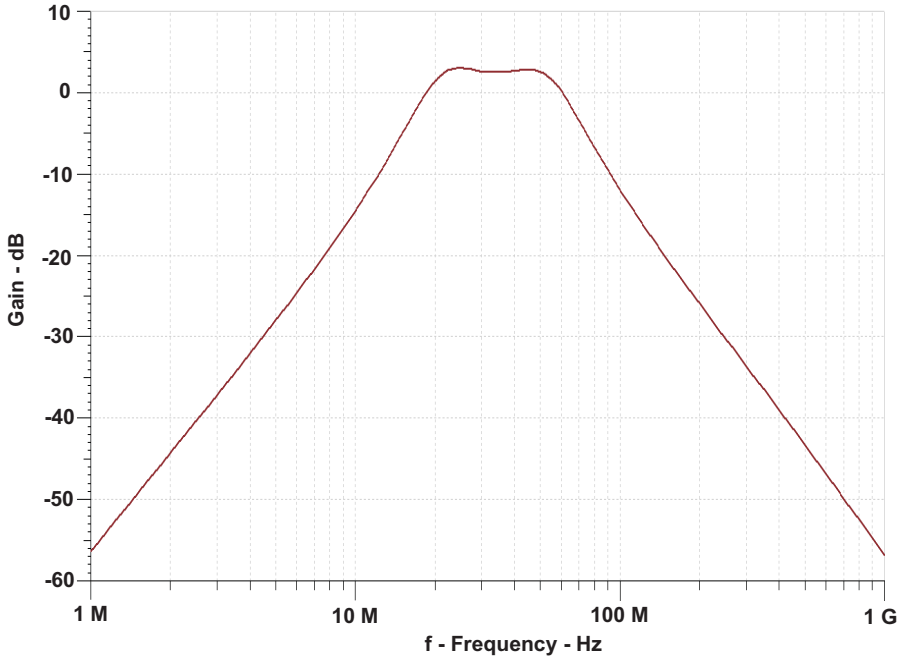

Figure 6. Simulated Filter Response

The same circuit was tested on the bench with ADS5483, for the frequency response as shown in Figure 7.

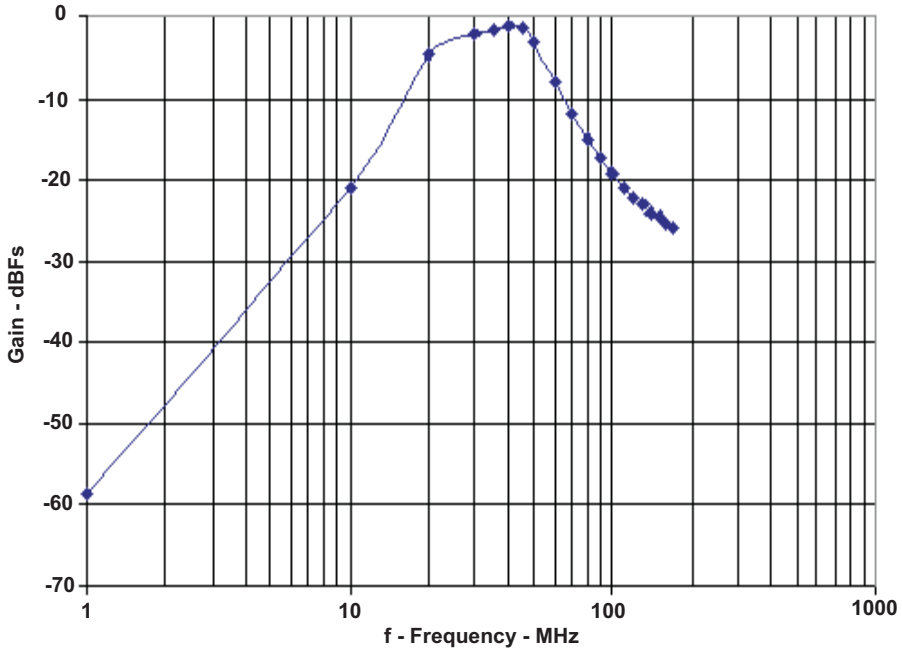

Figure 7. On-Bench Filter Response

The result was captured using the TSW1200 for the input frequency of 57.6 MHz and the sampling frequency of 122.88 MHz.

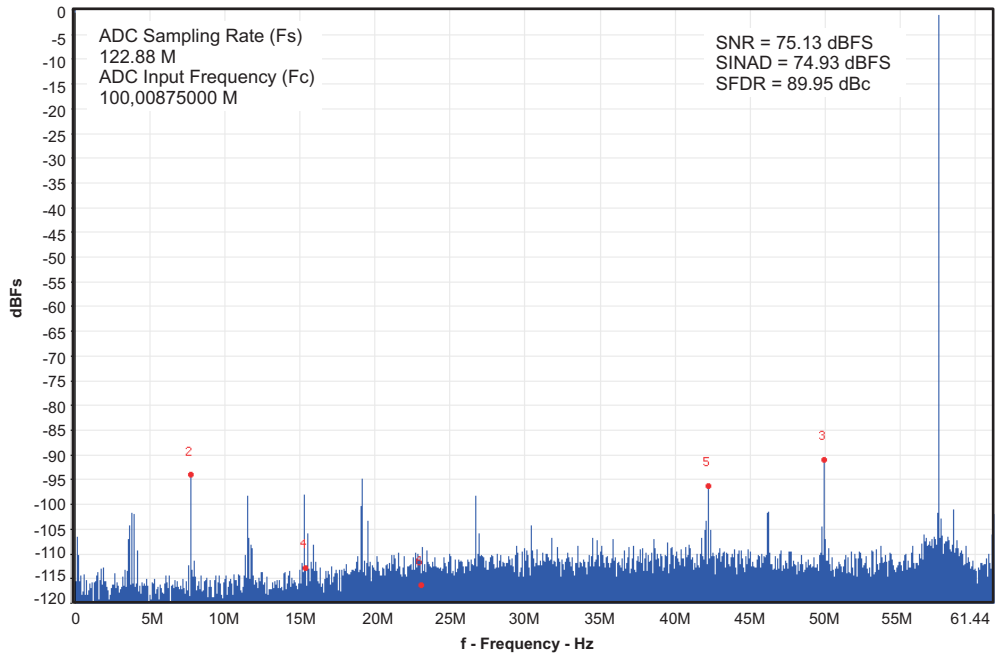

Figure 8. ADC Performance With THS4509

4 Physical Description

This section describes the physical characteristics and printed-circuit board (PCB) layout of the EVM.

4.1 PCB Schematics

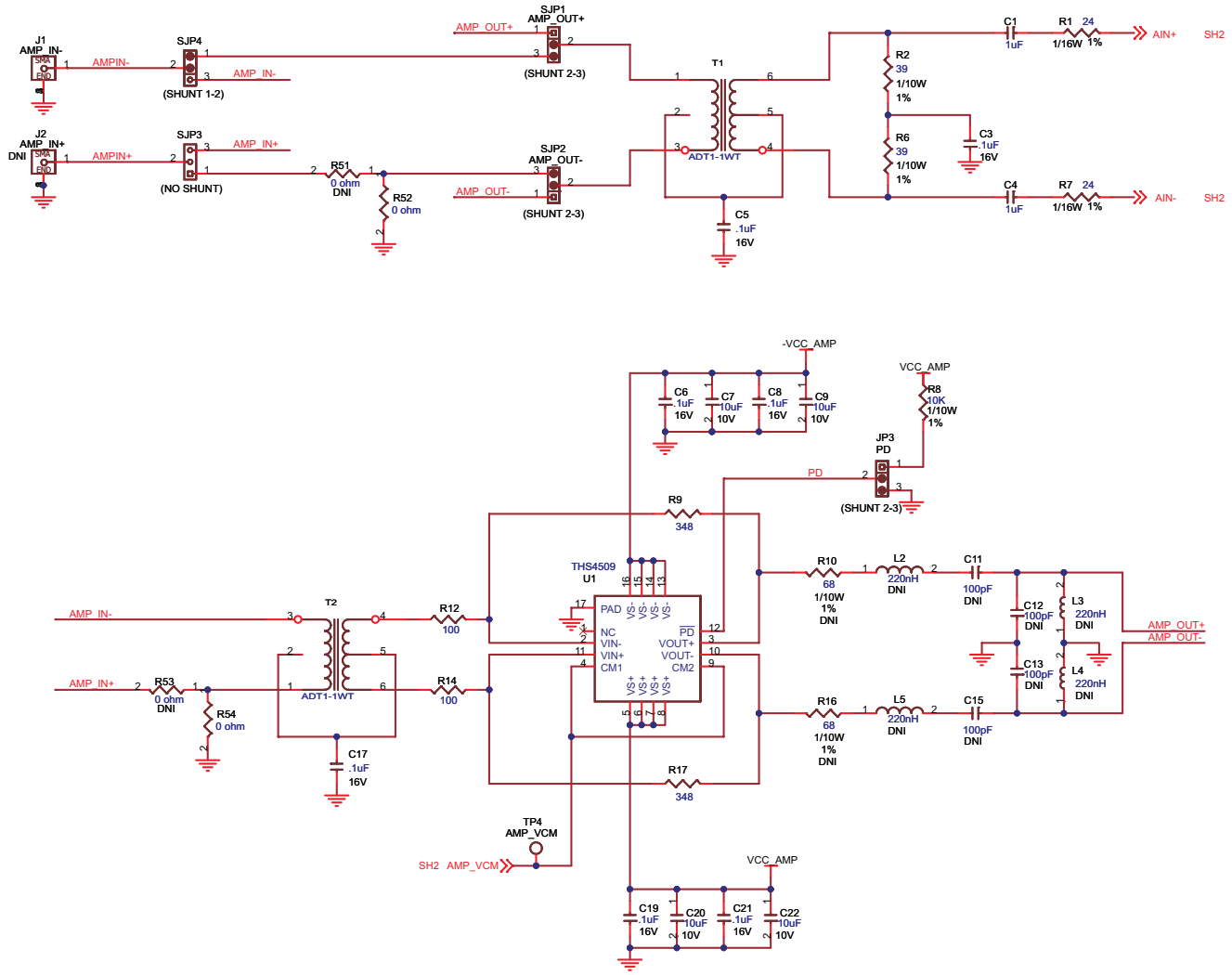

Figure 9. EVM Schematics, Sheet 1

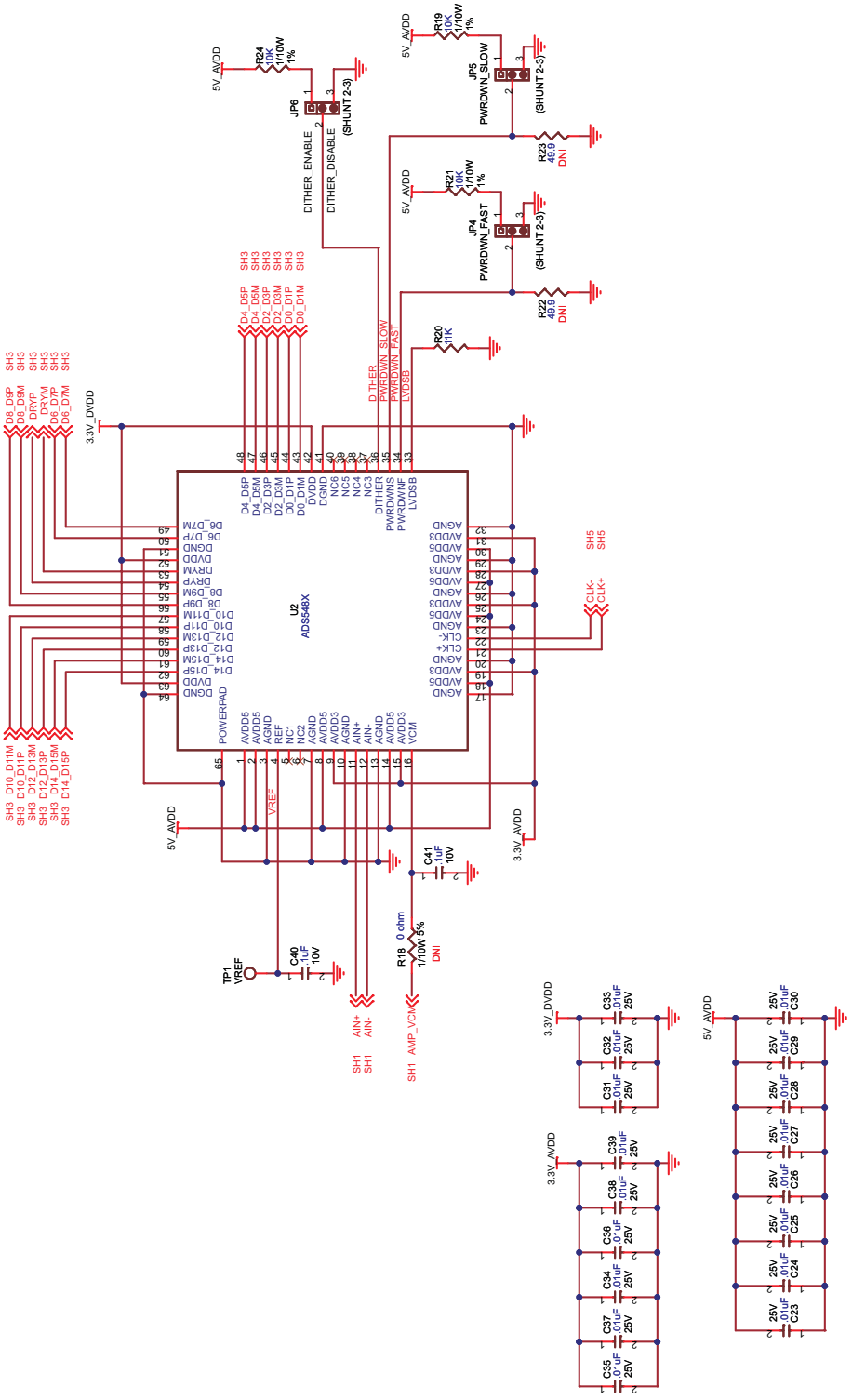

Figure 10. EVM Schematics, Sheet 2

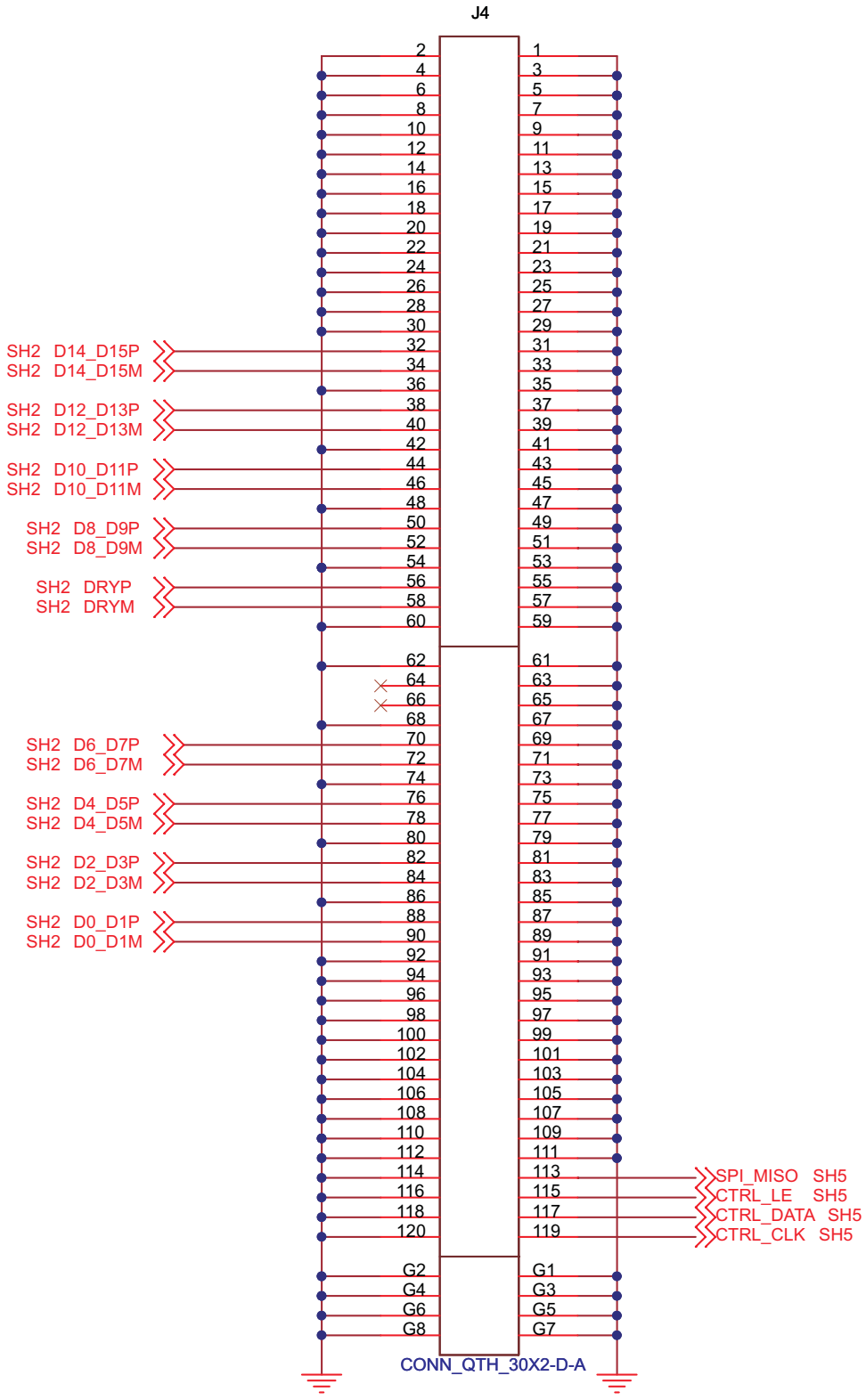

Figure 11. EVM Schematics, Sheet 3

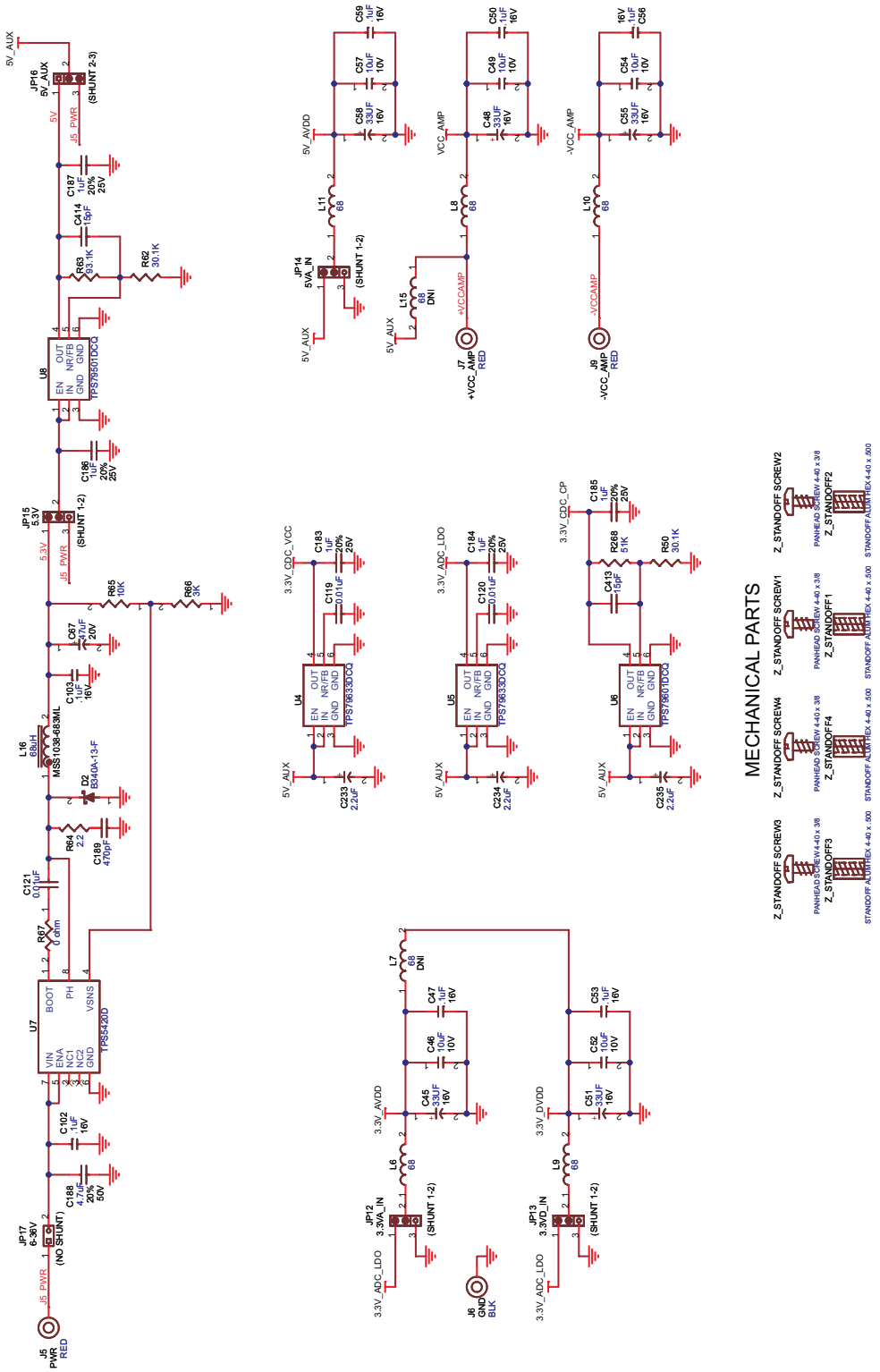

Figure 12. EVM Schematics, Sheet 4

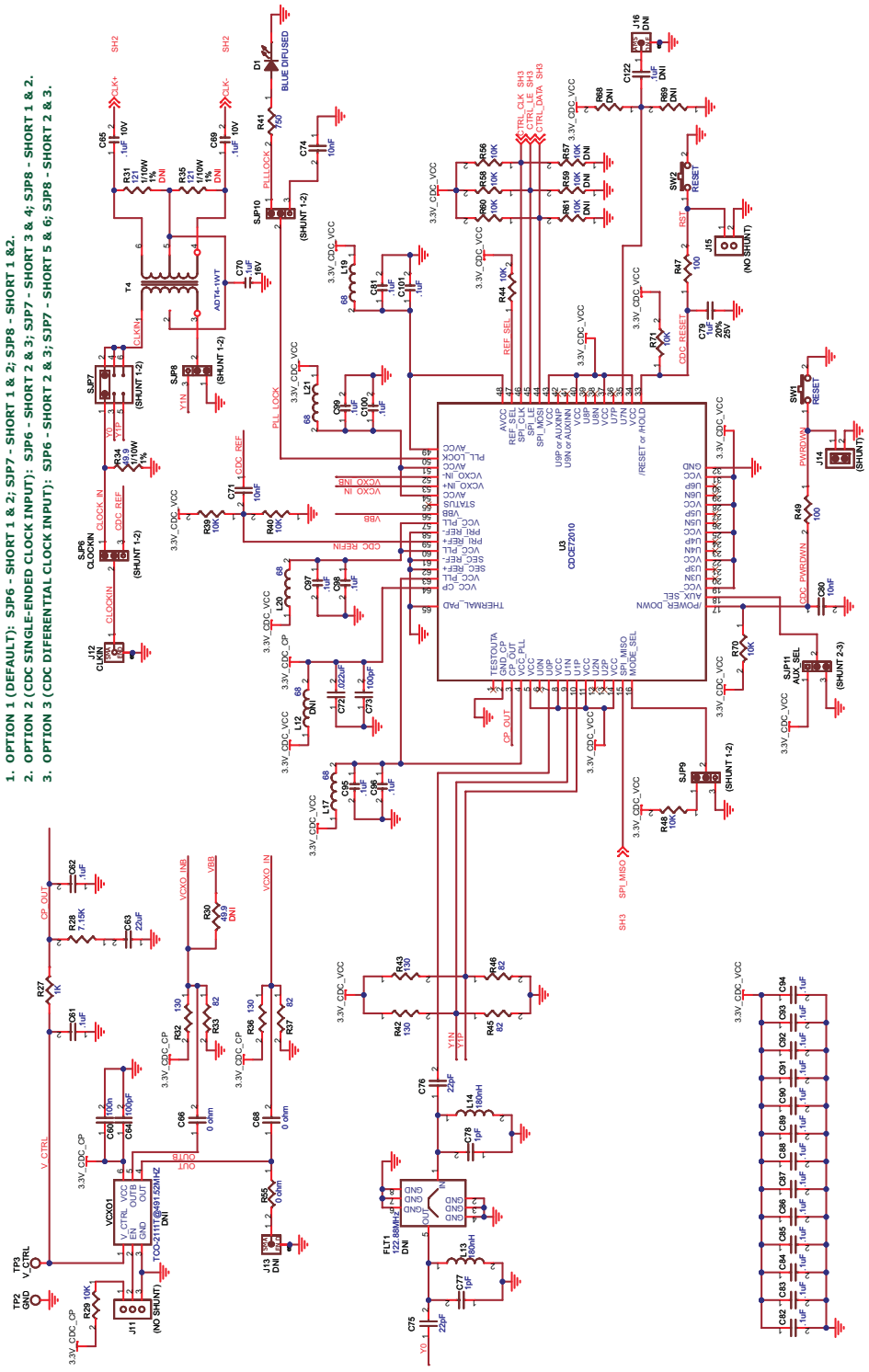

Figure 13. EVM Schematics, Sheet 5

4.2 PCB Layout

The EVM is constructed on a six-layer, 0.062-inch-thick printed-circuit board (PCB) using FR-4 material. The individual layers are shown in Figure 14 through Figure 19. The layout features a common ground plane; however, similar performance can be obtained with careful layout using a split ground plane.

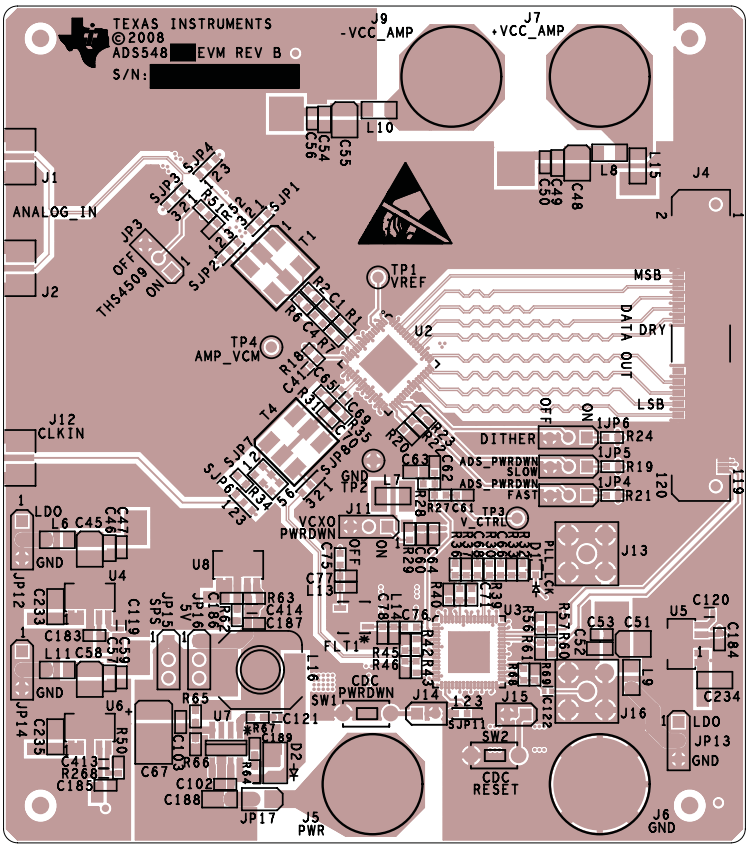

Figure 14. Component Side

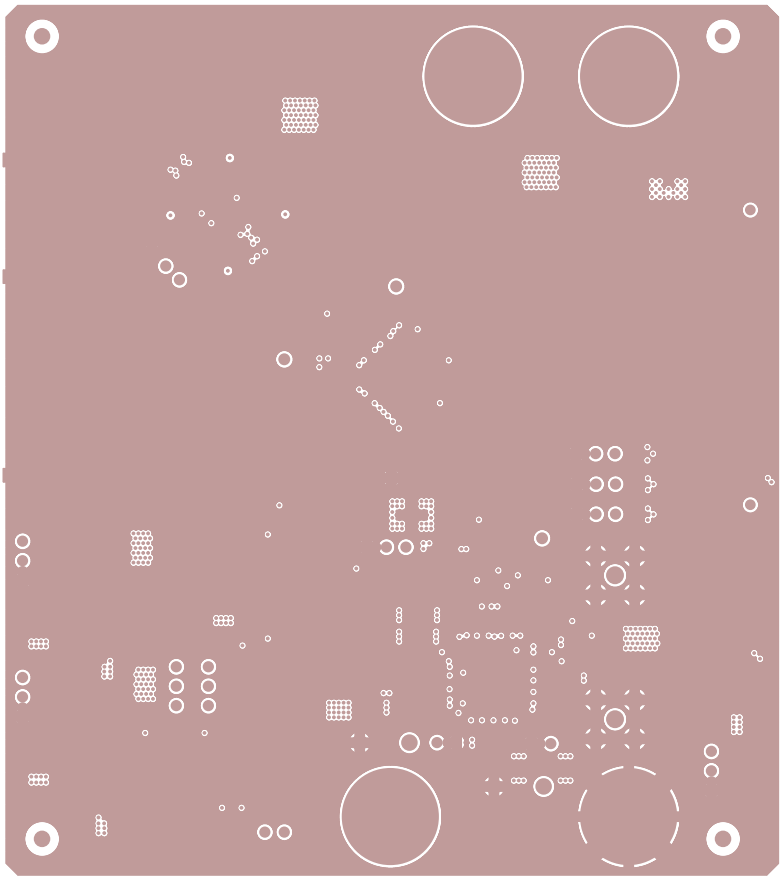

Figure 15. Ground Plane 1

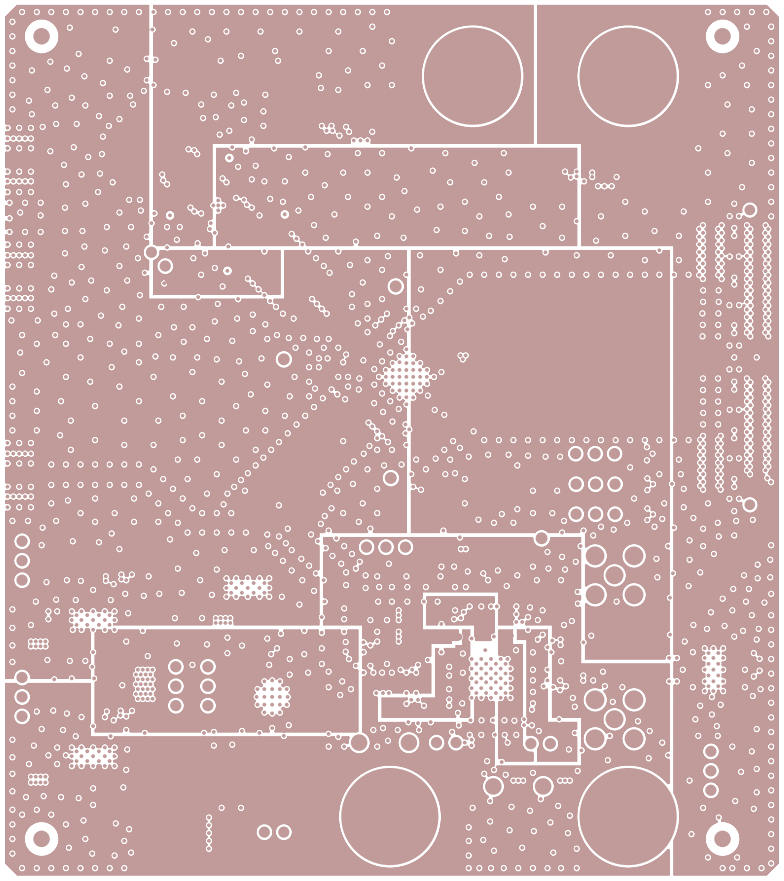

Figure 16. Power Plane 1

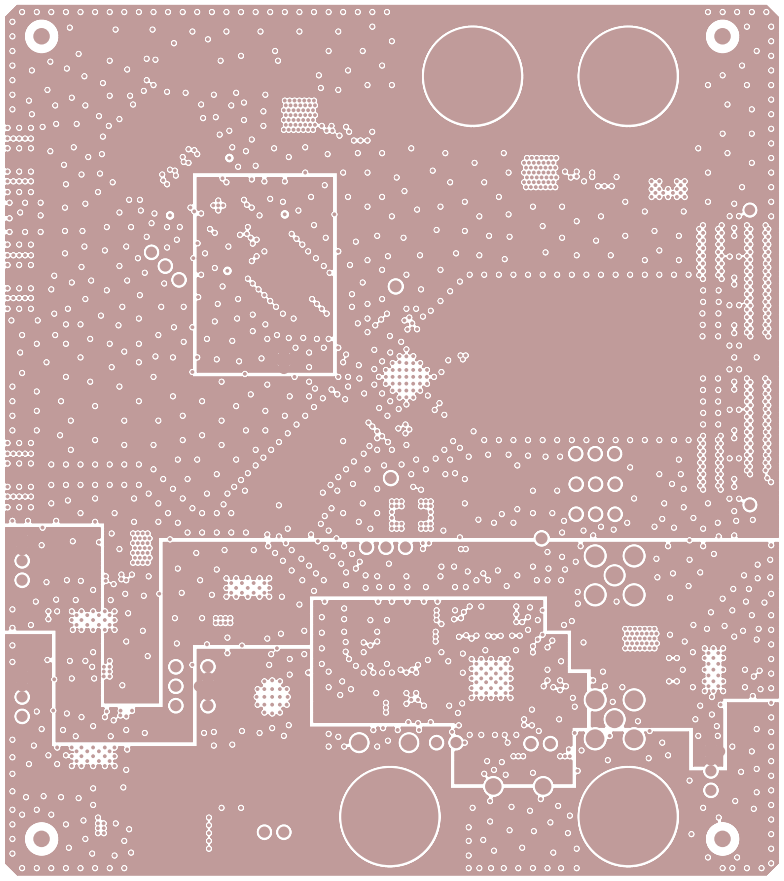

Figure 17. Power Plane 2

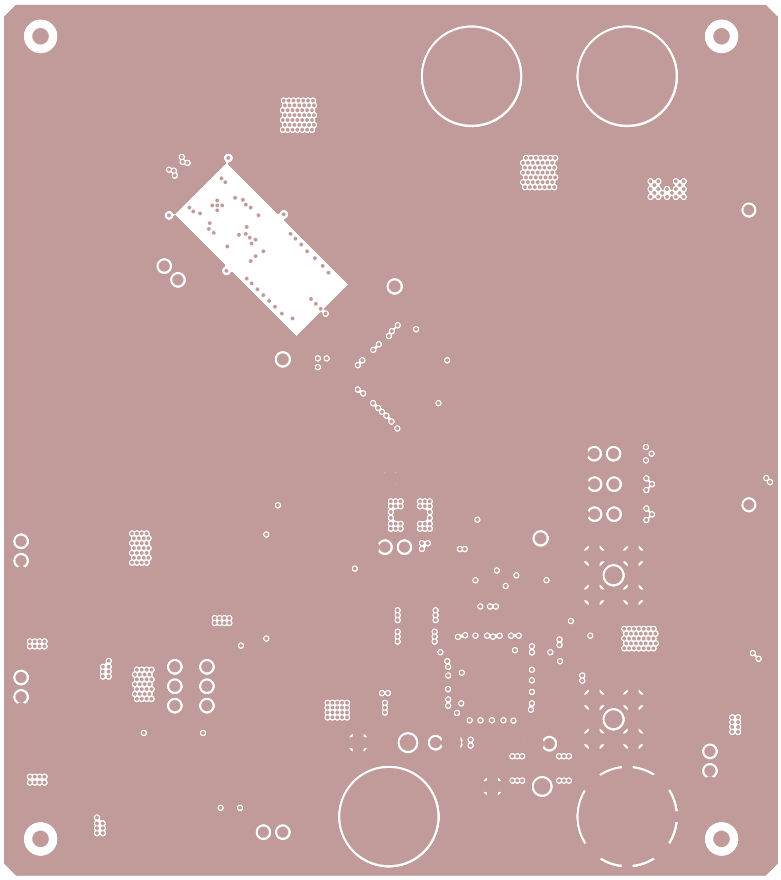

Figure 18. Ground Plane 2

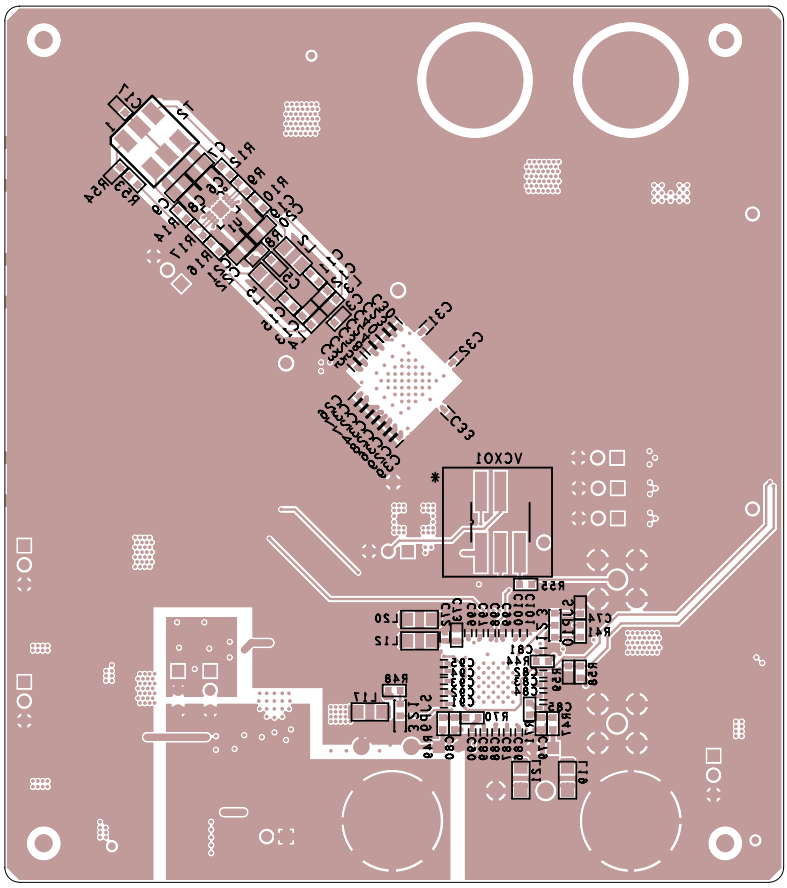

Figure 19. Bottom Side

4.3 Bill of Materials

Qty	Reference	Value	Footprint	MFR.	Part Number	Tol	Volt	Wat	Note
2	C1,C4	1 µF	603	Panasonic	ECJ-1VB1A105K	10%	10V		
6	C3,C5,C6,C17,C19, C21	0.1 µF	603	Panasonic	ECJ-1VB1C104K	10%	16V		
9	C7,C9,C20,C22,C46,C49,C52,C54,C57	10 µF	805	Panasonic	ECJ-2FB1A106K	10%	10V		
1	C8	0.1 µF	603	Panasonic	ECJ-1VB1C104K	10%	16V	1/10W	
0	C11–C13,C15	100 pF	603	Murata	GQM1885C1H101JB01D_DNI				DNI
15	C23–C37	0.01 µF	402	Panasonic	ECJ-0EB1E103K	±10%	25V		
2	C38, C39	0.01 µF	402	Panasonic	ECJ-0EB1E103K	10%	25V		
4	C40, C41, C65, C69	0.1 µF	402	Panasonic	ECJ-0EB1A104K	10%	10V		
5	C45, C48, C51, C55, C58	33 µF	TANT_B	AVX	TPSB336K016R0350	10%	16V		
8	C47, C50, C53, C56, C59, C70, C102, C103	0.1 µF	603	Panasonic	ECJ-1VB1C104K	10%	16V		
1	C60	100 n	603	Panasonic	ECJ-1VB1C104K	10%	16V		
2	C61, C62	0.1 µF	603	Panasonic	ECJ-1VB1C104K	10%	16V		
1	C63	22 µF	805	Panasonic	ECJ-2FB0J226M	20%	6.3V		
2	C64, C73	100 pF	603	Panasonic	ECJ-1VC1H101J	5%	50V		
2	C66, C68	0 Ω	603	DALE	CRCW06030000Z0EA	5%		1/10W	
1	C67	47 µF	TANT_E	AVX	TPSE476M020R0150	10%	20V		
3	C71, C74, C80	10 nF	603	AVX	06035C103KAZ2A	10%	50V		
1	C72	0.022 µF	402	AVX Corporation	0402YC223KAT2A				
2	C75, C76	22 pF	603	AVX	06033J220GBTTR	2%	25V		
2	C77, C78	1 pF	603	Murata	GQM1885C2A1R0CB01D	0.25pF	100V		
6	C79,C183–C187	1 µF	603	Panasonic	ECJ-1V41E105M	20%	25V		
21	C81–C101	0.1 µF	201	Panasonic	ECJ-ZEBFJ104K	5%	50V		
3	C119–C121	0.01 µF	402	Panasonic	ECJ-0EB1E103K	10%			
0	C122	0.1 µF	402	Panasonic	ECJ-0EB1C104K_DNI	10%	16V		DNI
1	C188	4.7 µF	1206	Murata	GRM31CF51H475ZA01L	20%	50V		
1	C189	470 pF	603	Murata	GRM188R71H471MA01D	20%	50V		
3	C233–C235	2.2 µF	1206	Panasonic	ECJ-HVB1A225K				
2	C413,C414	15 pF	402	Panasonic	ECJ-0EC1H150J	5%	50V		
1	D1	Blue diffused	DIODE_SM_HSMN_C170	AVAGO	HSMN-C170				
1	D2	B340A-13-F	DIODE_SM_DO_214AC	Diodes Inc	B340A-13-F				
0	FLT1	122.88 MHz	FILTER_8_SM_150x150	Toyocom	TF2-C2EC1_DNI				DNI
5	JP3–JP6, JP16	HEADER_1x3_100_430L	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-.240				(Shunt 2-3)
4	JP12–JP15	HEADER_1x3_100_430L	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-.240				(Shunt 1-2)
1	JP17	HEADER_1x2_100_430L	HDR_THVT_1x2_100_M	SAMTEC	HMTSW-102-07-G-S-.240				(No shunt)
2	J1, J12	SMA_END_JACK_RND	SMA_SMEL_250x215	Johnson Components	142-0711-821				
0	J2	SMA_END_JACK_RND	SMA_SMEL_250x215	Johnson Components	142-0711-821_DNI				DNI
1	J4	CONN_QTH_30X2-D-A	conn_QTH_30X2-D-A	Samtec	QTH-060-02-F-D-A				
3	J5, J7, J9	Red	JACK_THVT_BANANA_500DIA	SPC Technology	845-R				
1	J6	Black	JACK_THVT_BANANA_500DIA	SPC Technology	845-B				
1	J11	HMTSW-103-07-G-S-.240	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-.240				(No shunt)
0	J13, J16	TI_SILKTEXT	SMA_THVT_320x320	Johnson Components	142-0701-201_DNI				DNI
1	J14	HMTSW-102-07-G-S-.240	HDR_THVT_1x2_100_M	SAMTEC	HMTSW-102-07-G-S-.240				(Shunt)
1	J15	HMTSW-102-07-G-S-.240	HDR_THVT_1x2_100_M	SAMTEC	HMTSW-102-07-G-S-.240				(No shunt)
0	L2, L5	220nH	1206	Coilcraft	1206CS-221X-LB_DNI				DNI
0	L3, L4	220 nH	603	Coilcraft	0603CS-R22X-LU_DNI	2%			DNI
9	L6,L8–L11, L17, L19–L21	68	1206	Panasonic	EXC-ML32A680U				
0	L7, L12, L15	68	1206	Panasonic	EXC-ML32A680U_DNI				DNI

Qty	Reference	Value	Footprint	MFR.	Part Number	Tol	Volt	Wat	Note
2	L13, L14	180 nH	603	Panasonic	ELJ-RER18JF3	5%			
1	L16	68 µH	IND_SM_MSS1038	Coilcraft	MSS1038-683ML				
2	R1, R7	24	603	Panasonic	ERJ-3GEYJ240V	1%		1/16W	
2	R2, R6	39	603	Panasonic	RC0603FR-0739RL	1%		1/10W	
4	R8, R19, R21, R24	10K	603	Panasonic	ERJ-3EKF1002V	1%		1/10W	
2	R9, R17	348	603	Panasonic	ERJ-3EKF3480V	1%		1/10W	
0	R10, R16	68	603	Panasonic	ERA-3AEB680V_DNI	1%		1/10W	DNI
2	R12, R14	100	603	Panasonic	ERJ-3EKF1000V	1%		1/10W	
0	R18	0 Ω	603	Panasonic	ERJ-3GEY0R00V_DNI	5%		1/10W	DNI
1	R20	11K	603	Panasonic	ERJ-3EKF1102V	1%		1/10W	
0	R22, R23, R30	49.9	603	Panasonic	ERJ-3EKF49R9V_DNI	1%		1/10W	DNI
1	R27	1K	603	Panasonic	ERJ-3EKF1001V				
1	R28	7.15K	603	Yageo	RT0603DRD077K15L	0.50%		1/10W	
11	R29, R39, R40, R44,R48, R56, R58, R60, R65, R70, R71	10K	603	DALE	CRCW060310K0FKEA	1%		1/10W	
0	R31, R35	121	603	Panasonic	ERJ-3EKF1210V_DNI	1%		1/10W	DNI
4	R32, R36, R42, R43	130	603	DALE	CRCW0603130RFKEA	1%		1/10W	
4	R33, R37, R45, R46	82	603	DALE	CRCW060382R0FKEA	1%		1/10W	
1	R34	49.9	603	Panasonic	ERJ-3EKF49R9V	1%		1/10W	
1	R41	750	603	DALE	CRCW0603750RFKEA				
2	R47, R49	100	603	DALE	CRCW0603100RFKEA	1%		1/10W	
2	R50, R62	30.1K	603	Panasonic	ERJ-3EKF3012V	1%	1/10 W		
0	R51, R53	0 Ω	603	DALE	CRCW06030000Z0EA_DNI	5%		1/10W	DNI
4	R52, R54, R55, R67	0 Ω	603	DALE	CRCW06030000Z0EA	5%		1/10W	
0	R57, R59, R61	10K	603	DALE	CRCW060310K0FKEA_DNI	1%		1/10W	DNI
1	R63	93.1K	603	Panasonic	ERJ-3EKF9312V	1%	1/10 W		
1	R64	2.2	603	Panasonic	ERJ-3RQF2R2V	1%	1/10 W		
1	R66	3K	603	Yageo	RC0603FR-073KL	1%		1/10W	
0	R68, R69	10K	603	DALE	CRCW060310K0FKEA_DNI	1%		1/10W	DNI
1	R268	51K	402	Panasonic	ERJ-S02F5102X	1%			
3	SJP1, SJP2, SJP11	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI				(Shunt 2-3)
1	SJP3	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI				(No shunt)
5	SJP4, SJP6, SJP8–JP10	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI				(Shunt 1-2)
1	SJP7	JUMPER_3X2_SMT	SMD_BRIDGE_2x3_0603	DNI	DNI				(Shunt 1-2)
2	SW1, SW2	RESET	SW_THVT_SPST_PTS635SL43	ITT Industries/ C&K Div	PTS635SL43				
3	TP1–TP3	TP_THVT_060_RND-WHT	TP_THVT_060_RND	Components Corporation	TP-105-01-09				
1	TP4	Test Point Black	TP_THVT_060_RND	Keystone	5001				
2	T1, T2	ADT1-1WT	TRANS_SMVT_CD542_6	Mini Circuits	ADT1-1WT				
1	T4	ADT4-1WT	TRANS_SMVT_CD542_6	Mini Circuits	ADT4-1WT				
1	U1	THS4509	QFN_16_124x124_pwrpad	Texas Instruments	THS4509RGTT				TI Supplied
1	U2	ADS548X	QFN64	Texas Instruments	ADS548X				TI Supplied
1	U3	CDCE72010	QFN64	Texas Instruments	CDCE72010				TI Supplied
2	U4, U5	TPS79633DCQ	SOT_223_6_TG	Texas Instruments	TPS79633DCQ				TI Supplied
1	U6	TPS79601DCQ	SOT_223_6_TG	Texas Instruments	TPS79601DCQ				TI Supplied
1	U7	TPS5420D	SOIC_8_197x157_50	Texas Instruments	TPS5420D				TI Supplied
1	U8	TPS79501DCQ	SOT_223_6_TG	Texas Instruments	TPS79501DCQ				TI Supplied
0	VCXO1	TCO-2111T at 491.52MHz	VCXO_6_Custom2	TOYOCOM	TCO-2111T at 491.52MHz_DNI				DNI
10	Z_SH-H1–Z_SH-H10	Shunt-header		Keltron	MJ-5.97-G or equivalent				Shunt for header

Qty	Reference	Value	Footprint	MFR.	Part Number	Tol	Volt	Wat	Note
9	Z_SH-J1, Z_SH-J2, Z_SH-J4,– Z_SH-J10	Shunt-jumper-0603		Panasonic	ERJ-3GE0R00X				Shunt for jumper
4	Z_STANDOFF SCREW1– Z_STANDOFF SCREW4	Panhead Screw 4-40 x 3/8		Building Fasteners	PMS 440 0038 PH				Screw for standoff
4	Z_STANDOFF1– Z_STANDOFF4	Standoff Alum Hex 4-40 x .500		Keystone	2203				Standoff

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