ADS42LBx9EVM

The ADS42LB49 and ADS42LB69 are dual-channel, 250-MSPS, analog-to-digital converters that are 14-bit and 16-bit resolutions, respectively. The ADS42LB49EVM and ADS42LB69EVM (ADS42LBx9EVM) are specifically suited for interfacing with TI's TSW1400EVM to capture and display waveforms from the ADC. The EVM schematic, BOM, and layout files are found in the design package in the ADS42LBx9EVM product folder on www.ti.com.

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1 Introduction

1.1 Overview

The ADS42LB49EVM and ADS42LB69EVM (ADS42LBx9EVM) are evaluation modules (EVMs) that allow for the evaluation of TI's ADS42LB49 and ADS42LB69. The ADS42LB49 and ADS42LB69 (ADS42LBx9) are dual-channel, low-power, 250-MSPS analog-to-digital converters (ADC) with 14-bit and 16-bit resolutions, respectively and buffered analog inputs and LVDS outputs. The EVM has transformer coupled analog and clock inputs to accommodate a wide range of signal sources and frequencies. The ADS42LBx9 is programmable through an easy-to-use software GUI enabling quick configuration for a variety of uses.

The ADS42LBx9EVM is designed to mate with the TSW1400EVM which is a full-function data-capture card. The High Speed Data Converter Pro (HSDCPro) software GUI can then process the data from the TSW1400EVM to quickly assess the performance of the ADS42LBx9. It is also compatible with Altera and Xilinx FPGA development platforms which have FMC or HSMC connectors, via the appropriate interposer card.

1.2 Block Diagram

The block diagram for the ADS42LBx9EVM is shown in Figure 1. The various inputs, outputs, and jumpers of the ADS42LBx9EVM are described in Table 1.

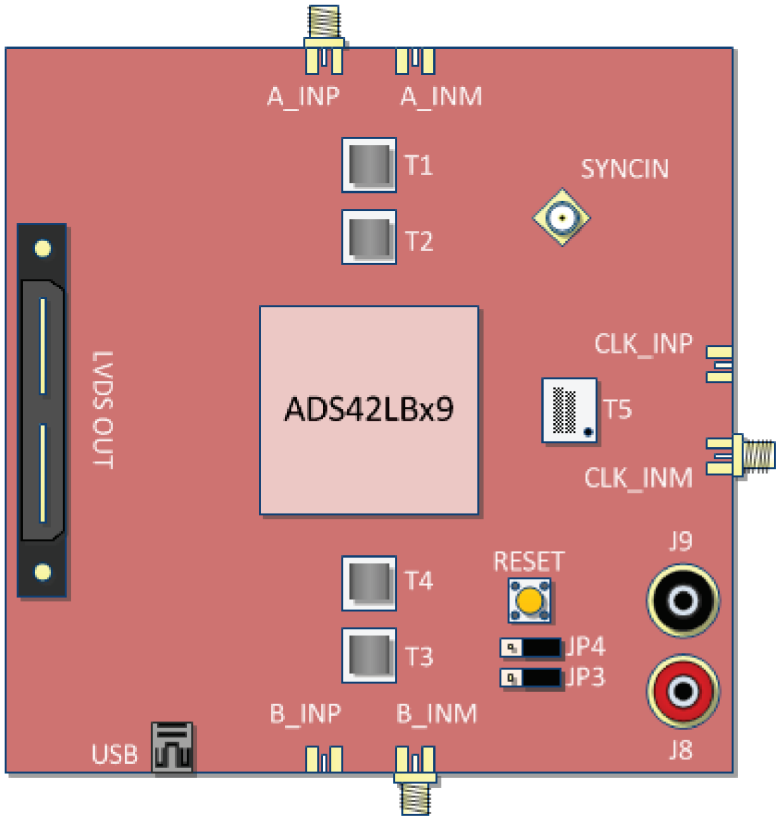

Figure 1. Block Diagram of the ADS42LBx9EVM

Table 1. Input and Output Connectors and Jumper Descriptions of the ADS42LBx9EVM

Component	Description
A_INP	Single-ended analog input for channel A
B_INM	Single-ended analog input for channel B
CLK_INM	Single-ended ADC clock input
J8	Positive power connection (3.3 V)
J9	Negative power connection (GND)
USB	USB connection
LVDS OUT	LVDS connector to connect to the TSW1400
SYNCIN	ADC sync input
RESET	Switch to reset the ADC using the RESET pin
JP4	ADC CNTRL1 pin, controls power down modes (default: short 2-3)
JP3	ADC CNTRL2 pin, controls power down modes (default: short 2-3)

2 Software Control

This section provides installation instructions for the ADS42LBx9 GUI and descriptions of the various controls.

2.1 Installation Instructions

1. The software can be downloaded from the ADS42LB69EVM product page on www.ti.com. Find the page by searching for *ADS42LB69EVM*.
2. Extract the files from the zip file named *ADS42LBx9 GUI vXpY installer.zip* where XpY represents the version number.
3. Run *setup.exe* and follow the installation prompts.
4. Start the GUI by going to **Start Menu** → **All Programs** → **Texas Instruments ADCs** → **ADS42LBx9 GUI**.
5. When plugging the board into the computer for the first time through the USB cable, you are prompted to install the USB drivers.
   - Windows® XP: If Windows XP does not automatically install the drivers, follow the prompts on the screen to do so. Do not let Windows XP search Microsoft Update for the drivers, but do let Windows XP install the drivers automatically.
   - Windows 7: After installing the GUI, Windows 7 should automatically be able to install the drivers for the ADS42LBx9EVM with no input from the user.

2.2 Software Operation

The software GUI allows full programming control of the ADS42LBx9 device. Figure 2 shows the GUI front panel which contains a block diagram of the ADS42LBx9. Clicking on the various blocks of the ADS42LBx9 allows configuration of the settings for that block. Detailed descriptions for each screen of the GUI are given in this section. Please refer to the ADS42LBx9 datasheet (SLAS904) for more detailed explanations of the register fields.

2.2.1 Top Level

Figure 2 shows the top-level view of the GUI which contains the block diagram of the ADS42LBx9. The blue blocks can be clicked on to see the controls for that block. Along the top of the GUI are **SEND**, **READ**, **SAVE**, and **LOAD** buttons. The **SEND** and **READ** buttons write or read all of the registers of the ADS42LBx9. The **SAVE** and **LOAD** buttons can be used to save or load a text file of the registers. The flashing **RESET** button can be clicked to reset the USB port connection. It reads **CONNECTED** when the GUI is successfully connected to the EVM. On the right side is a white text box that shows the registers as they are written to the device, it also shows the results of a read command.

The ADS42LBx9 reset and powerdown controls are available in the top-left corner, for easy access. The reset control automatically clears in the device, so only a single mouse click is needed. The **DEVICE ON** button displays **DEVICE OFF** when clicked and the device has been powered down. Monitoring the power suppy current when toggling the power down mode is a simple way to verify that the GUI is communicating with the device. Finally, the *Divide by 1,2,4* block is a control that sets the internal clock divider. The clock divider value is shown above the block. Note that clicking on this block does not take the user away from the top-level screen.

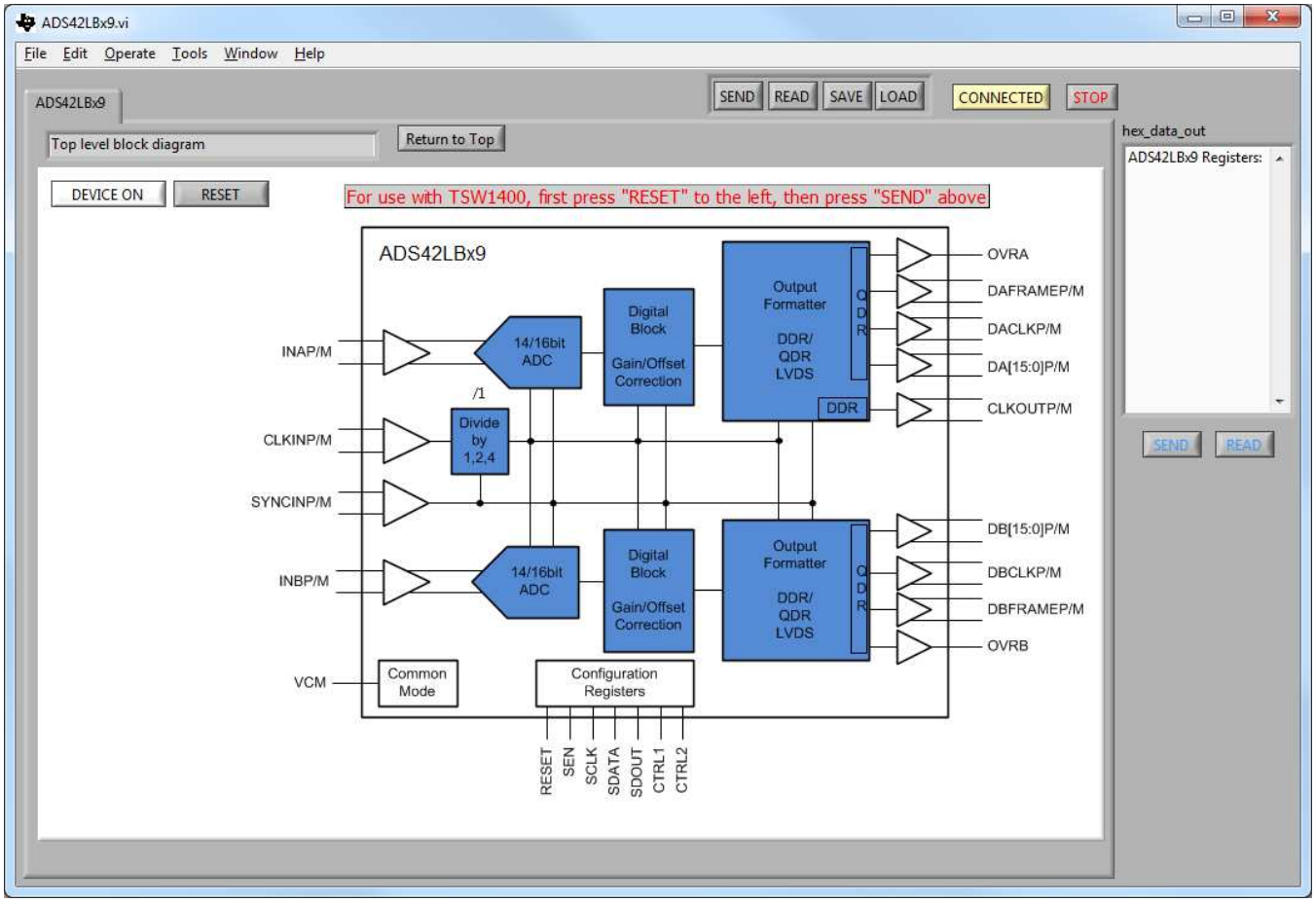

Figure 2. Top-Level Block Diagram Window of the ADS42LBx9 GUI

2.2.2 ADC Controls

Clicking on either *14 or 16bit ADC* block takes the user to the *ADC Controls* window, shown in Figure 3. The *ADC Controls* window controls various ADC functions such as the data format, overrange detection, and test patterns. Table 2 describes the controls seen in this window. Select the **Return to Top** button to return to the top-level block diagram.

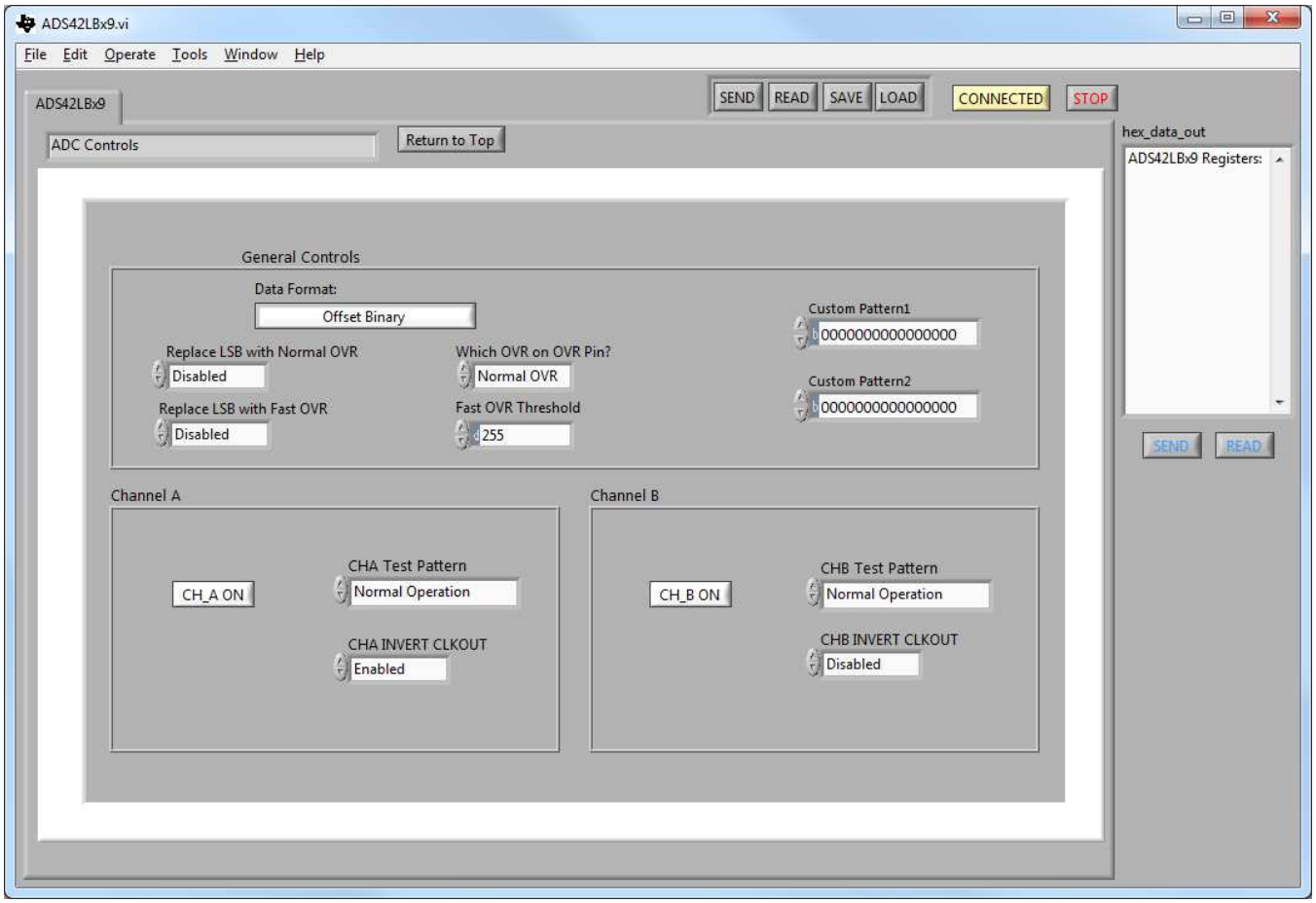

Figure 3. ADC Controls Window of the ADS42LBx9 GUI

Table 2. ADC Controls Window Descriptions

Control	Description
Data Format	Set the output data format as offset binary or 2's compliment
Replace LSB with Normal OVR	Use the LSB as the normal OVR output
Replace LSB with Fast OVR	Use the LSB as the fast OVR output
Which OVR on OVR Pin?	Select which OVR signal should be output on the OVR pin
Fast OVR Threshold	Set the threshold for the fast OVR function
Custom Pattern1	Write a custom test pattern here
Custom Pattern2	Write a custom test pattern here
CH_A ON	Turn on and off channel A
CHA Test Pattern	Select various test pattern modes for channel A
CHA INVERT CLKOUT	Invert the channel A output clock when in 2xDDR mode
CH_B ON	Turn on and off channel B
CHB Test Pattern	Select various test pattern modes for channel B
CHB INVERT CLKOUT	Invert the channel B output clock when in 2xDDR mode

2.2.3 Digital Block Controls

Clicking on either *Digital Block* region brings up the *Digital Block Controls* window, shown in Figure 4. Descriptions for the various controls are given in Table 3.

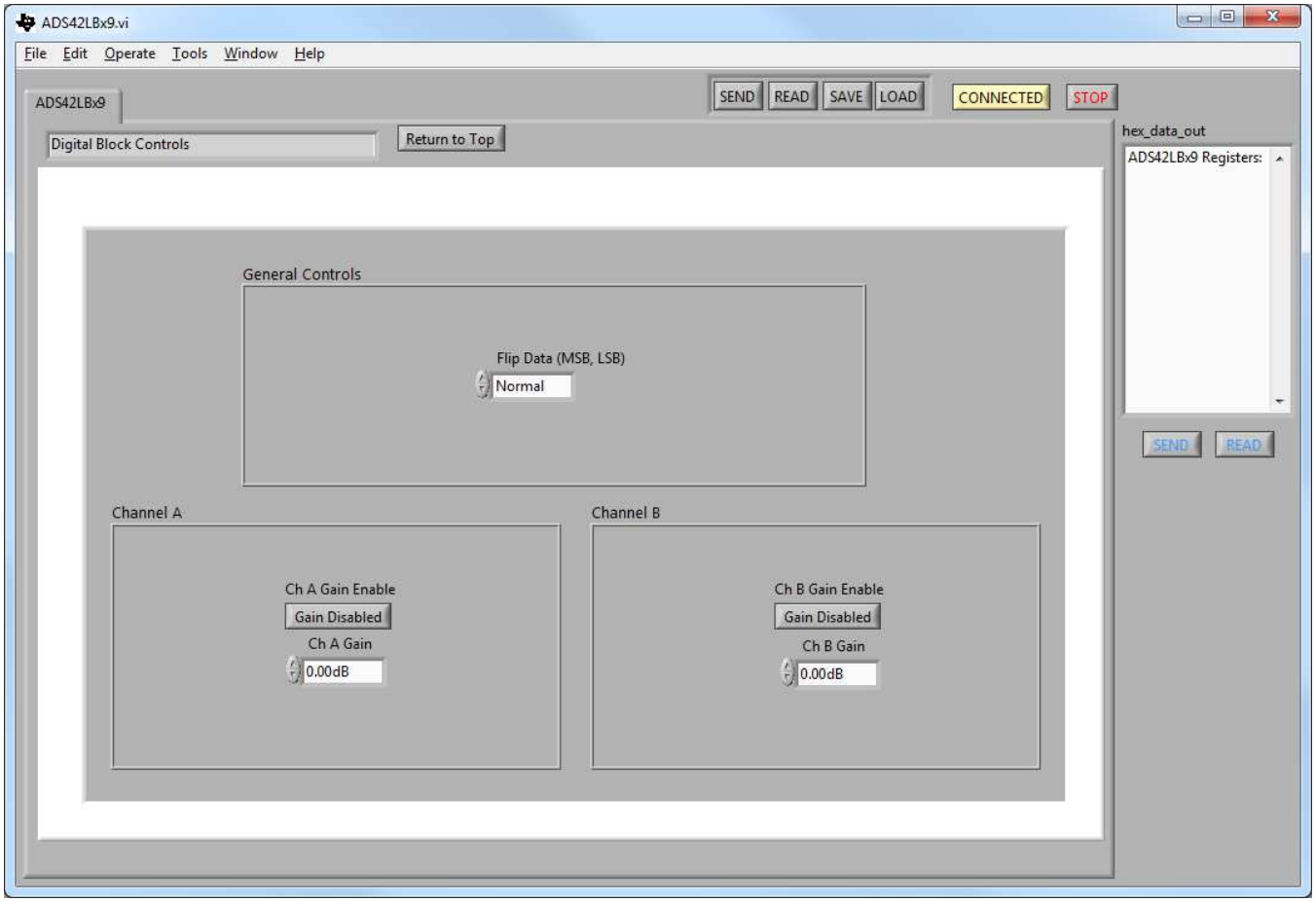

Figure 4. Digital Block Controls Window of the ADS42LBx9 GUI

Table 3. Digital Block Controls Window Descriptions

Control	Description
Flip Data (MSB, LSB)	Reverse the order of the digital output bits, such that the MSB changes to the LSB pin
Ch A Gain Enable	Enable or disable the gain feature of channel A
Ch A Gain	Set the gain of channel A
Ch B Gain Enable	Enable or disable the gain feature of channel B
Ch B Gain	Set the gain of channel B

2.2.4 LVDS Controls

Clicking on either *Output Formatter* block opens the *LVDS Controls* window, shown in Figure 5. Descriptions for the various controls are given in Table 4.

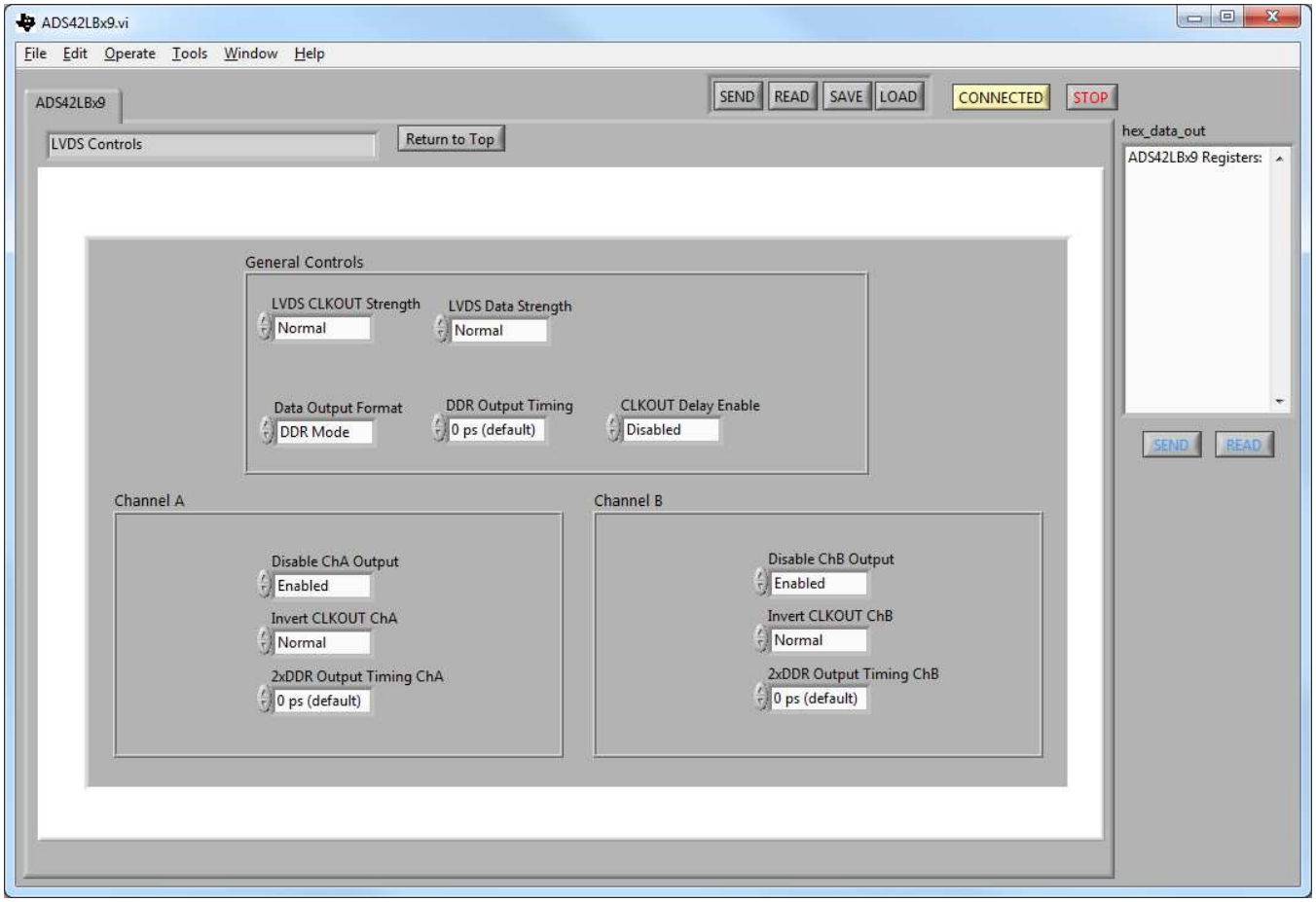

Figure 5. LVDS Controls Window of the ADS42LBx9 GUI

Table 4. LVDS Controls Window Descriptions

Control	Description
LVDS CLKOUT Strength	Set the strength of the LVDS data output clock
LVDS Data Strength	Set the strength of the LVDS data outputs
Data Output Format	Set the data output format as DDR mode or 2xDDR mode
DDR Output Timing	Shift the clock edge relative to the data edge
CLKOUT Delay Enable	Enable or disable the DDR output timing adjustment
Disable ChA Output	Disable the output buffer of channel A
Invert CLKOUT ChA	Invert the clock output of channel A in 2xDDR mode
2xDDR Output Timing ChA	Shift the channel A clkout to data timing in 2xDDR mode
Disable ChB Output	Disable the output buffer of channel B
Invert CLKOUT ChB	Invert the clock output of channel B in 2xDDR mode
2xDDR Output Timing ChB	Shift the channel B clkout to data timing in 2xDDR mode

3 Basic Test Setup

This section outlines basic testing of the ADS42LBx9EVM.

3.1 Test Block Diagram

The test setup for the ADS42LBx9EVM is shown in Figure 6. The TSW1400EVM is used to capture data from the ADS42LBx9, which is then transferred to the computer for analysis in the HSDCPro software tool. The analog signal source shown is an HP8644B signal generator, however any analog signal source can be used. The clock source is also an HP8644B, but other clock sources can be used, such as a TI clock-chip EVM. Note that there are filters on both the analog and clock sources, which is necessary to achieve the best performance.

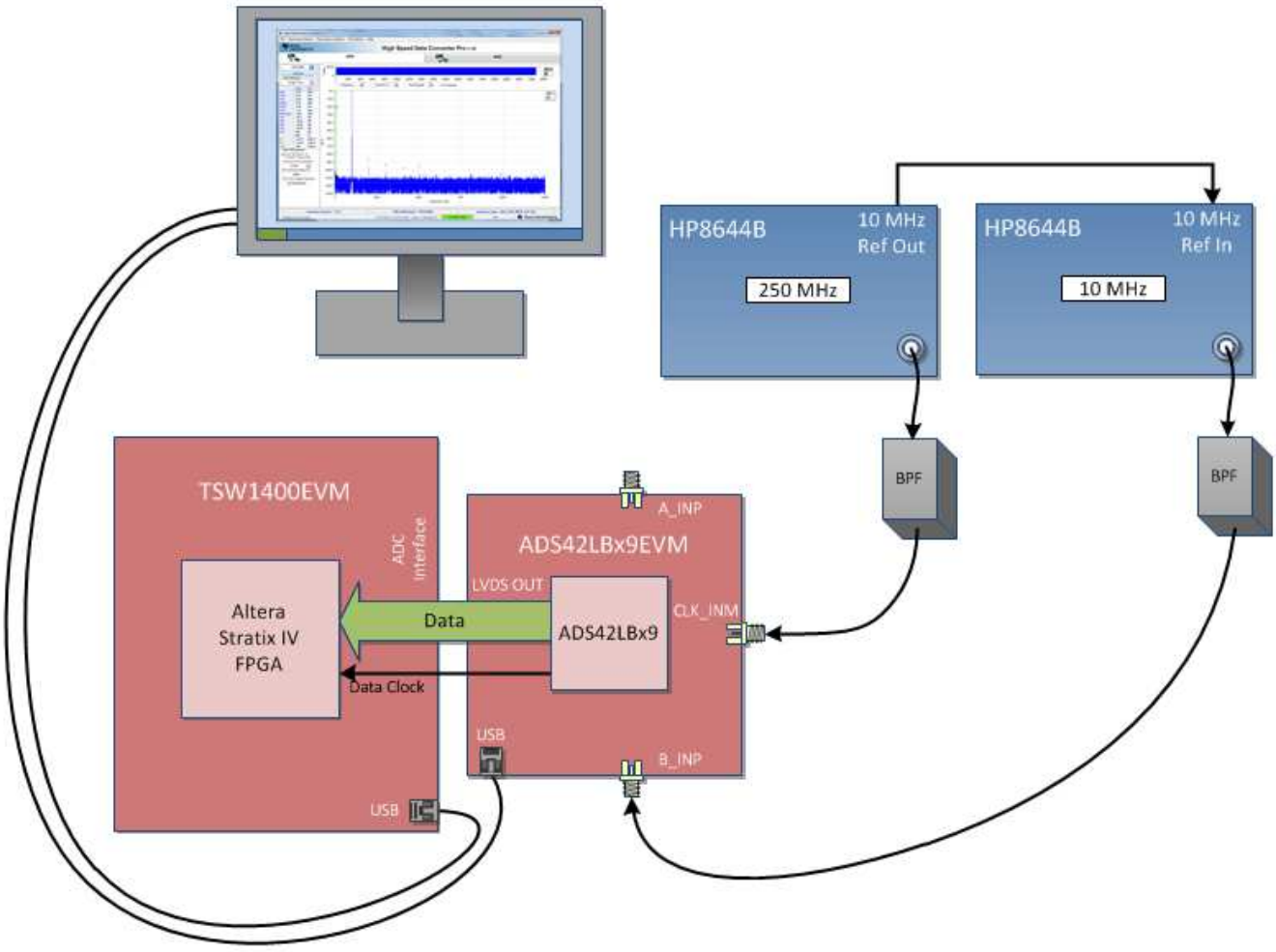

Figure 6. Quick Start Test Setup for the ADS42LBx9EVM

3.2 TSW1400EVM Setup

See the TSW1400EVM User's Guide (SLWU079) for a more detailed explanation of the TSW1400 setup and its features. This document assumes that the HSDCPro software and the TSW1400 pattern capture and generation board are both installed and functioning properly. This information can be found at http://www.ti.com/tool/tsw1400evm

http://www.ti.com/tool/tsw1400evm.

3.3 ADS42LBx9EVM Quick-Start Procedure

3.3.1 TSW1400 Data Capture Card

1. Connect a 5-V power supply to connector *J12* of the TSW1400EVM.
2. Flip switch *SW7* to the *ON* position.
3. Insert a USB cable into the USB port on the TSW1400. Connect the other end to the PC.

3.3.2 ADS42LBx9EVM

1. Connect a 3.3-V power supply to the banana jacks, *J8* and *J9*. Connect the positive end to *J8* and the negative end to *J9*.
2. Connect a USB cable to the USB port on the ADS42LBx9EVM and connect the other end to the PC.
3. Connect a clock to the SMA connector labeled *CLK_INM*. The maximum clock frequency is 250 MHz and the clock should be around 1 Vpp. A smaller voltage may reduce the SNR performance. A bandpass filter should be placed on the clock in order to achieve the best SNR performance.
4. Connect a signal source to either analog input SMA connector, *A_INP* or *B_INM*. For single-tone testing, a bandpass filter should be used to achieve the best SNR and harmonic performance.
5. Connect the ADS42LBx9EVM to the TSW1400 by connecting *J7* on the ADS42LBx9EVM to the ADC Interface connector on the bottom of the TSW1400.
6. Press the *RESET* switch, *SW1*.

3.3.3 ADS42LBx9 GUI

1. Start the ADS42LBx9 GUI by selecting **Start Menu → Program Files → Texas Instruments ADCs → ADS42LBx9 GUI**.
2. In the upper right-hand corner is either a flashing red and yellow button showing *RESET* or a yellow button that says *CONNECTED*. if it says *RESET*, then click the button until it reads *CONNECTED* and stops flashing. This indicates that the ADS42LBx9EVM is connected to the computer.
3. By default, the GUI controls are setup for use with the TSW1400. In order to program it in the correct mode, first press the **RESET** button to the top-left of the block diagram (Figure 2).
4. Pressing the **SEND** button at the top of the GUI, sends all the registers. By default, this puts the ADC into the DDR output format and into offset binary mode.

3.3.4 High Speed Data Converter Pro (HSDCPro)

1. Start the HSDCPro software tool by selecting **Start Menu → All Programs → Texas Instruments ADCs → High Speed Data Converter Pro**.
2. When prompted for the serial number of the board, select the serial number that represents the TSW1400 that has been connected to the ADS42LBx9. This number is on a sticker on the TSW1400 board.
3. In the *Select ADC* drop-down box select either *ADS42LB49* or *ADS42LB69*, depending on which EVM is being used. If it asks to download the firmware, select *Yes*. Multiple LEDs light up on the TSW1400, once the firmware has finished downloading.
4. Select *Single Tone* from the *Test Selection* drop-down menu.
5. At the bottom-left corner, enter *250M* in the *ADC Sampling Rate (Fs)* box, or another value if a clock other than 250 MHz is used. Enter the input frequency into the *ADC Input Target Frequency* box. Press the Enter key.
6. If a windowing function is desired, then *Blackman* should be selected above the plot window. If the signals are synchronized and coherent, select *Rectangular*.
7. All boards and software are now setup. Click the *Capture* button. A sample capture is shown in Figure 7 for the ADS42LB69 with a 250-MHz clock and 10-MHz input frequency.

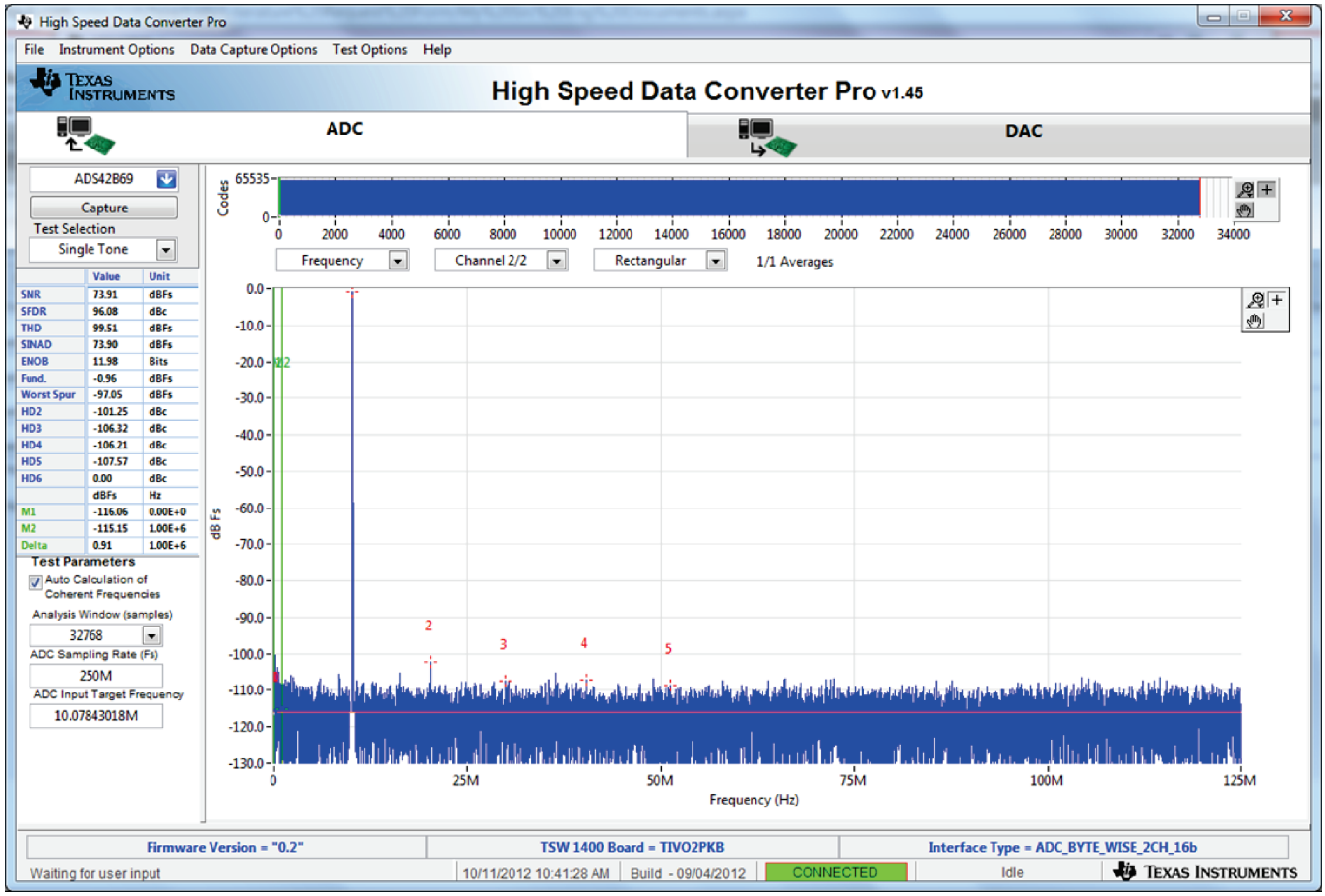

Figure 7. ADS42LB69 Sample Capture using the TSW1400

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Caution

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Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

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2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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