EVS32M16T-5B
1Gbit Double-Data-Rate (DDR) SDRAM

Datasheet - *Preliminary Specification*

Features

- Utilizes 2 Micron MT46V32M16P-5B IT components in 32 Meg x 6 stacked package
- V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture (x 16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x 16 has two - one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto Refresh
- Longer lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL_2 compatible)
- Concurrent auto precharge option is supported
- ^{t}RAS lockout supported (^{t}RAP = ^{t}RCD)
- Industry standard 66-pin TSOP II (400 mil) footprint
- Industrial Temperature rating of -40ºC to +85ºC
- Detailed information on the MT46V32M16P-5B IT SDRAMs can be downloaded here.

KEY TIMING PARAMETERS

SPEED GRADE	CLOCKRATE			DATA-OUT WINDOW	ACCESS WINDOW	DQS-DQ SKEW
	CL = 2*	CL = 2.5*	CL = 3			
-5B	133 MHz	167 MHz		1.6 ns	±0.70 ns	±0.40 ns

*** CL = CAS (Read) Latency**

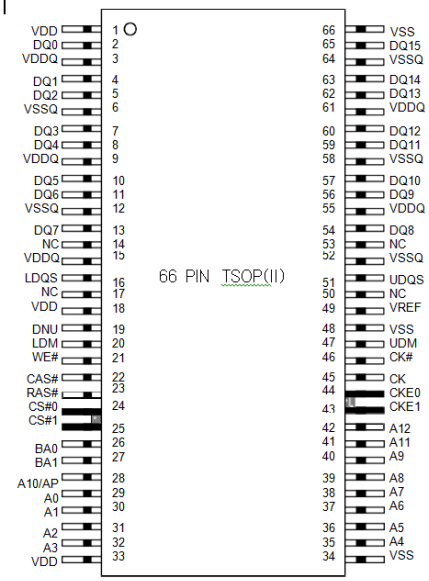
Introduction

The 1 Gbit DDR is made by stacking two 512 Mbit, double-data-rate synchronous dynamic RAM TSOP ICs. Stacking provides a generational advance in density in the same footprint as the current generation IC. The DDR SDRAM uses double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2n-bit-wide, one-clock-cycle data transfer at the internal DRAM core, and two corresponding n-bit-wide, one-half clock-cycle data transfer at the I/O pins.

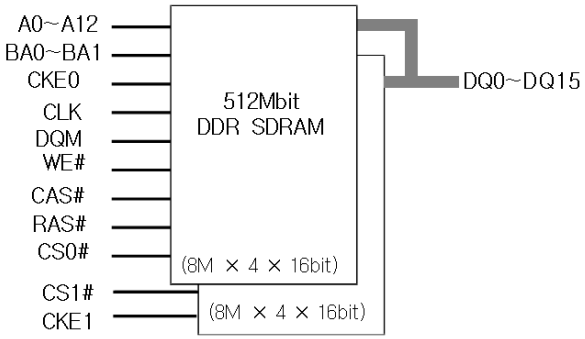
I/O transfers occur on both edges of the bi-directional data strobe DQS. This doubles the maximum data rate possible with single data rate SDRAM devices. The DQS is edge-aligned for reads and is center-aligned for writes. Since the DQS always travels with the data, clocking skew due to loading and flight time is minimized. A separate differential CK /CK# pair provides clocking for the address and most control lines.

All inputs are compatible with the JEDEC Standard for SSTL_2. All full-drive options outputs are SSTL_2, Class II compatible.

PIN CONFIGURATION
(Top view)

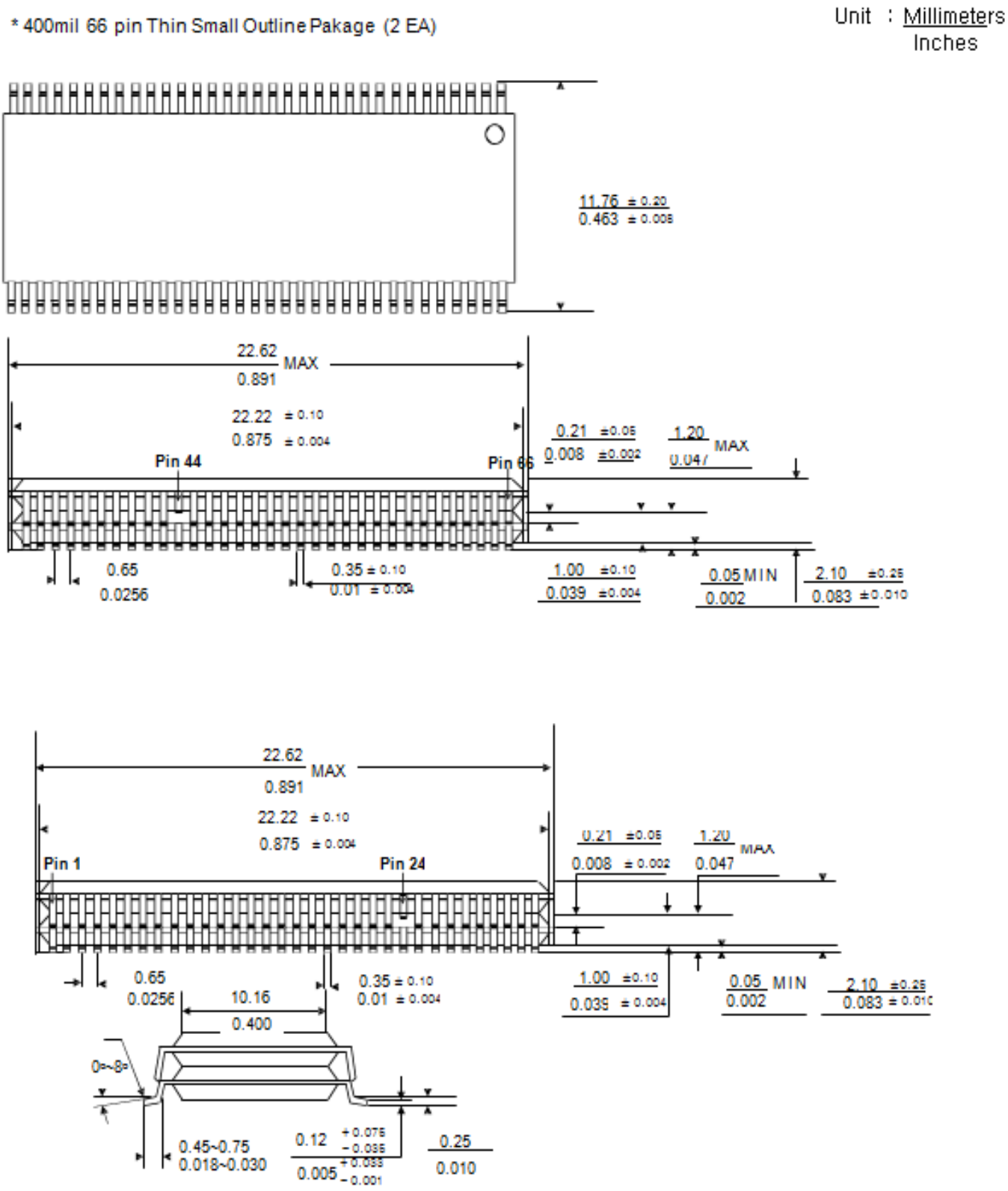


FUNCTIONAL BLOCK DIAGRAM



Mechanical Drawing

Stacked Package Mechanical Specification



3. Ordering Information

This product is available in Industrial temperature version.

Table 4-1. Ordering Information (1)(3)

EV(X)(4)	**S**	**32M16**	**T**	**- 5B**	**I**
	Stacked Package	Configuration	Package Type	Speed Grade	Operating Temperature Range
e2v Prefix	S	32M16 32 Meg x 16	T = TSOPII(2)	-5B T_{CK}= 5ns, CL=3	I = –40 to 85°C

Notes:
1. For availability of the different versions, contact your local e2v sales office.
2. Lead finish: eutectic SnPb
3. These products are classified preliminary until the completion of all qualification tests. The specifications in this datasheet are intended to be final but are subject to change.
4. The letter X in the part number designates a “Prototype” product that has not been qualified by e2v. Reliability of an EVX part number is not guaranteed and such part number shall not be used in Flight Hardware.

5. Document Revision History

Table 5-1 provides a revision history for this hardware specification.

Table 5-1. Document Revision History

Rev. No	**Date**	**Substantive Change(s)**
1	4/14/2015	Initial revision

Visit our website at www.e2v-us.com for the latest version of the datasheet.