REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Pages 1, 2, 3, 4, 14, 15, 16, editorial changes. Pages 5, 6, 7, 8, symbol corrections. Page 18, added vendor.	81-12-09	M. A. Frye
B	Add device type 03. Type 02 inactive for new design: Use MIL-M-38510/52002 for case Q. Type 01 and new type 03 are still active.	83-04-06	M. A. Frye
C	Add device types 04 and 05.	84-10-31	M. A. Frye
D	Case temperature to +125°C. Add LCC package, electrical test improvements.	85-11-12	M. A. Frye
E	Change to military drawing format. Add device type 06, changes to 1.4, add vendor CAGE number 66958, delete vendor CAGE number 34335, changes to table I, changes to figures 1, 2, and 3. Editorial changes throughout. Change Code Ident. No. to 67268.	87-12-17	M. A. Frye
F	Update boilerplate to MIL-PRF-38535 requirements. Correct drawing title to indicate device function. - CFS	03-06-11	Thomas M. Hess
G	Correct marking requirements in 3.5. Update boilerplate in accordance with MIL-PRF-38535 requirements. - PHN.	05-03-23	Thomas M. Hess
H	Add device type 06 to case outlines X and Q in figure 2. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	12-12-19	Thomas M. Hess
J	Correct the circuit function 16 bit instead of 6 bit in the title. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - MAA	14-08-07	Thomas M. Hess

REV																				
SHEET																				
REV	J	J	J	J	J	J	J	J	J	J	J	J								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								

REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Ray Monnin	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles Reusing APPROVED BY Michael. A. Frye DRAWING APPROVAL DATE 80-07-21 REVISION LEVEL J	MICROCIRCUIT, DIGITAL, 16-BIT N-CHANNEL SINGLE-CHIP MICROPROCESSOR, MONOLITHIC SILICON SIZE A CAGE CODE **67268** **80003** SHEET 1 OF 26

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

80003	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	Z8001	4.0 MHz	16-Bit N-channel single-chip microprocessor
02	Z8002	4.0 MHz	16-Bit N-channel single-chip microprocessor
03	Z8001A	6.0 MHz	16-Bit N-channel single-chip microprocessor
04	Z8001B	10.0 MHz	16-Bit N-channel single-chip microprocessor
05	Z8002B	10.0 MHz	16-Bit N-channel single-chip microprocessor
06	Z8002A	6.0 MHz	16-Bit N-channel single-chip microprocessor

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
U	CQCC1-N52	52	Square leadless chip carrier
X	See figure 1	48	Dual-in-line
Y	CQCC1-N44	44	Square leadless chip carrier
Z	CQCC1-N68	68	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range with respect to ground (V_{CC}) ..... -0.3 V dc to +7.0 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) (per device) ..... 2.2 W
Lead temperature (soldering, 5 seconds) ..... +270°C
Maximum junction temperature (T_J) ..... +150°C
Thermal resistance, junction-to-case (θ_{JC}):
Case X ..... 14°C/W
Cases Q, U, Y, Z ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}):	
Logic inputs	+2.2 V dc to V_{CC} + 0.3 V dc
Clock input	V_{CC} – 0.4 V dc to V_{CC} + 0.3 V dc
RESET (NMI)	2.4 V dc to V_{CC} + 0.3 V dc
Maximum low level input voltage (V_{IL}):	
Logic inputs	-0.3 V dc to +0.8 V dc
Clock input	-0.3 V dc to +0.45 V dc
Frequency of operation:	
01, 02	0.5 MHz to 4.0 MHz
03, 06	0.5 MHz to 6.0 MHz
04, 05	0.5 MHz to 10.0 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Clock rise time (t_r):	
01, 02	20 ns maximum
03, 06	15 ns maximum
04, 05	10 ns maximum
Clock fall time (t_f):	
01, 02	20 ns maximum
03, 06	10 ns maximum
04, 05	15 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic functions. The logic functions shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock input low voltage	V_{IL1}	Driven by external clock generator.	1, 2, 3	All	-0.3 1/	0.45	V
Clock input high voltage	V_{IH1}		1, 2, 3	All	V_{CC} – 0.4	V_{CC} + 0.3 1/	V
Input low voltage	V_{IL2}		1, 2, 3	All	-0.3 1/	0.8	V
Input high voltage	V_{IH2}		1, 2, 3	All	2.4	V_{CC} + 0.3 1/	V
Reset input high voltage ($\overline{NMI}$)	V_{IH3}		1, 2, 3	All	2.4	V_{CC} + 0.3 1/	V
High level output voltage all outputs	V_{OH}	I_{OH} = -250 µA V_{CC} = 4.5 V	1, 2, 3	All	2.4		V
Low level output voltage all outputs	V_{OL}	I_{OL} = +2.0 mA V_{CC} = 4.5 V	1, 2, 3	All		0.4	V
High-impedance (off-state) output current (High) (In Float)	I_{ZH}	V_{IN} = 2.4 V V_{CC} = 5.5 V	1, 2, 3	All	–10	+10	µA
High-impedance (off-state) output current (Low) (In Float)	I_{ZL}	V_{IN} = 0.4 V V_{CC} = 5.5 V	1, 2, 3	All	–10	+10	µA
High level input current (input and bi-directional)	I_{IH}	V_{IN} = 2.4 V V_{CC} = 5.5 V	1, 2, 3	All	-10	+10	µA
Low level input current (input and bi-directional)	I_{IL}	V_{IN} = 0.4 V V_{CC} = 5.5 V	1, 2, 3	All	-10	+10	µA
Low level input current ($\overline{SEGT}$)	I_{ILS}	$0.4\ V \le V_{IN} \le 2.4\ V$ $4.5\ V \le V_{CC} \le 5.5\ V$	1, 2, 3	01, 03, 04		+200	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	All		400	mA
Functional tests		See 4.3.1c	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock pulse	t_{cyc}	See figure 4. See Reference No. 1 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	250	2000	ns
				03, 06	165	2000	
				04, 05	100	2000	
Clock pulse width (Low)	t_{PWL1}	See figure 4. See Reference No. 2 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	105		ns
				03, 06	70		
				04, 05	40		
Clock pulse width (High)	t_{PWH1}	See figure 4. See Reference No. 3 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	105		ns
				03, 06	70		
				04, 05	40		
Clock ↑ to segment number valid	TdC(SNv) 3/ 4/	See figure 4. See Reference No. 6 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01		130	ns
				03		110	
				04		90	
Clock ↑ to segment number not valid	TdC(SNn) 4/	See figure 4. See Reference No. 7 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01	20		ns
				03	10		
				04	0		
Clock ↑ to bus float	TdC(Bz) 1/	See figure 4. See Reference No. 8 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		65	ns
				03, 06		55	
				04, 05		50	
Clock ↑ to address valid	TdC(A)	See figure 4. See Reference No. 9 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		100	ns
				03, 06		75	
				04, 05		65	
Clock ↑ to address float	TdC(Az) 1/	See figure 4. See Reference No. 10 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		65	ns
				03, 06		55	
				04, 05		50	
Address valid to data in required valid	TdA(DR)	See figure 4. See Reference No. 11 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02		475	ns
				03, 06		305	
				04, 05		180	
Data to CLK ↓ setup time	TsDR(C)	See figure 4. See Reference No. 12 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	30		ns
				03, 06	20		
				04, 05	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{DS}$ ↑ to address active	TdDS(A)	See figure 4. See Reference No. 13 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	80		ns
				03, 06	45		
				04, 05	20		
Clock ↑ to data out valid	TdC(DW)	See figure 4. See Reference No. 14 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		100	ns
				03, 06		75	
				04, 05		60	
Data in to $\overline{DS}$ ↑ hold time	ThDR(DS)	See figure 4. See Reference No. 15 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	0		ns
				03, 06	0		
				04, 05	0		
Data out valid to $\overline{DS}$ ↑ delay	TdDW(DS)	See figure 4. See Reference No. 16 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	295		ns
				03, 06	195		
				04, 05	110		
Address valid to $\overline{MREQ}$ ↓ delay	TdA(MR)	See figure 4. See Reference No. 17 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	55		ns
				03, 06	35		
				04, 05	20		
Clock ↓ to $\overline{MREQ}$ ↓ delay	TdC(MR)	See figure 4. See Reference No. 18 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		80	ns
				03, 06		70	
				04, 05		50	
$\overline{MREQ}$ width (High)	TwMRh	See figure 4. See Reference No. 19 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	210		ns
				03, 06	135		
				04, 05	80		
$\overline{MREQ}$ ↓ to address not active	TdMR(A) 1/	See figure 4. See Reference No. 20 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	70		ns
				03, 06	35		
				04, 05	15		
Data out valid to $\overline{DS}$ ↓ (Write Delay)	TdDW (DSW)	See figure 4. See Reference No. 21 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	55		ns
				03, 06	35		
				04, 05	15		
$\overline{MREQ}$ ↓ to data in required valid	TdMR(DR)	See figure 4. See Reference No. 22 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02		370	ns
				03, 06		230	
				04, 05		140	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock ↓ to $\overline{\text{MREQ}}$ ↑ delay	TdC(MR)	See figure 4. See Reference No. 23 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		80	ns
				03, 06		60	
				04, 05		50	
Clock ↑ to $\overline{\text{AS}}$ ↓ delay	TdC(ASf)	See figure 4. See Reference No. 24 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		80	ns
				03, 06		60	
				04, 05		45	
Address valid to $\overline{\text{AS}}$ ↑ delay	TdA(AS)	See figure 4. See Reference No. 25 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	55		ns
				03, 06	35		
				04, 05	20		
Clock ↓ to $\overline{\text{AS}}$ ↑ delay	TdC(ASr)	See figure 4. See Reference No. 26 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		90	ns
				03, 06		80	
				04, 05		45	
$\overline{\text{AS}}$ ↑ to data in required valid	TdAS(DR)	See figure 4. See Reference No. 27 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02		360	ns
				03, 06		220	
				04, 05		140	
$\overline{\text{DS}}$ ↑ to $\overline{\text{AS}}$ ↓ delay	TdDS(AS)	See figure 4. See Reference No. 28 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	70		ns
				03, 06	35		
				04, 05	15		
$\overline{\text{AS}}$ width (Low)	TwAS	See figure 4. See Reference No. 29 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	85		ns
				03, 06	55		
				04, 05	30		
$\overline{\text{AS}}$ ↑ to address not active delay	TdAS(A) 1/	See figure 4. See Reference No. 30 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	70		ns
				03, 06	45		
				04, 05	15		
Address float to $\overline{\text{DS}}$ (Read) ↓ delay	TdAz(DSR) 1/	See figure 4. See Reference No. 31 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	0		ns
				03, 06	0		
				04, 05	0		
$\overline{\text{AS}}$ ↑ to $\overline{\text{DS}}$ ↓ (Read) delay	TdAS(DSR)	See figure 4. See Reference No. 32 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	80		ns
				03, 06	55		
				04, 05	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{DS}$ (Read) ↓ to data in required valid	TdDSR(DR)	See figure 4. See Reference No. 33 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02		205	ns
				03, 06		130	
				04, 05		70	
Clock ↓ to $\overline{DS}$ ↑ delay	TdC(DSr)	See figure 4. See Reference No. 34 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		70	ns
				03, 06		65	
				04, 05		50	
$\overline{DS}$ ↑ to data out not valid	TdDS(DW) 1/	See figure 4. See Reference No. 35 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	75		ns
				03, 06	45		
				04, 05	25		
Address valid to $\overline{DS}$ (Read) ↓ delay	TdA(DSR)	See figure 4. See Reference No. 36 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	180		ns
				03, 06	110		
				04, 05	65		
Clock ↑ to $\overline{DS}$ (Read) ↓ delay	TdC(DSR)	See figure 4. See Reference No. 37 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		120	ns
				03, 06		85	
				04, 05		65	
$\overline{DS}$ (Read) width (Low)	TwDSR	See figure 4. See Reference No. 38 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	275		ns
				03, 06	185		
				04, 05	110		
Clock ↓ to $\overline{DS}$ (Write) ↓ delay	TdC(DSW)	See figure 4. See Reference No. 39 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		95	ns
				03, 06		80	
				04, 05		65	
$\overline{DS}$ (Write) width (Low)	TwDSW	See figure 4. See Reference No. 40 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	185		ns
				03, 06	110		
				04, 05	75		
$\overline{DS}$ (Input) ↓ to data in required valid	TdDSI(DR)	See figure 4. See Reference No. 41 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02		330	ns
				03, 06		210	
				04, 05		120	
Clock ↓ to $\overline{DS}$ (I_O) ↓ delay	TdC(DSf)	See figure 4. See Reference No. 42 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		120	ns
				03, 06		90	
				04, 05		70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{DS}$ (I/O) width (Low)	TwDS	See figure 4. See Reference No. 43 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	410		ns
				03, 06	255		
				04, 05	160		
$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ delay	TdAS(DSA)	See figure 4. See Reference No. 44 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	1065		ns
				03, 06	690		
				04, 05	410		
Clock ↑ to $\overline{DS}$ (Acknowledge) ↓ delay	TdC(DSA)	See figure 4. See Reference No. 45 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		120	ns
				03, 06		85	
				04, 05		70	
$\overline{DS}$ (Acknowledge) ↓ to data in required delay	TdDSA(DR)	See figure 4. See Reference No. 46 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02		455	ns
				03, 06		295	
				04, 05		165	
Clock ↑ to status valid delay	TdC(S)	See figure 4. See Reference No. 47 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		110	ns
				03, 06		85	
				04, 05		65	
Status valid to $\overline{AS}$ ↑ delay	TdS(AS)	See figure 4. See Reference No. 48 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	50		ns
				03, 06	30		
				04, 05	10		
$\overline{RESET}$ to clock ↑ set-up time	TsR(C)	See figure 4. See Reference No. 49 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	180		ns
				03, 06	70		
				04, 05	50		
$\overline{RESET}$ to clock ↑ hold time	ThR(C)	See figure 4. See Reference No. 50 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	0		ns
				03, 06	0		
				04, 05	0		
$\overline{NMI}$ width (Low)	TwNMI	See figure 4. See Reference No. 51 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	100		ns
				03, 06	70		
				04, 05	50		
$\overline{NMI}$ to clock ↑ set-up time	TsNMI(C)	See figure 4. See Reference No. 52 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	140		ns
				03, 06	70		
				04, 05	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{VI}$, $\overline{NVI}$ to clock ↑ set-up time	TsVI(C)	See figure 4. See Reference No. 53 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	110		ns
				03, 06	50		
				04, 05	40		
$\overline{VI}$, $\overline{NVI}$ to clock ↑ hold time	ThVI(C)	See figure 4. See Reference No. 54 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	20		ns
				03, 06	20		
				04, 05	10		
$\overline{SEGT}$ to clock ↑ set-up time	TsSGT(C) 4/	See figure 4. See Reference No. 55 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01	70		ns
				03	55		
				04	40		
$\overline{SEGT}$ to clock ↑ hold time	ThSGT(C) 4/	See figure 4. See Reference No. 56 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01	0		ns
				03	0		
				04	0		
$\overline{MI}$ to clock ↑ set-up time	TsMI(C)	See figure 4. See Reference No. 57 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	180		ns
				03, 06	140		
				04, 05	80		
$\overline{MI}$ to clock ↑ hold time	ThMI(C)	See figure 4. See Reference No. 58 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	0		ns
				03, 06	0		
				04, 05	0		
Clock ↑ to $\overline{MO}$ delay time	TdC(MO)	See figure 4. See Reference No. 59 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		120	ns
				03, 06		85	
				04, 05		80	
$\overline{STOP}$ to clock ↓ set-up time	TsSTP(C)	See figure 4. See Reference No. 60 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	140		ns
				03, 06	100		
				04, 05	50		
$\overline{STOP}$ to clock ↓ hold time	ThSTP(C)	See figure 4. See Reference No. 61 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	0		ns
				03, 06	0		
				04, 05	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{WAIT}$ to clock ↓ set-up time	TsW(C)	See figure 4. See Reference No. 62 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	50		ns
				03, 06	30		
				04, 05	20		
$\overline{WAIT}$ to clock ↓ hold time	ThW(C)	See figure 4. See Reference No. 63 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	10		ns
				03, 06	10		
				04, 05	5		
$\overline{BUSRQ}$ to clock ↑ set-up time	TsBRQ(C)	See figure 4. See Reference No. 64 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	90		ns
				03, 06	80		
				04, 05	60		
$\overline{BUSRQ}$ to clock ↑ hold time	ThBRQ(C)	See figure 4. See Reference No. 65 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02	10		ns
				03, 06	10		
				04, 05	5		
Clock ↑ to $\overline{BUSAK}$ ↑ delay	TdC(BAKr)	See figure 4. See Reference No. 66 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		100	ns
				03, 06		75	
				04, 05		65	
Clock ↑ to $\overline{BUSAK}$ ↓ delay	TdC(BAKf)	See figure 4. See Reference No. 67 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11	01, 02		100	ns
				03, 06		75	
				04, 05		65	
Address valid width	TwA	See figure 4. See Reference No. 68 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	150		ns
				03, 06	95		
				04, 05	50		
$\overline{DS}$ ↑ to status not valid	TdDS(s) 1/	See figure 4. See Reference No. 69 2/ C_L = 50 pF to 100 pF ±10%, all outputs	9, 10, 11 5/	01, 02	80		ns
				03, 06	55		
				04, 05	30		

See footnotes on next sheet.

1/ Guaranteed, if not tested.

2/ The waveform reference number refers to the position where the parameter appears on figure 4.

3/ For waveform reference number 6, C_L = 50 pF ±10%.

4/ These parameters are for 01, 03, and 04 devices only.

5/ These waveform reference number parameters are clock dependent. The limits provided are at F_{MAX}. To determine the limits at other frequencies use the following equations:

Waveform reference number	Device types 01 and 02	Device types 03 and 06	Device types 04 and 05
11	$2\ t_{cyc} + t_{PWH1} - 130$ ns	$2\ t_{cyc} + t_{PWH1} - 95$ ns	$2\ t_{cyc} + t_{PWH1} - 60$ ns
13	$t_{PWL1} - 25$ ns	$t_{PWL1} - 25$ ns	$t_{PWL1} - 20$ ns
16	$t_{cyc} + t_{PWH1} - 60$ ns	$t_{cyc} + t_{PWH1} - 40$ ns	$t_{cyc} + t_{PWH1} - 30$ ns
17	$t_{PWH1} - 50$ ns	$t_{PWH1} - 35$ ns	$t_{PWH1} - 20$ ns
19	$t_{cyc} - 40$ ns	$t_{cyc} - 30$ ns	$t_{cyc} - 20$ ns
20	$t_{PWL1} - 35$ ns	$t_{PWL1} - 35$ ns	$t_{PWL1} - 20$ ns
21	$t_{PWH1} - 50$ ns	$t_{PWH1} - 35$ ns	$t_{PWH1} - 25$ ns
22	$2\ t_{cyc} - 130$ ns	$2\ t_{cyc} - 100$ ns	$2\ t_{cyc} - 60$ ns
25	$t_{PWH1} - 50$ ns	$t_{PWH1} - 35$ ns	$t_{PWH1} - 20$ ns
27	$2\ t_{cyc} - 140$ ns	$2\ t_{cyc} - 110$ ns	$2\ t_{cyc} - 60$ ns
28	$t_{PWL1} - 35$ ns	$t_{PWL1} - 35$ ns	$t_{PWL1} - 25$ ns
29	$t_{PWH1} - 20$ ns	$t_{PWH1} - 15$ ns	$t_{PWH1} - 10$ ns
30	$t_{PWL1} - 35$ ns	$t_{PWL1} - 25$ ns	$t_{PWL1} - 20$ ns
32	$t_{PWL1} - 25$ ns	$t_{PWL1} - 15$ ns	$t_{PWL1} - 10$ ns
33	$t_{cyc} + t_{PWH1} - 150$ ns	$t_{cyc} + t_{PWH1} - 105$ ns	$t_{cyc} + t_{PWH1} - 70$ ns
35	$t_{PWL1} - 30$ ns	$t_{PWL1} - 25$ ns	$t_{PWL1} - 15$ ns
36	$t_{cyc} - 70$ ns	$t_{cyc} - 55$ ns	$t_{cyc} - 35$ ns
38	$t_{cyc} + t_{PWH1} - 80$ ns	$t_{cyc} + t_{PWH1} - 50$ ns	$t_{cyc} + t_{PWH1} - 30$ ns
40	$t_{cyc} - 65$ ns	$t_{cyc} - 55$ ns	$t_{cyc} - 25$ ns
41	$2\ t_{cyc} - 170$ ns	$2\ t_{cyc} - 120$ ns	$2\ t_{cyc} - 80$ ns
43	$2\ t_{cyc} - 90$ ns	$2\ t_{cyc} - 75$ ns	$2\ t_{cyc} - 40$ ns
44	$4\ t_{cyc} + t_{PWL1} - 40$ ns	$4\ t_{cyc} + t_{PWL1} - 40$ ns	$4\ t_{cyc} + t_{PWL1} - 30$ ns
46	$2\ t_{cyc} + t_{PWH1} - 150$ ns	$2\ t_{cyc} + t_{PWH1} - 105$ ns	$2\ t_{cyc} + t_{PWH1} - 75$ ns
48	$t_{PWH1} - 55$ ns	$t_{PWH1} - 40$ ns	$t_{PWH1} - 30$ ns
68	$t_{cyc} - 90$ ns	$t_{cyc} - 70$ ns	$t_{cyc} - 50$ ns
69	$t_{PWL1} - 25$ ns	$t_{PWL1} - 15$ ns	$t_{PWL1} - 10$ ns

Case Outline X

Device types 01, 03, and 04.

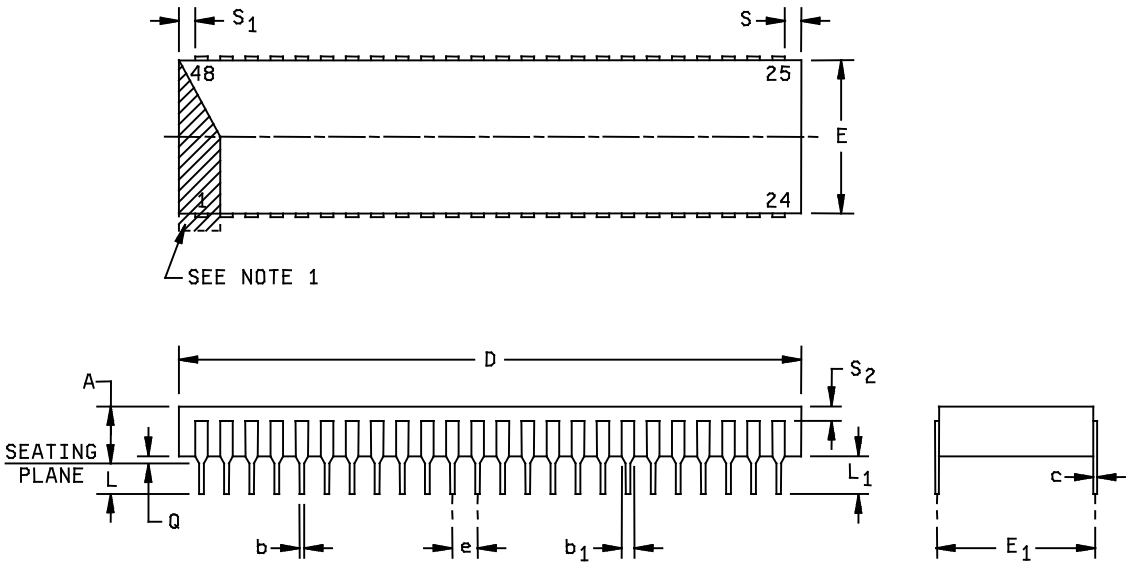

FIGURE 1. Case outlines.

Case Outline X

Device types 01, 03, and 04.

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	---	.225	---	5.72	
b	.014	.023	0.36	0.58	7
b_1	.030	.070	0.76	1.78	2, 7
c	.008	.015	0.20	0.38	7
D	---	2.480	---	62.99	
E	.510	.620	12.95	15.75	
E_1	.520	.620	13.21	15.75	6
e	.100 BSC		2.54 BSC		4, 8
L	.120	.200	3.05	5.08	
L_1	.150	---	3.81	---	
Q	.020	.060	0.51	1.52	3
S	---	.098	---	2.40	5
S_1	.005	---	0.13	---	5
S_2	.005	---	0.13	---	9

Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .020 (0.51 mm) for leads number 1, 24, 25, and 48 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within $\pm$.010 (0.25 mm) of its exact longitudinal position relative to pins 1 and 48.
5. Applies to all four corners (leads number 1, 24, 25, and 48) (see MIL-STD-1835).
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
8. Forty-six spaces.
9. The top of the lead shall not exceed above the brazed pad top surface.

FIGURE 1. Case outlines - Continued.

Case outlines X and Q

Device types: 01, 03, and 04			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AD_0	25	SN_1
2	AD_9	26	$\overline{SN_0}$
3	AD_{10}	27	$\overline{BUSRQ}$
4	AD_{11}	28	$\overline{WAIT}$
5	AD_{12}	29	BUSAK
6	$\overline{AD_{13}}$	30	$R/\overline{W}$
7	STOP	31	N/S
8	$\overline{MI}$	32	$B/\overline{W}$
9	AD_{15}	33	NC
10	AD_{14}	34	$\overline{AS}$
11	V_{CC}	35	CLOCK
12	$\overline{VI}$	36	GND
13	$\overline{NVI}$	37	SN_2
14	$\overline{SEGT}$	38	AD_1
15	$\overline{NMI}$	39	AD_2
16	$\overline{RESET}$	40	AD_3
17	$\overline{M_O}$	41	AD_5
18	$\overline{MREQ}$	42	SN_4
19	DS	43	AD_4
20	ST_3	44	AD_6
21	ST_2	45	AD_7
22	ST_1	46	SN_5
23	ST_0	47	SN_6
24	SN_3	48	AD_8

Device types: 02, 05, and 06			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AD_9	21	$\overline{ST_0}$
2	AD_{10}	22	$\overline{BUSRQ}$
3	AD_{11}	23	$\overline{WAIT}$
4	AD_{12}	24	$\overline{BUSAK}$
5	$\overline{AD_{13}}$	25	$R/\overline{W}$
6	$\overline{STOP}$	26	$\overline{N/S}$
7	M_I	27	B/W
8	AD_{15}	28	$\overline{NC}$
9	AD_{14}	29	AS
10	V_{CC}	30	CLOCK
11	$\overline{VI}$	31	GND
12	$\overline{NVI}$	32	AD_1
13	$\overline{NMI}$	33	AD_2
14	$\overline{RESET}$	34	AD_3
15	$\overline{M_O}$	35	AD_5
16	$\overline{MREQ}$	36	AD_4
17	DS	37	AD_6
18	ST_3	38	AD_7
19	ST_2	39	AD_8
20	ST_1	40	AD_0

NC = No internal connection.

FIGURE 2. Terminal connections.

Case outline U

Device types: 01, 03, and 04			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AD_0	27	SN_1
2	AD_9	28	$\overline{SN_0}$
3	AD_{10}	29	$\overline{BUSRQ}$
4	AD_{11}	30	$\overline{WAIT}$
5	AD_{12}	31	BUSAK
6	AD_{13}	32	NC
7	$\overline{NC}$	33	$\overline{NC}$
8	$\overline{STOP}$	34	$R/\overline{W}$
9	$\overline{M_I}$	35	$N/\overline{S}$
10	AD_{15}	36	$B/\overline{W}$
11	AD_{14}	37	RESERVED
12	V_{CC}	38	$\overline{AS}$
13	$\overline{NC}$	39	CLK
14	$\overline{VI}$	40	GND
15	$\overline{NVI}$	41	SN_2
16	$\overline{SEGT}$	42	AD_1
17	$\overline{NMI}$	43	AD_2
18	$\overline{RESET}$	44	AD_3
19	$\overline{M_O}$	45	AD_5
20	$\overline{MREQ}$	46	SN_4
21	DS	47	AD_4
22	ST_3	48	AD_6
23	ST_2	49	AD_7
24	ST_1	50	SN_5
25	ST_0	51	SN_6
26	SN_3	52	AD_8

NC = No internal connection.

FIGURE 2. Terminal connections - Continued.

Case outline Z

Device types: 01, 03, and 04			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	35	SN_1
2	+5V	36	$\overline{SN_0}$
3	AD_0	37	$\overline{BUSRQ}$
4	AD_9	38	$\overline{WAIT}$
5	AD_{10}	39	$\overline{BUSAK}$
6	AD_{11}	40	NC
7	AD_{12}	41	NC
8	AD_{13}	42	NC
9	NC	43	NC
10	NC	44	NC
11	$\overline{STOP}$	45	$R/\overline{W}$
12	$\overline{M_I}$	46	$N/\overline{S}$
13	AD_{15}	47	$B/\overline{W}$
14	AD_{14}	48	RESERVED
15	+5V	49	$\overline{AS}$
16	+5V	50	GND
17	GND	51	CLK
18	GND	52	+5V
19	$\overline{VI}$	53	GND
20	$\overline{NVI}$	54	SN_2
21	$\overline{SEGT}$	55	AD_1
22	$\overline{NMI}$	56	AD_2
23	$\overline{RESET}$	57	AD_3
24	$\overline{M_O}$	58	AD_5
25	$\overline{MREQ}$	59	SN_4
26	NC	60	NC
27	NC	61	NC
28	NC	62	NC
29	$\overline{DS}$	63	AD_4
30	ST_3	64	AD_6
31	ST_2	65	AD_7
32	ST_1	66	SN_5
33	ST_0	67	SN_6
34	SN_3	68	AD_8

NC = No internal connection.

FIGURE 2. Terminal connections - Continued.

Case outline Y

Device types: 02, 05, and 06			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AD_9	23	ST_0
2	AD_{10}	24	NC
3	AD_{11}	25	$\overline{NC}$
4	AD_{12}	26	$\overline{BUSRQ}$
5	AD_{13}	27	$\overline{WAIT}$
6	$\overline{NC}$	28	BUSAK
7	STOP	29	R/$\overline{W}$
8	$\overline{M_I}$	30	N/$\overline{S}$
9	AD_{15}	31	B/$\overline{W}$
10	AD_{14}	32	RESERVED
11	V_{CC}	33	$\overline{AS}$
12	$\overline{NC}$	34	CLK
13	$\overline{VI}$	35	GND
14	$\overline{NVI}$	36	AD_1
15	$\overline{NMI}$	37	AD_2
16	$\overline{RESET}$	38	AD_3
17	$\overline{M_O}$	39	AD_5
18	MREQ	40	AD_4
19	$\overline{DS}$	41	AD_6
20	ST_3	42	AD_7
21	ST_2	43	AD_8
22	ST_1	44	AD_0

NC = No internal connection.

FIGURE 2. Terminal connections - Continued.

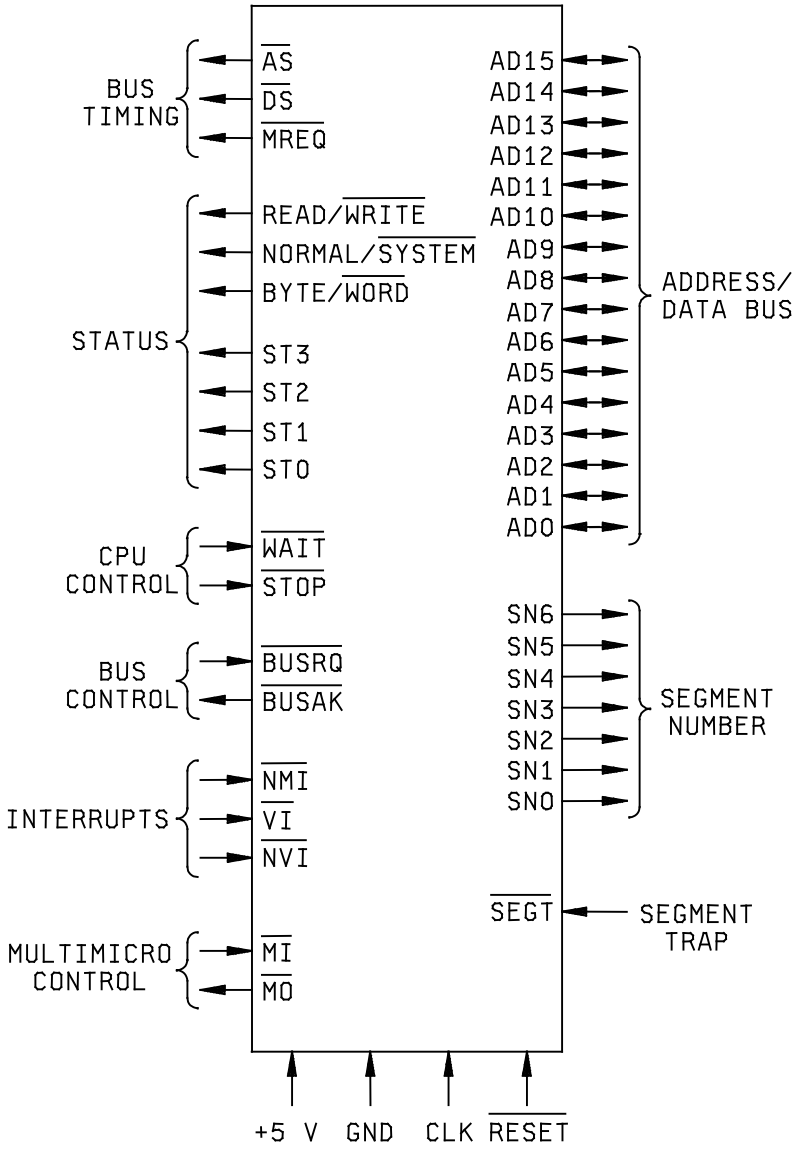

FIGURE 3. Logic functions.

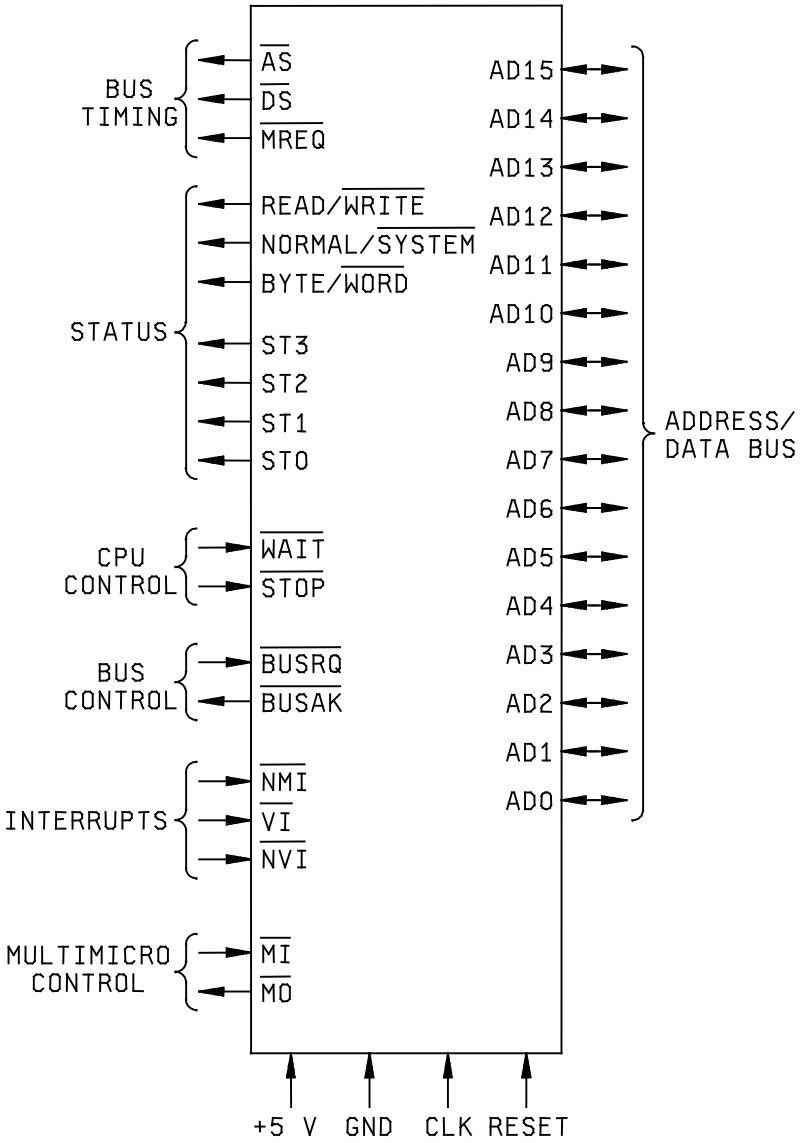

FIGURE 3. Logic functions - Continued.

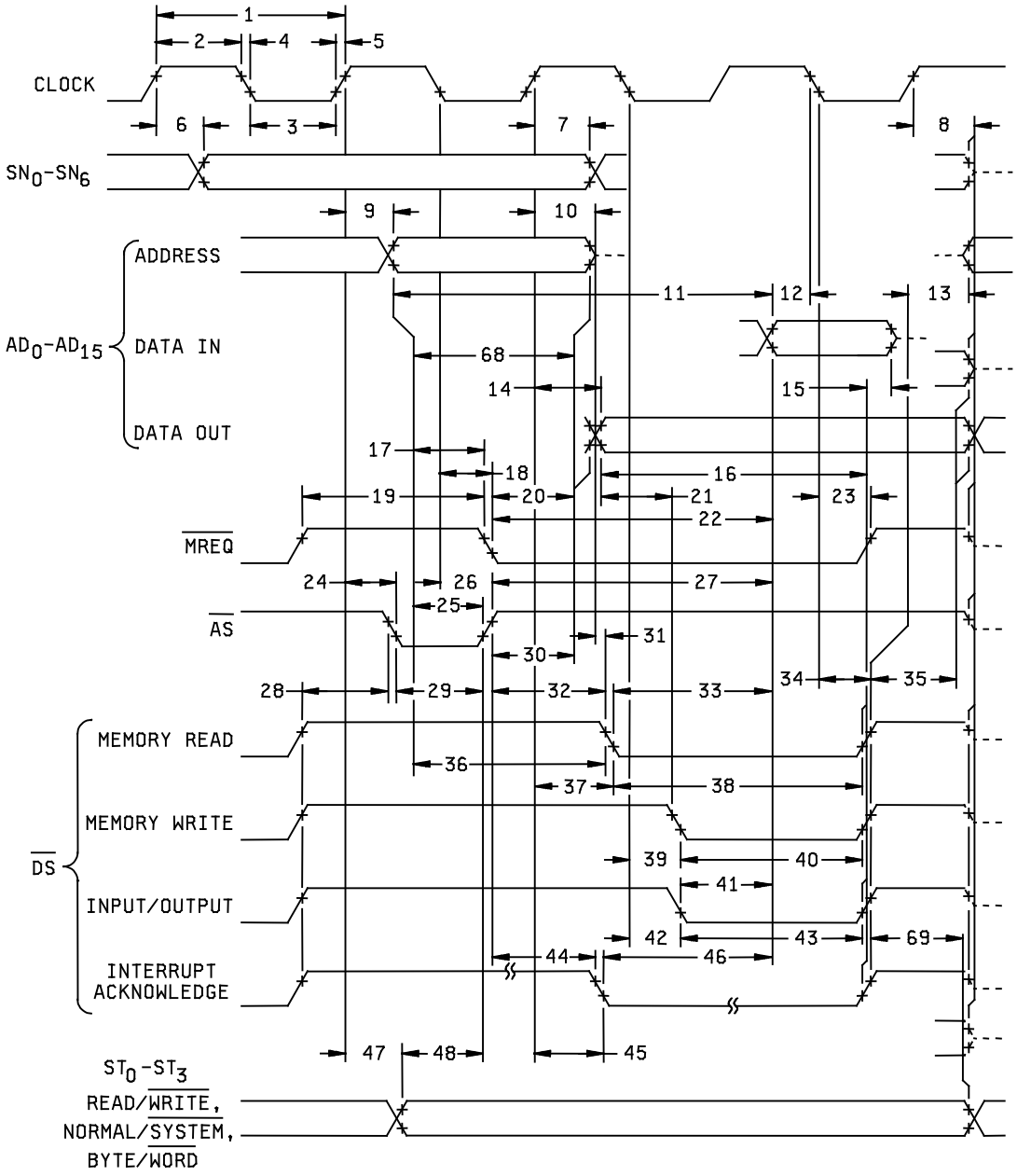

FIGURE 4. Timing waveforms.

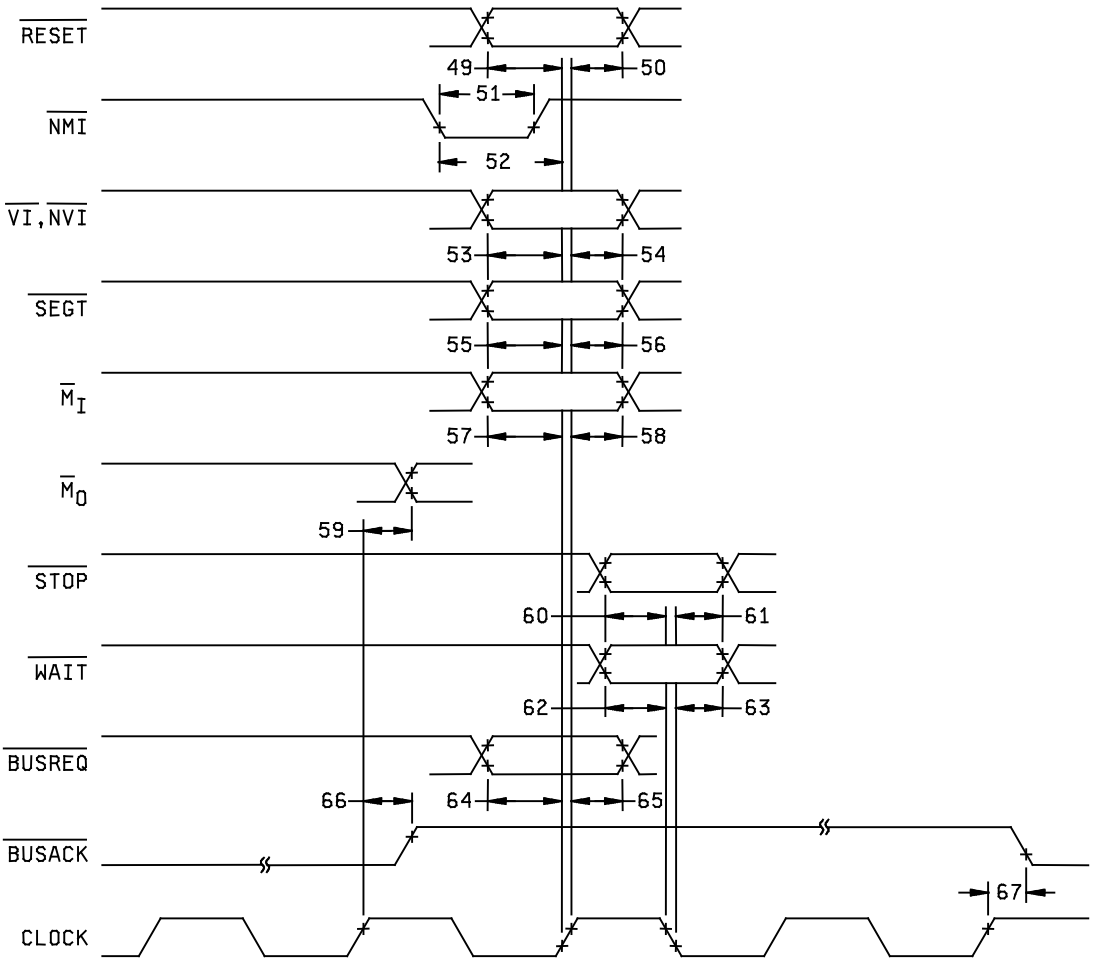

FIGURE 4. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the functionality of the device. It forms a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Pin descriptions.

Name	Description
$AD_0 – AD_{15}$ (Address/Data Bus)	Inputs/outputs, active High, three-state. These multiplexed address and data used for both I/O and to address memory. AD_{15} = MSB.
$\overline{AS}$ (Address Strobe)	Output, active Low, three-state. The rising edge of $\overline{AS}$ indicates addresses are valid.
$\overline{BUSAK}$ (Bus Acknowledge)	Output, active Low. A low on this line indicates the CPU has relinquished control of the bus. This occurs after completion of the current machine cycle. BUSAK goes inactive one clock cycle after the synchronization of $\overline{BUSRQ}$ being released.
$\overline{BUSRQ}$ (Bus Request)	Input, active Low. This line must be driven Low to request the bus from the CPU. sampled for being active at the beginning of each machine cycle. When it is released, it is synchronized with the next rising clock edge.

6.7 Pin descriptions - Continued.

Name	Description
$\overline{DS}$ (Data Strobe)	Output, active Low, three-state. This line times the data in and out of the CPU.
$\overline{MREQ}$ (Memory Request)	Output, active Low, three-state. A low on this line indicates that the address/data bus holds a memory address.
$\overline{MI}$, $\overline{MO}$ (Multi-Micro In, Multi-Micro Out)	Input and output, active Low. These two lines form a resource-request daisy chain that allows one CPU in a multi-microprocessor system to access a shared resource. $\overline{MI}$ is sampled on the rising edge of T_3 of the last machine cycle of any instruction and Internally latched.
$\overline{NMI}$ (Non-Maskable Interrupt)	Edge triggered, input, active Low. A high-to-low transition on $\overline{NMI}$ request a non-maskable interrupt. The NMI interrupt has the highest priority of the three types of interrupts. The internal $\overline{NMI}$ latch is sampled on the rising edge of T_3 of the last machine cycle of any instruction.
$\overline{NVI}$ (Non-Vectored Interrupt)	Input, active Low. A low on this line requests a non-vectored interrupt. It is sampled on the rising edge of T_3 of the last machine cycle of any instruction.
CLK (System Clock)	Input. CLK is a 5 V single-phase time-base input.
$\overline{RESET}$ (Reset)	Input, active Low. A low on this line resets the CPU. $\overline{RESET}$ must be active for at least five clock cycles.
R/$\overline{W}$ (Read/Write)	Output, Low = Write, three-state. R/W indicates that the CPU is reading from or writing to memory or I/O.
$ST_0 – ST_3$ (Status)	Outputs, active High, three-state. These lines specify the CPU status.
$\overline{STOP}$ (Stop)	Input, active Low. This input can be used to single-step instruction execution. It is sampled on the last falling clock edge preceding any first instruction fetch cycle.
$\overline{VI}$ (Vectored Interrupt)	Input, active Low. A low on this line requests a vectored interrupt. It is sampled on the rising edge of T_3 of the last machine cycle of any instruction.
$\overline{WAIT}$ (Wait)	Input, active Low. This line indicates to the CPU that the memory or I/O device is not ready for data transfer. It is sampled on the falling edge of T_2 and any subsequent $\overline{WAIT}$ states.
B/$\overline{W}$ (Byte/Word)	Output, Low = word, three-state. This signal defines the type of memory reference on the 16-bit address/data bus.
N/$\overline{S}$ (Normal/System Mode)	Output, Low = system mode, three-state. N/$\overline{S}$ indicates the CPU is in the normal or system mode.
$SN_0 – SN_6$ (Segment Number)	Outputs, active High, three-state. These lines provide the 7-bit segment number used to address one of 128 segments by the memory management unit. Outputs by the 01, 03, and 04 parts only. SN_6 = MSB.
$\overline{SEGT}$ (Segment Trap)	Input, active Low. The memory management unit interrupts the CPU with a low on this line when the MMU detects a segmentation trap. Input on the 01, 03, and 04 parts only. It is sampled on the rising edge of T_3 of the last machine cycle of any instruction.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-08-07

Approved sources of supply for SMD 80003 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8000301UA	0C7V7	Z0800104LMB
8000301XA	0C7V7	Z0800104CMB
8000301ZA	3/	Z8001K2/883
8000302QA	0C7V7	Z0800204CMB
8000302YA	0C7V7	Z0800204LMB
8000303UA	0C7V7	Z0800106LMB
8000303XA	0C7V7	Z0800106CMB
8000303ZA	3/	Z8001AK2/883
8000304UA	0C7V7	Z0800110LMB
8000304XA	0C7V7	Z0800110CMB
8000304ZA	3/	Z8001BK2/883
8000305QA	0C7V7	Z0800210CMB
8000305YA	0C7V7	Z0800210LMB
8000305YC	0C7V7	Z0800210LMB
8000306QA	0C7V7	Z0800206CMB
8000306YA	0C7V7	Z0800206LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	e2v, Inc. dba QP Semiconductor, Inc. 765 Sycamore Drive Milpitas, CA 95035

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.