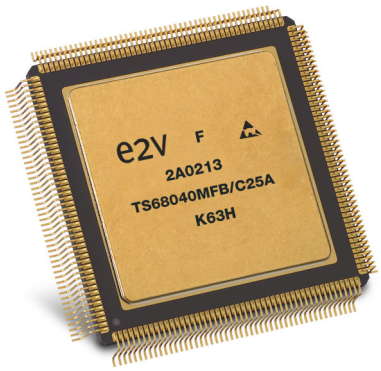
TS68040
Third-Generation 32-bit Microprocessor

Datasheet

Features



- 26-42 MIPS Integer Performance
- 3.5-5.6 MFLOPS Floating-Point-Performance
- IEEE® 754-Compatible FPU
- Independent Instruction and Data MMUs
- 4K bytes Physical Instruction Cache and 4K bytes Physical Data Cache Accessed Simultaneously
- 32-bit, Nonmultiplexed External Address and Data Buses with Synchronous Interface
- User-Object-Code Compatibility with All Earlier TS68000 Microprocessors
- Multimaster/Multiprocessor Support via Bus Snooping
- Concurrent Integer Unit, FPU, MMU, Bus Controller, and Bus Snooper Maximize Throughput
- 4G bytes Direct Addressing Range
- Software Support Including Optimizing C Compiler and UNIX® System V Port
- IEEE P 1149-1 Test Mode (JTAG)
- f = 25 MHz, 33 MHz; V_{CC} = 5V ± 5%; P_D = 7W
- The Use of the TS88915T Clock Driver is Suggested

Description

The TS68040 is e2v's third generation of 68000-compatible, high-performance, 32-bit microprocessors. The TS68040 is a virtual memory microprocessor employing multiple, concurrent execution units and a highly integrated architecture to provide very high performance in a monolithic HCMOS device. On a single chip, the TS68040 integrates a 68030-compatible integer unit, an IEEE 754-compatible floating-point unit (FPU), and fully independent instruction and data demand-paged memory management units (MMUs), including 4K bytes independent instruction and data caches. A high degree of instruction execution parallelism is achieved through the use of multiple independent execution pipelines, multiple internal buses, and a full internal Harvard architecture, including separate physical caches for both instruction and data accesses. The TS68040 also directly supports cache coherency in multimaster applications with dedicated on-chip bus snooping logic.

The TS68040 is user-object-code compatible with previous members of the TS68000 Family and is specifically optimized to reduce the execution time of compiler-generated code. The 68040 HCMOS technology, provides an ideal balance between speed, power, and physical device size.

Figure 1-1 on page 2 is a simplified block diagram of the TS68040. Instruction execution is pipelined in both the integer unit and FPU. Independent data and instruction MMUs control the main caches and the address translation caches (ATCs). The ATCs speed up logical-to-physical address translations by storing recently used translations. The bus snooper circuit ensures cache coherency in multimaster and multiprocessing applications.

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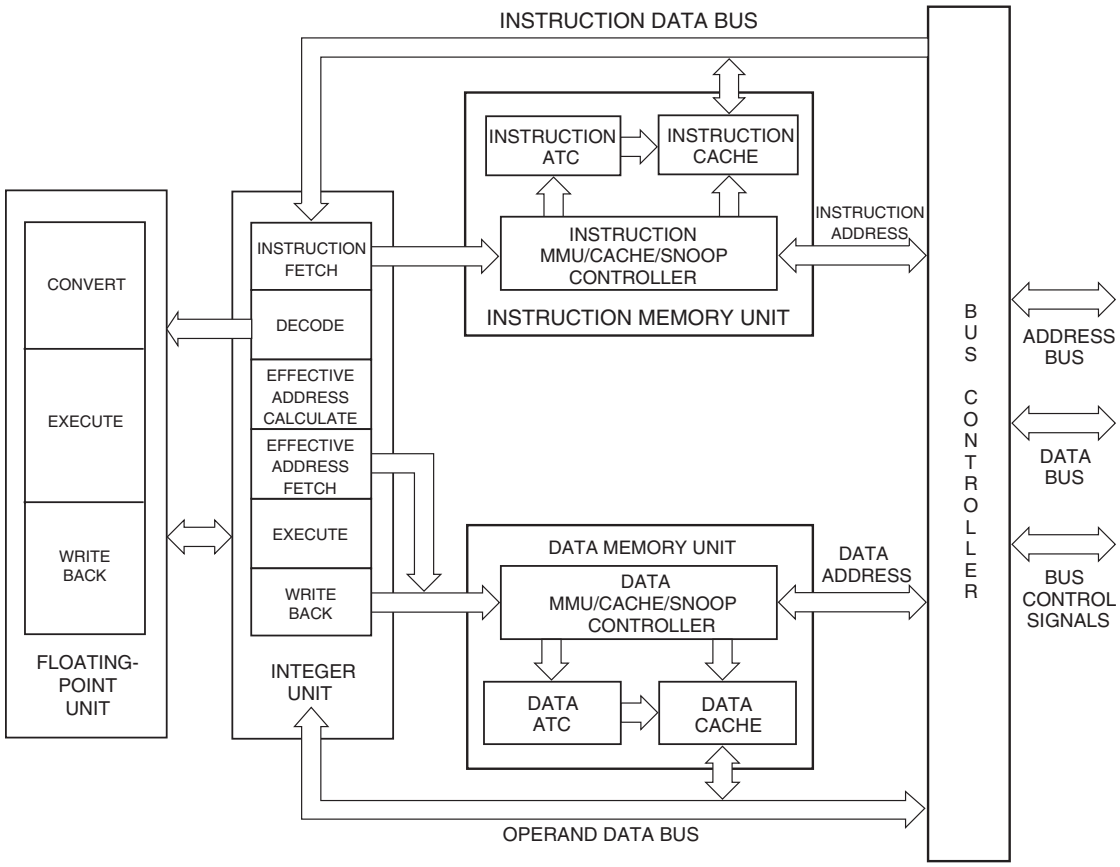
Screening

- MIL-STD-883
- DESC. Drawing 5962-93143
- e2v Standards

1. Block Diagram

Figure 1-1. Simplified Block Diagram



2. Introduction

The TS68040 is an enhanced, 32-bit, HCMOS microprocessor that combines the integer unit processing capabilities of the TS68030 microprocessor with independent 4K bytes data and instruction caches and an on-chip FPU. The TS68040 maintains the 32-bit registers available with the entire TS68000 Family as well as the 32-bit address and data paths, rich instruction set, and versatile addressing modes. Instruction execution proceeds in parallel with accesses to the internal caches, MMU operations, and bus controller activity. Additionally, the integer unit is optimized for high-level language environments.

The TS68040 FPU is user-object-code compatible with the TS68882 floating-point coprocessor and conforms to the ANSI/IEEE Standard 754 for binary floating-point arithmetic. The FPU has been optimized to execute the most commonly used subset of the TS68882 instruction set, and includes additional instruction formats for single and double-precision rounding of results. Floating-point instructions in the FPU execute concurrently with integer instructions in the integer unit.

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The MMUs support multiprocessing, virtual memory systems by translating logical addresses to physical addresses using translation tables stored in memory. The MMUs store recently used address mappings in two separate ATCs-on-chip.

When an ATC contains the physical address for a bus cycle requested by the processor, a translation table search is avoided and the physical address is supplied immediately, incurring no delay for address translation. Each MMU has two transparent translation registers available that define a one-to-one mapping for address space segments ranging in size from 16M bytes to 4G bytes each.

Each MMU provides read-only and supervisor-only protections on a page basis. Also, processes can be given isolated address spaces by assigning each a unique table structure and updating the root pointer upon a task swap. Isolated address spaces protect the integrity of independent processes.

The instruction and data caches operate independently from the rest of the machine, storing information for fast access by the execution units. Each cache resides on its own internal address bus and internal data bus, allowing simultaneous access to both. The data cache provides write through or copyback write modes that can be configured on a page-by-page basis.

The TS68040 bus controller supports a high-speed, non multiplexed, synchronous external bus interface, which allows the following transfer sizes: byte, word (2 bytes), long word (4 bytes), and line (16 bytes). Line accesses are performed using burst transfers for both reads and writes to provide high data transfer rates.

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3. Pin Assignments

3.1 PGA 179

Figure 3-1. Bottom View

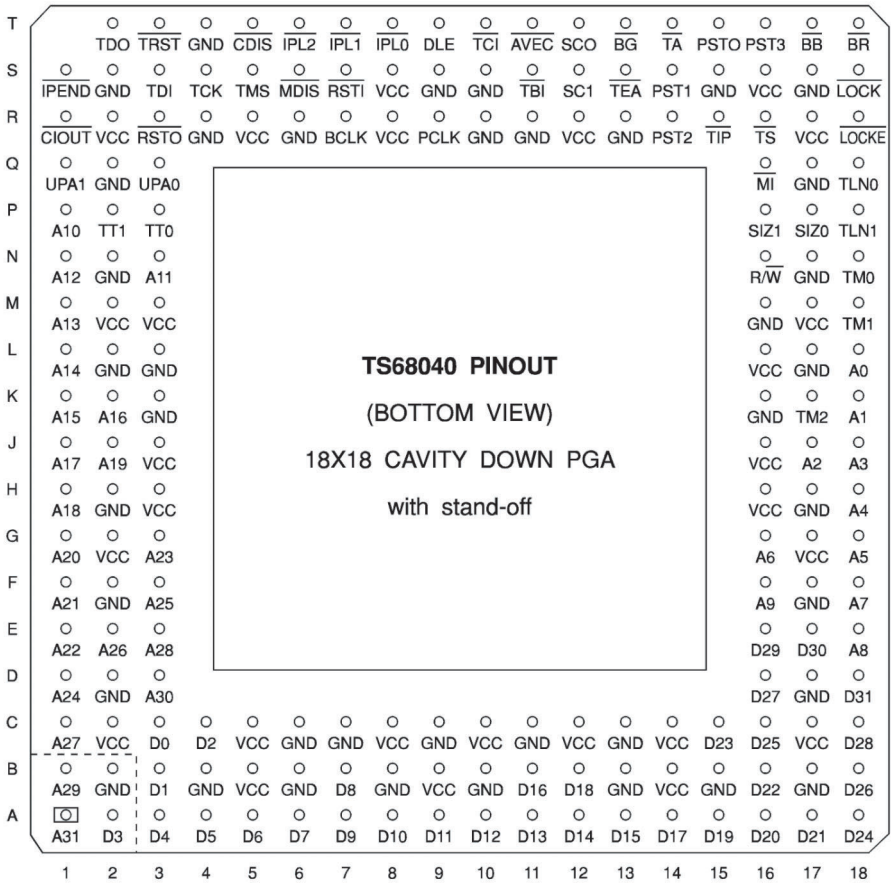

Table 3-1. Power Supply Affectation to PGA Body

	GND	V_{CC}
PLL		S8
Internal Logic	C6, C7, C9, C11,C13, K3, K16, L3, M16, R4, R11, R13, S10, T4, S9, R6, R10	C5, C8, C10, C12, C14, H3, H16, J3, J16, L16, M3, R5, R12, R8
Output Drivers	B2, B4, B6, B8, B10, B13, B15, B17, D2, D17, F2, F17, H2, H17, L2, L17, N2, N17, Q2, Q17, S2, S15, S17	B5, B9, B14, C2, C17, G2, G17, M2, M17, R2, R17, S16

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3.2 CQFP 196

Figure 3-2. Pin Assignments

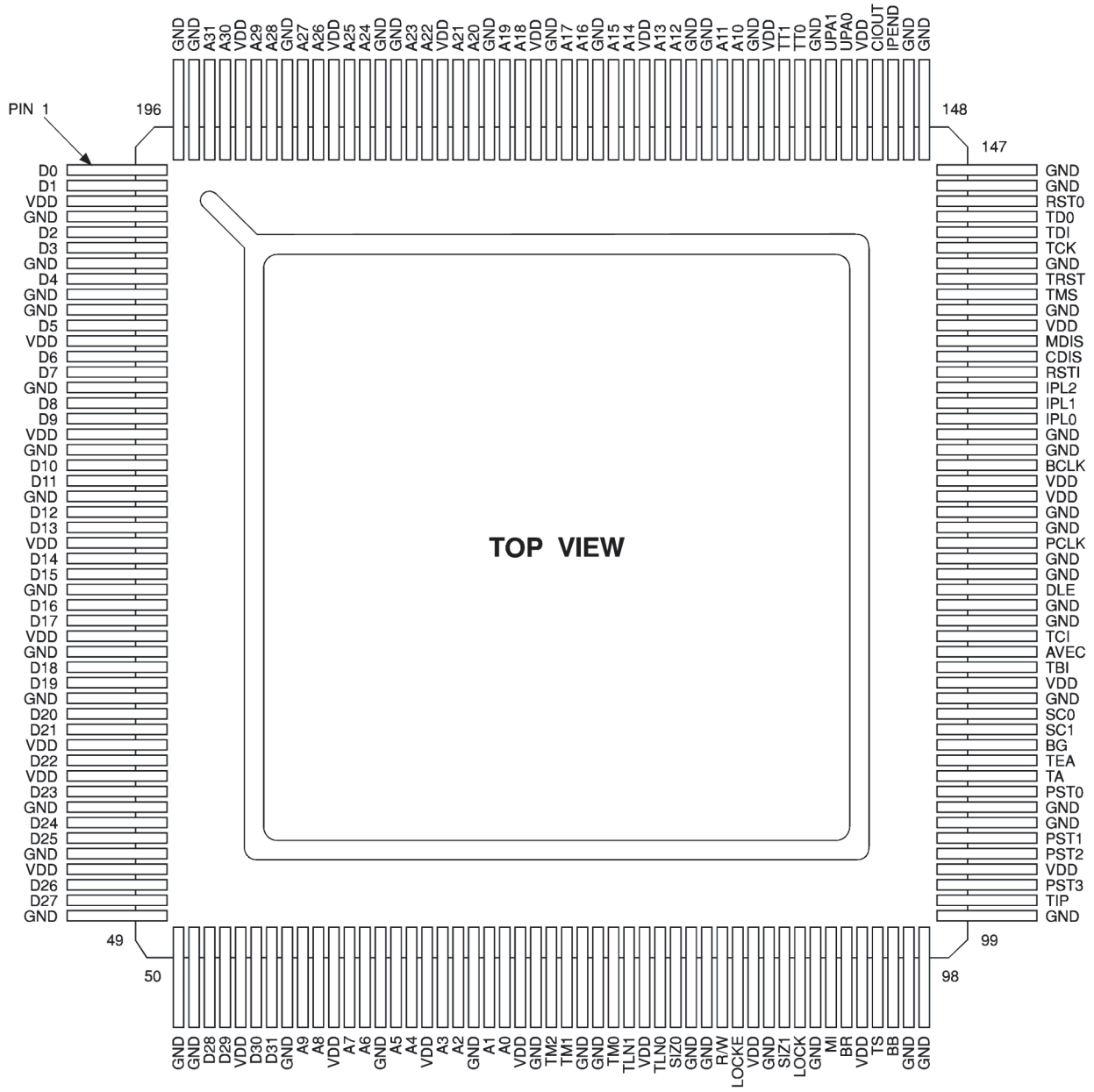

Table 3-2. Power Supply Affectation to CQFP Body

	GND	**V_{CC}**
PLL		127
Internal Logic	4, 9, 10, 19, 32, 45, 73, 88, 113, 119, 121, 122, 124, 125, 129, 130, 141, 159, 172	3, 18, 31, 40, 46, 60, 72, 87, 114, 126, 137, 158, 173, 186
Output Drivers	7, 15, 22, 28, 35, 42, 49, 50, 51, 57, 63, 69, 76, 77, 83, 84, 91, 97, 98, 99, 105, 106, 146, 147, 148, 149, 155, 162, 163, 169, 176, 182, 183, 189, 195, 196	12, 25, 38, 54, 66, 80, 94, 102, 152, 166, 179, 192

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4. Signal Description

Figure 3-1 and Table 3-1 describe the signals on the TS68040 and indicate signal functions. The test signals, $\overline{TRST}$, TMS, TCK, TDI, and TDO, comply with subset P-1149.1 of the IEEE testability bus standard.

Figure 4-1. Functional Signal Groups

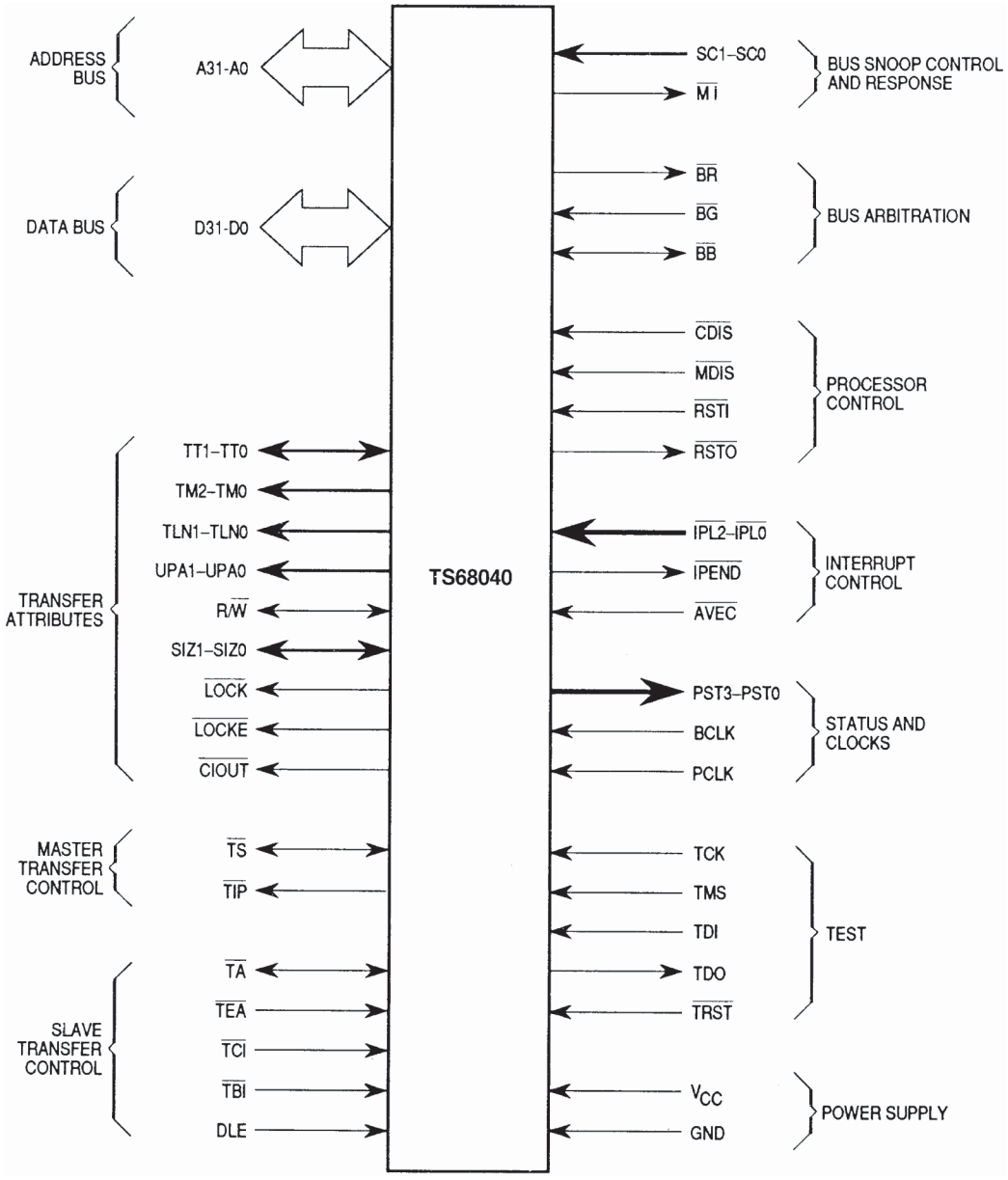

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Table 4-1. Signal Index

Signal Name	Mnemonic	Function
Address Bus	A31-A0	32-bit address bus used to address any of 4G bytes
Data Bus	D31-D0	32-bit data bus used to transfer up to 32 bits of data per bus transfer
Transfer Type	TT1, TT0	Indicates the general transfer type: normal, MOVE 16, alternate logical function code, and acknowledge
Transfer Modifier	TM2, TM0	Indicates supplemental information about the access
Transfer Line Number	TLN1, TLN0	Indicates which cache line in a set is being pushed or loaded by the current line transfer
User Programmable Attributes	UPA1, UPA0	User-defined signals, controlled by the corresponding user attribute bits from the address translation entry
Read Write	R/$\overline{W}$	Identifies the transfer as a read or write
Transfer Size	SIZ1, SIZ0	Indicates the data transfer size. These signals, together with A0 and A1, define the active sections of the data bus
Bus Lock	$\overline{LOCK}$	Indicates a bus transfer is part of a read-modify-write operation, and that the sequence of transfers should not be interrupted
Bus Lock End	$\overline{LOCKE}$	Indicates the current transfer is the last in a locked sequence of transfer
Cache Inhibit Out	$\overline{CIOUT}$	Indicates the processor will not cache the current bus transfer
Transfer Start	$\overline{TS}$	Indicates the beginning of a bus transfer
Transfer in Progress	$\overline{TIP}$	Asserted for the duration of a bus transfer
Transfer Acknowledge	$\overline{TA}$	Asserted to acknowledge a bus transfer
Transfer Error Acknowledge	$\overline{TEA}$	Indicates an error condition exists for a bus transfer
Transfer Cache Inhibit	$\overline{TCI}$	Indicates the current bus transfer should not be cached
Transfer Burst Inhibit	$\overline{TBI}$	Indicates the slave cannot handle a line burst access
Data Latch Enable	DLE	Alternate clock input used to latch input data when the processor is operating in DLE mode
Snoop Control	SC1, SC0	Indicates the snooping operation required during an alternate master access
Memory Inhibit	$\overline{MI}$	Inhibits memory devices from responding to an alternate master access during snooping operations
Bus Request	$\overline{BR}$	Asserted by the processor to request bus mastership
Bus Grant	$\overline{BG}$	Asserted by an arbiter to grant bus mastership to the processor
Bus Busy	$\overline{BB}$	Asserted by the current bus master to indicate it has assumed ownership of the bus
Cache Disable	$\overline{CDIS}$	Dynamically disables the internal caches to assist emulator support
MMU Disable	$\overline{MDIS}$	Disables the translation mechanism of the MMUs
Reset In	$\overline{RSTI}$	Processor reset
Reset Out	$\overline{RSTO}$	Asserted during execution of the RESET instruction to reset external devices
Interrupt Priority Level	$\overline{IPL2}$-$\overline{IPL0}$	Provides an encoded interrupt level to the processor
Interrupt Pending	$\overline{IPEND}$	Indicates an interrupt is pending
Autovector	$\overline{AVEC}$	Used during an interrupt acknowledge transfer to request internal generation of the vector number

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Table 4-1. Signal Index (Continued)

Signal Name	Mnemonic	Function
Processor Status	PST3-PST0	Indicates internal processor status
Bus Clock	BCLK	Clock input used to derive all bus signal timing
Processor Clock	PCLK	Clock input used for internal logic timing. The PCLK frequency is exactly 2X the BCLK frequency
Test Clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)
Test Mode Select	TMS	Selects the principle operations of the test-support circuitry
Test Data Input	TDI	Serial data input for the TAP
Test Data Output	TDO	Serial data output for the TAP
Test Reset	$\overline{\text{TRST}}$	Provides an asynchronous reset of the TAP controller
Power Supply	V_{CC}	Power supply
Ground	GND	Ground connection

5. Scope

This drawing describes the specific requirements for the microprocessor TS68040 - 25 MHz and 33 MHz, in compliance with MIL-STD-883 class B or e2v standard screening.

6. Applicable Documents

6.1 MIL-STD-883

1. MIL-STD-883: test methods and procedures for electronics.
2. MIL-I-38535: general specifications for microcircuits.
3. DESC 5962-93143.

7. Requirements

7.1 General

The microcircuits are in accordance with the applicable document and as specified herein.

7.2 Design and Construction

7.2.1 Terminal Connections

See Figure 2-1 and Figure 2-2.

7.2.2 Lead Material and Finish

Lead material and finish shall be as specified in MIL-STD-883 (see enclosed “MIL-STD-883 C and Internal Standard” on page 46).

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7.2.3 Package

The macro circuits are packaged in hermetically sealed ceramic packages which conform to case outlines of MIL-STD-1835-or as follow:

- CMGA 10-179-PAK pin grid array, but see “179 pins – PGA” on page 43.
- Similar to CQCC1-F196C-U6 ceramic uniform lead chip carrier package with ceramic nonconductive tie-bar but use e2v’s internal drawing, see “196 pins – Tie Bar CQFP Cavity Up (on request)” on page 44.
- Gullwing shape CQFP see “196 pins – Gullwing CQFP cavity up” on page 45.

The precise case outlines are described at the end of the specification (See “Package Mechanical Data” on page 43.) and into MIL-STD-1835.

7.3 Electrical Characteristics

7.3.1 Absolute Maximum Ratings

Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 7-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage Range		-0.3	7.0	V
V_I	Input Voltage Range		-0.3	7.0	V
P_D	Power Dissipation	Large buffers enabled		7.7	W
		Small buffers enabled		6.3	W
T_C	Operating Temperature		-55	T_J	°C
T_{stg}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature(1)			+125	°C
T_{lead}	Lead Temperature	Max.10 sec soldering		+300	°C

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature Tj = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

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Table 7-2. Recommended Conditions of Use
Unless otherwise stated, all voltages are referenced to the reference terminal

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage Range		+4.75		+5.25	V
V_{IL}	Logic Low Level Input Voltage Range		GND - 0.3		0.8	V
V_{IH}	Logic High Level Input Voltage Range		+2.0		V_{CC} + 0.3	V
V_{OH}	High Level Output Voltage		2.4			V
V_{OL}	Low Level Output Voltage				0.5	V
f_c	Clock Frequency	-25 MHz Version		25		MHz
		-33 MHz Version		33		MHz
T_C	Case Operating Temperature Range(1)		-55		T_{Jmax}	°C
T_J	Maximum Operating Junction Temperature				+125	°C

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature T_J = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

7.4 Thermal Considerations

7.4.1 General Thermal Considerations

This section is only given as user information.

As microprocessors are becoming more complex and requiring more power, the need to efficiently cool the device becomes increasingly more important. In the past, the TS68000 Family, has been able to provide a 0-70°C ambient temperature part for speeds less than 40 MHz. However, the TS68040, which has a 50 MHz arithmetic logic unit (ALU) speed, is specified with a maximum power dissipation for a particular mode, a maximum junction temperature, and a thermal resistance from the die junction to the case. This provides a more accurate method of evaluating the environment, taking into consideration both the air-flow and ambient temperature available. This also allows a user the information to design a cooling method which meets both thermal performance requirements and constraints of the board environment.

This section discusses the device characteristics for thermal management, several methods of thermal management, and an example of one method of cooling the TS68040.

7.4.2 Thermal Device Characteristics

The TS68040 presents some inherent characteristics which should be considered when evaluating a method of cooling the device. The following paragraphs discuss these die/package and power considerations.

7.4.3 Die and Package

The TS68040 is being placed in a cavity-down alumina-ceramic 179-pin PGA that has a specified thermal resistance from junction to case of 1°C/W. This package differs from previous TS68000 Family PGA packages which were cavity up. This cavity-down design allows the die to be attached to the top surface of the package, which increases the ability of the part to dissipate heat through the package surface or an attached heat sink. The maximum perimeter that the TS68040 allows for a heat sink on its surface without interfering with the capacitor pads is 1.48" x 1.48". The specific dimensions and design of the particular heat sink will need to be determined by the system designer considering both thermal performance requirements and size requirements.

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7.4.4 Power Considerations

The TS68040 has a maximum power rating, which varies depending on the operating frequency and the output buffer mode combination being used. The large buffer output mode dissipates more power than the small, and the higher frequencies of operation dissipate more power than the lower frequencies. The following paragraphs discuss trade-offs in using the different output buffer modes, calculation of specific maximum power dissipation for different modes, and the relationship of thermal resistances and temperatures.

7.4.5 Output Buffer Mode

The 68040 is capable of resetting to enable for a combination of either large buffers or small buffers on the outputs of the miscellaneous control signals, data bus, and address bus/transfer attribute pins. The large buffers offer quicker output times, which allow for an easier logic design. However, they do so by driving about 11 times as much current as the small buffers (refer to TS68040 Electrical specifications for current output). The designer should consider whether the quicker timings present enough advantage to justify the additional consideration to the individual signal terminations, the die power consumption, and the required cooling for the device. Since the TS68040 can be powered-up in one of eight output buffer modes upon reset, the actual maximum power consumption for TS68040 rated at a particular maximum operating frequency is dependent upon the power up mode.

Therefore, the TS68040 is rated at a maximum power dissipation for either the large buffers or small buffers at a particular frequency (refer to TS68040 Electrical specifications). This allows the possibility of some of the thermal management to be controlled upon reset. The following equation provides a rough method to calculate the maximum power consumption for a chosen output buffer mode:

$$P_D = P_{DSB} + (P_{DLB} - P_{DSB}) \cdot (PINS_{LB}/PINS_{CLB}) \qquad (1)$$

where:

P_D = Max. power dissipation for output buffer mode selected

P_{DSB} = Max. power dissipation for small buffer mode (all outputs)

P_{DLB} = Max. power dissipation for large buffer mode (all outputs)

$PINS_{LB}$ = Number of pins large buffer mode

$PINS_{CLB}$ = Number of pins capable of the large buffer mode

Table 6-3 shows the simplified relationship on the maximum power dissipation for eight possible configurations of output buffer modes.

Table 7-3. Maximum Power Dissipation for Output Buffer Mode Configurations

Output Configuration			Maximum Power Dissipation
Data Bus	**Address Bus and Transfer Attrib.**	**Misc. Control Signals**	**PD**
Small Buffer	Small Buffer	Small Buffer	P_{DSB}
Small Buffer	Small Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 13\%$
Small Buffer	Large Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 52\%$

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Table 7-3. Maximum Power Dissipation for Output Buffer Mode Configurations (Continued)

Output Configuration			Maximum Power Dissipation
Data Bus	Address Bus and Transfer Attrib.	Misc. Control Signals	PD
Small Buffer	Large Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 65\%$
Large Buffer	Small Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 35\%$
Large Buffer	Small Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 48\%$
Large Buffer	Large Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 87\%$
Large Buffer	Large Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 100\%$

To calculate the specific power dissipation of a specific design, the termination method of each signal must be considered. For example, a signal output that is not connected would not dissipate any additional power if it were configured in the large buffer rather than the small buffer mode.

7.4.6 Relationships Between Thermal Resistances and Temperatures

Since the maximum operating junction temperature has been specified to be 125°C. The maximum case temperature, TC, in °C can be obtained from:

$$T_C = T_J - P_D \cdot \Phi_{JC} \quad (2)$$

where:

T_C = Maximum case temperature
T_J = Maximum junction temperature
P_D = Maximum power dissipation of the device
Φ_{JC} = Thermal resistance between the junction of the die and the case

In general, the ambient temperature, T_A, in °C is a function of the following formula:

$$T_A = T_J - P_D \cdot \Phi_{JC} - P_D \cdot \Phi_{CA} \quad (3)$$

Where the thermal resistance from case to ambient, Φ_{CA}, is the only user-dependent parameter once a buffer output configuration has been determined. As seen from equation (3), reducing the case to ambient thermal resistance increases the maximum operating ambient temperature. Therefore, by utilizing such methods as heat sinks and ambient air cooling to minimize the Φ_{CA}, a higher ambient operating temperature and/or a lower junction temperature can be achieved.

However, an easier approach to thermal evaluation uses the following formulas:

$$T_A = T_J - P_D \cdot \Phi_{JA} \quad (4)$$

or alternatively,

$$T_J = T_A - P_D \cdot \Phi_{JA} \quad (5)$$

where:

Φ_{JA} = thermal resistance from the junction to the ambient ($\Phi_{JC} + \Phi_{CA}$).

This total thermal resistance of a package, Φ_{JA}, is a combination of its two components, Φ_{JC} and Φ_{CA}. These components represent the barrier to heat flow from the semiconductor junction to the package (case) surface (Φ_{JC}) and from the case to the outside ambient (Φ_{JC}). Although Φ_{JC} is device related and cannot be influenced by the user, Φ_{CA} is user dependent. Thus, good thermal management by the user can significantly reduce Φ_{CA} achieving either a lower semiconductor junction temperature or a higher ambient operating temperature.

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7.4.7 Thermal Management Techniques

To attain a reasonable maximum ambient operating temperature, a user must reduce the barrier to heat flow from the semiconductor junction to the outside ambient (Φ_{JA}). The only way to accomplish this is to significantly reduce Φ_{CA} by applying such thermal management techniques as heat sinks and ambient air cooling.

The following paragraphs discuss some results of a thermal study of the TS68040 device without using any thermal management techniques; using only air-flow cooling, using only a heat sink, and using heat sink combined with air-flow cooling.

7.4.8 Thermal Characteristics in Still Air

A sample size of three TS68040 packages was tested in free-air cooling with no heat sink. Measurements showed that the average Φ_{JA} was 22.8°C/W with a standard deviation of 0.44°C/W. The test was performed with 3W of power being dissipated from within the package. The test determined that Φ_{JA} will decrease slightly for the increasing power dissipation range possible. Therefore, since the variance in Φ_{JA} within the possible power dissipation range is negligible, it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Using the formulas introduced previously, Table 6-4 shows the results of a maximum power dissipation of 3 and 5W with no heat sink or air-flow (refer to Table 6-3 to calculate other power dissipation values).

Table 7-4. Thermal Parameters With No Heat Sink or Air-flow

Defined Parameters			Measured	Calculated		
P_D	T_J	Φ_{JC}	Φ_{JA}	$\Phi_{CA} = \Phi_{JA} - \Phi_{JC}$	$T_C = T_J - P_D * \Phi_{JC}$	$T_A = T_J - P_D * \Phi_{JA}$
3 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	122°C	59.6°C
5 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	120°C	16°C

As seen by looking at the ambient temperature results, most users will want to implement some type of thermal management to obtain a more reasonable maximum ambient temperature.

7.4.9 Thermal Characteristics in Forced Air

A sample size of three TS68040 packages was tested in forced air cooling in a wind tunnel with no heat sink. This test was performed with 3W of power being dissipated from within the package. As previously mentioned, since the variance in ΦJA within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Using the previous formulas, Table 6-5 shows the results of the maximum power dissipation at 3 and 5W with air-flow and no heat sink (refer to Table 6-3 to calculate other power dissipation values).

Table 7-5. Thermal Parameters With Forced Air Flow and No Heat Sink

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Air-flow velocity	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	3W	125°C	1°C/W	11.7°C/W	10.7°C/W	122°C	89.9°C
250 LFM	3W	125°C	1°C/W	10°C/W	9°C/W	122°C	95°C
500 LFM	3W	125°C	1°C/W	8.9°C/W	7.9°C/W	122°C	98.3°C
750 LFM	3W	125°C	1°C/W	8.5°C/W	7.5°C/W	122°C	99.5°C
1000 LFM	3W	125°C	1°C/W	8.3°C/W	7.3°C/W	122°C	100.1°C

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Table 7-5. Thermal Parameters With Forced Air Flow and No Heat Sink (Continued)

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Air-flow velocity	**P_D**	**T_J**	**Φ_{JC}**	**Φ_{JA}**	**Φ_{CA}**	**T_C**	**T_A**
100 LFM	5W	125°C	1°C/W	11.7°C/W	10.7°C/W	120°C	66.5°C
250 LFM	5W	125°C	1°C/W	10°C/W	9°C/W,	120°C	75°C
500 LFM	5W	125°C	1°C/W	8.9°C/W	7.9°C/W	120°C	80.5°C
750 LFM	5W	125°C	1°C/W	8.5°C/W	7.5°C/W	120°C	82.5°C
1000 LFM	5W	125°C	1°C/W	8.3°C/W	7.3°C/W	120°C	83.5°C

By reviewing the maximum ambient operating temperatures, it can be seen that by using the all-small-buffer configuration of the TS68040 with a relatively small amount of air flow (100 LFM), a 0-70°C ambient operating temperature can be achieved. However, depending on the output buffer configuration and available forced-air cooling, additional thermal management techniques may be required.

7.4.10 Thermal Characteristics with a Heat Sink

In choosing a heat sink the designer must consider many factors: heat sink size and composition, method of attachment, and choice of a wet or dry connection. The following paragraphs discuss the relationship of these decisions to the thermal performance of the design noticed during experimentation.

The heat sink size is one of the most significant parameters to consider in the selection of a heat sink. Obviously a larger heat sink will provide better cooling. However, it is less obvious that the most benefit of the larger heat sink of the pin fin type used in the experimentation would be at still air conditions. Under forced-air conditions as low as 100 LFM, the difference between the ΦCA becomes very small (0.4°C/W or less). This difference continues to decrease as the forced air flow increases. The particular heat sink used in our testing fit the perimeter package surface area available within the capacitor pads on the TS68040 (1.48" x 1.48") and showed a nice compromise between height and thermal performance needs. The heat sink base perimeter area was 1.24" x 1.30" and its height was 0.49". It was a pin-fin-type (i.e. bed of nails) design composed of Al alloy. The heat sink is shown in Figure 6-1 can be obtained through Thermalloy Inc. by referencing part number 2338B.

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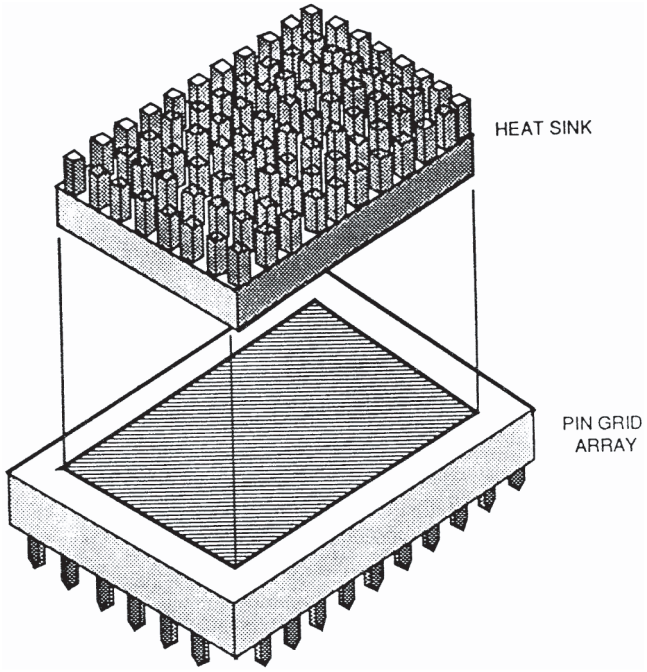
Figure 7-1. Heat Sink Example



All pin fin heat sinks tested were made from extrusion Al products. The planar face of the heat sink mating to the package should have a good degree of planarity; if it has any curvature, the curvature should be convex at the central region of the heat sink surface to provide intimate physical contact to the PGA surface. All heat sinks tested met this criteria. Nonplanar, concave curvature the central regions of the heat sink will result in poor thermal contact to the package. A specification needs to be determined for the planarity of the surface as part of any heat sink design.

Although there are several ways to attach a heat sink to the package, it was easiest to use a demountable heat sink attach called “E-Z attach for PGA packages” developed by Thermalloy (see Figure 6-2). The heat sink is clamped to the package with the help of a steel spring to a plastic frame (or plastic shoes Besides the height of the heat sink and plastic frame, no additional height added to the package. The interface between the ceramic package and the heat sink was evaluated for both dry and wet (i.e., thermal grease) interfaces in still air. The thermal grease reduced the Φ_{CA} quite significantly (about 2.5 °C/W) in still air. Therefore, it was used in all other testing done with the heat sink. According to other testing, attachment with thermal grease provided about the same thermal performance as if a thermal epoxy were used.

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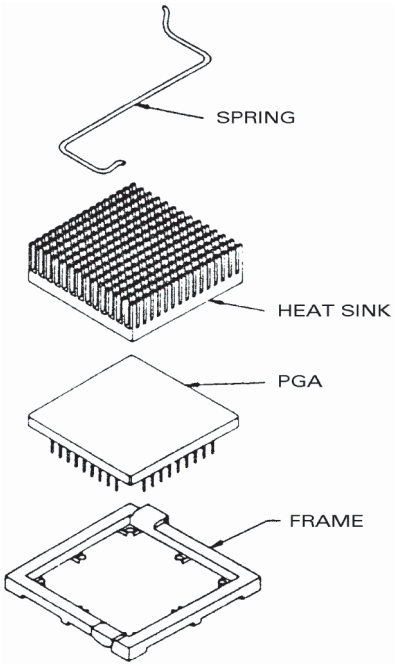
Figure 7-2. Heat Sink with Attachment



A sample size of one TS68040 package was tested in still air with the heat sink and attachment method previously described. This test was performed with 3W of power being dissipated from within the package. Since the variance in Φ_{JA} within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Table 6-6 shows the result assuming a maximum power dissipation of the part at 3 and 5W (refer to Table 6-3 to calculate other power dissipation values).

Table 7-6. Thermal Parameters With Heat Sink and No Air Flow

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Heat Sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
2338B	3W	125°C	1°C/W	14°C/W	13°C/W	122°C	83°C
2338B	5W	125°C	1°C/W	14°C/W	13°C/W	120°C	55°C

7.4.11 Thermal Characteristics with a Heat Sink and Forced Air

A sample size of three TS68040 packages was tested in forced-air cooling in a wind tunnel with a heat sink. This test was performed with 3W of power being dissipated from within the package. As mentioned previously, the variance in Φ_{JA} within the possible power range is negligible; it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Table 6-7 shows the results, assuming a maximum power dissipation at 3 and 5W with air flow and heat sink thermal management (refer to Table 6-3 to calculate other power dissipation values).

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Table 7-7. Thermal Parameters with Heat Sink and Air Flow

Thermal Mgmt. Technique		Defined Parameters			Measured	Calculated		
Air-flow	**Heat sink**	**P_D**	**T_J**	**Φ_{JC}**	**Φ_{JA}**	**Φ_{CA}**	**T_C**	**T_A**
100 LFM	2338B	3W	125°C	1°C/W	3.1°C/W	2.1°C/W	122°C	115.7°C
250 LFM	2338B	3W	125°C	1°C/W	2.2°C/W	1.2°C/W	122°C	118.4°C
500 LFM	2338B	3W	125°C	1°C/W	1.7°C/W	0.7°C/W	122°C	119.9°C
750 LFM	2338B	3W	125°C	1°C/W	1.5°C/W	0.5°C/W	122°C	120.5°C
1000 LFM	2338B	3W	125°C	1°C/W	1.4°C/W	0.4°C/W	122°C	120.8°C
100 LFM	2338B	5W	125°C	1°C/W	3.1°C/W	2.1°C/W	120°C	109.5°C
250 LFM	2338B	5W	125°C	1°C/W	2.2°C/W	1.2°C/W	120°C	114°C
500 LFM	2338B	5W	125°C	1°C/W	1.7°C/W	0.7°C/W	120°C	116.5°C
750 LFM	2338B	5W	125°C	1°C/W	1.5°C/W	0.5°C/W	120°C	117.5°C
1000 LFM	2338B	5W	125°C	1°C/W	1.4°C/W	0.4°C/W	120°C	118°C

7.4.12 Thermal Testing Summary

Testing proved that a heat sink in combination with a relatively small amount of air-flow (100 LFM or less) will easily realize a 0-70°C ambient operating temperature for the TS68040 with almost any configuration of the output buffers. A heat sink alone may be capable of providing all necessary cooling, depending on the particular heat sink height/size restraints, the maximum ambient operating temperature required, and the output buffer configuration chosen. Also forced air cooling alone may attain a 0-70°C ambient operating temperature. However this factor is highly dependent on the output buffer configuration chosen and the available forced air for cooling. Figure 6-3 is a summary of the test results of the relationship between Φ_{JA} and air-flow for the TS68040.

Figure 7-3. Relationship of Φ_{JA} Air-Flow for PGA

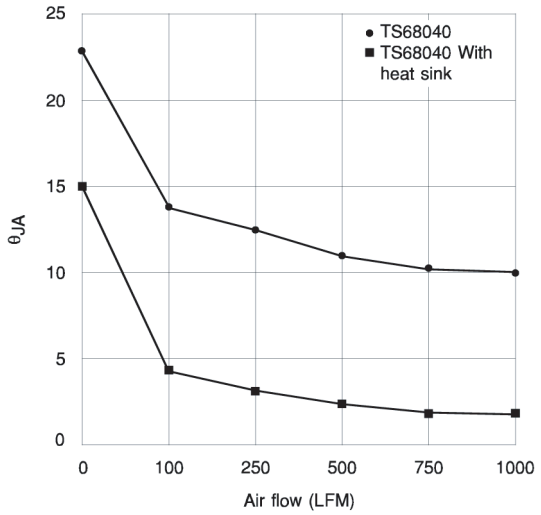

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Table 7-8. Characteristics Guaranteed

Package	Symbol	Parameter	Value	Unit
PGA 179	θ_{J-A}	Thermal Resistance Junction-to-ambient	See Figure 6-3	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W
CQFP 196	θ_{J-A}	Thermal Resistance Junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W

7.5 Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or for e2v standard screening.

7.6 Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

- e2v Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code Of Inspection Lot
- ESD Identifier If Available
- Country Of Manufacturing

8. Quality Conformance Inspection

8.1 DESC/MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Groups C and D inspection are performed on a periodical basis.

9. Electrical Characteristics

9.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 8-1: Static electrical characteristics for the electrical variants.
- Table 8-2: Dynamic electrical characteristics for TS68040 (25 MHz, 33 MHz).

For static characteristics (Table 8-1), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Table 8-2), test methods refer to clause "Static Characteristics" on page 19 of this specification.

Indication of "min." or "max." in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause Table 6-2 here above.

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9.2 Static Characteristics

Table 9-1. Electrical Characteristics
$-55°C \le T_C \le T_{Jmax}$; $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified(1)(2)(3)(4)

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Voltage	2	V_{CC}	V
V_{IL}	Input Low Voltage	GND	0.8	V
V_U	Undershoot		- 0.8	V
I_{in}	Input Leakage Current at 0.5/2.4V — $\overline{AVEC}$, BCLK $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$, PCLK, $\overline{RSTI}$, SCn, $\overline{TBI}$, $\overline{TCI}$, TCK, $\overline{TEA}$	-20	20	µA
I_{TSI}	Hi-z (Off-state) Leakage Current at 0.5/2.4V — An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, $\overline{TA}$, TDO, $\overline{TIP}$, TLNn, TMn, $\overline{TS}$, TTn, UPAn	-20	20	µA
I_{IL}	Signal Low Input Current V_{IL} = 0.8V — TMS, TDI, $\overline{TRST}$	-1.1	-0.18	mA
I_{IH}	Signal High Input Current V_{IH} = 2.0V — TMS, TDI, $\overline{TRST}$	-0.94	-0.16	mA
V_{OH}	Output High Voltage Larger Buffers - I_{OH} = 35 mA Small Buffers - I_{OH} = 5 mA	2.4		V
V_{OL}	Output Low Voltage Larger buffers - I_{OL} = 35 mA Small buffers - I_{OL} = 5 mA		0.5	V
P_D	Power Dissipation (T_J = 125°C) Larger Buffers Enabled Small Buffers Enabled		7.7 6.3	W
C_{in}	Capacitance - Note 4 V_{in} = 0V, f = 1 MHz		25	pF

Notes:
1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
3. Capacitance is periodically sampled rather than 100% tested.
4. Power dissipation may vary in between limits depending on the application.

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9.3 Dynamic Characteristics

Table 9-2. Clock AC Timing Specifications (see Figure 8-1)
$-55°C \le T_C \le T_{Jmax}$; $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified[1][2][3][4]

Num	Characteristic	25 MHz		33 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation		20	25	20	33	MHz
1	PCLK Cycle Time	20	25	15	25	ns
2	PCLK Rise Time[4]		1.7		1.7	ns
3	PCLK Fall Time[4]		1.6		1.6	ns
4	PCLK Duty Cycle Measured at 1.5V[4]	47.5	52.5	46.67	53.33	%
4a	PCLK Pulse Width High Measured at 1.5V[3][4]	9.5	10.5	7	8	ns
4b	PCLK Pulse Width Low Measured at 1.5V[3][4]	9.5	10.5	7	8	ns
5	BCLK Cycle Time	40	50	30	60	ns
6, 7	BCLK Rise and Fall Time		4		3	ns
8	BCLK Duty Cycle Measured at 1.5V[4]	40	60	40	60	%
8a	BCLK Pulse Width High Measured at 1.5V[4]	16	24	12	18	ns
8b	BCLK Pulse Width Low Measured at 1.5V[4]	16	24	12	18	ns
9	PCLK, BCLK Frequency Stability[4]		1000		1000	ppm
10	PCLK to BCLK Skew		9		n/a	ns

Notes:
1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
3. Specification value at maximum frequency of operation.
4. If not tested, shall be guaranteed to the limits specified.

Figure 9-1. Clock Input Timing

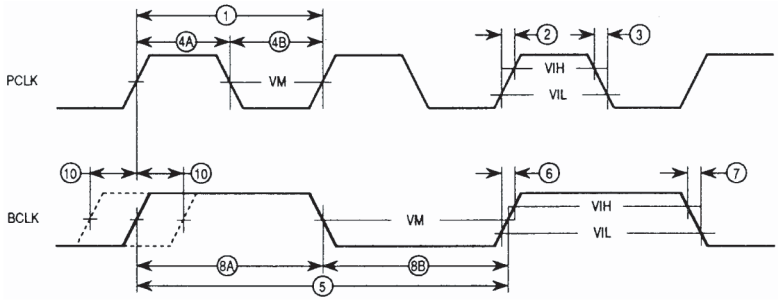

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Table 9-3. Output AC Timing Specifications[1] (Figure 8-2 to Figure 8-8)

These output specifications are only for 25 MHz. They must be scaled for lower operating frequencies. Refer to TS6804DH/AD for further information. -55°C ≤ T_C ≤ T_{Jmax}; 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified.[2][3][4]

Num	Characteristic	25 MHz				33 MHz				Unit
		Large Buffer[1]		Small Buffer[1]		Large Buffer[1]		Small Buffer[1]		
		Min	Max	Min	Max	Min	Max	Min	Max	
11	BCLK to address $\overline{CIOUT}$, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, TLN, TMn, UPAn valid[5]	9	21	9	30	6.50	18	6.50	25	ns
12	BCLK to output invalid (output hold)	9		9		6.50		6.50		ns
13	BCLK to $\overline{TS}$ valid	9	21	9	30	6.50	18	6.50	25	ns
14	BCLK to $\overline{TIP}$ valid	9	21	9	30	6.50	18	6.50	25	ns
18	BCLK to data-out valid[6]	9	23	9	32	6.50	20	6.50	27	ns
19	BCLK to data-out invalid (output hold)[6]	9		9		6.50		6.50		ns
20	BCLK to output low impedance[5][6]	9		9		6.50		6.50		ns
21	BCLK to data-out high impedance	9	20	9	20	6.50	17	6.50	17	ns
26	BCLK to multiplexed address valid[5]	19	31	19	40	14	26	14	33	ns
27	BCLK to multiplexed address driven[5]	19		19		14		14		ns
28	BCLK to multiplexed address high impedance[5][6]	9	18	9	18	6.50	15	6.50	15	ns
29	BCLK to multiplexed data driven[6]	19		19		14	20	14	20	ns
30	BCLK to multiplexed data valid[6]	19	33	19	42	14	28	14	35	ns
38	BCLK to address $\overline{CIOUT}$, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, $\overline{TS}$, TLNn, TMn, TTn, UPAn high impedance[5]	9	18	9	18	6.50	15	6.50	15	ns
39	BCLK to $\overline{BB}$, $\overline{TA}$, $\overline{TIP}$ high impedance	19	28	19	28	14	23	14	23	ns
40	BCLK to $\overline{BR}$, $\overline{BB}$ valid	9	21	9	30	6.50	18	6.50	25	ns
43	BCLK to $\overline{MI}$ valid	9	21	9	30	6.50	18	6.50	25	ns
48	BCLK to $\overline{TA}$ valid	9	21	9	30	6.50	18	6.50	25	ns
50	BCLK to $\overline{IPEND}$, PSTn, $\overline{RSTO}$ valid	9	21	9	30	6.50	18	6.50	25	ns

Notes:

1. Output timing is specified for a valid signal measured at the pin. Large buffer timing is specified driving a 50Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay, terminated through 50Ω to 2.5V. Large buffer output impedance is typically 3Ω, resulting in incident wave switching for this environment. Small buffer timing is specified driving an unterminated 30Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay. Small buffer output impedance is typically 30Ω; the small buffer specifications include approximately 5 ns for the signal to propagate the length of the transmission line and back.
2. All testing to be performed using worst-case test conditions unless otherwise specified.
3. The following pins are active low: $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPLO}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.
4. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

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5. Timing specifications 11, 20 and 38 for address bus output timing apply when normal bus operation is selected. Specifications 26, 27 and 28 should be used when the multiplexed bus mode of operation is enabled.
6. Timing specifications 18 and 19 for data bus output timing apply when normal bus operation is selected. Specifications 28 and 29 should be used when the multiplexed bus mode of operation is enabled.

Table 9-4. Input AC Timing Specifications (Figure 8-2 to Figure 8-8)
$-55°C \le T_C \le T_{Jmax}$; $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified[(1)(2)(3)(4)]

Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
15	Data-in Valid to BCLK (Setup)	5		4		ns
16	BCLK to Data-in Invalid (Hold)	4		4		ns
17	BCLK to Data-in High Impedance (Read Followed By Write)		49		36.5	ns
22a	$\overline{TA}$ Valid to BCLK (Setup)	10		10		ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	10		10		ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	10		10		ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	11		10		ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ Invalid (Hold)	2		2		ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	5		5		ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2		2		ns
31	DLE Width High	8		8		ns
32	Data-in Valid to DLE (Setup)	2		2		ns
33	DLE to Data-in Invalid (Hold)	8		8		ns
34	BCLK to DLE Hold	3		3		ns
35	DLE High to BCLK	16		12		ns
36	Data-in Valid to BCLK (DLE Mode Setup)	5		5		ns
37	BCLK Data-in Invalid (DLE Mode Hold)	4		4		ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	7		7		ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	8		7		ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ Valid to BCLK (Setup)	10		8		ns
41d	$\overline{IPLn}$ Valid to BCLK (Setup)	4		3		ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$ Invalid (Hold)	2		2		ns
44a	Address Valid to BCLK (Setup)	8		7		ns
44b	SIZn Valid BCLK (Setup)	12		8		ns
44c	TTn Valid to BCLK (Setup)	6		8.5		ns
44d	R/$\overline{W}$ Valid to BCLK (Setup)	6		5		ns
44e	SCn Valid to BCLK (Setup)	10		11		ns
45	BCLK to Address SIZn, TTn, R/$\overline{W}$, SCn Invalid (Hold)	2		2		ns
46	$\overline{TS}$ Valid to BCLK (Setup)	5		9		ns
47	BCLK to $\overline{TS}$ Invalid (Hold)	2		2		ns
49	BCLK to $\overline{BB}$ High Impedance (68040 Assumes Bus Mastership)		9		9	ns

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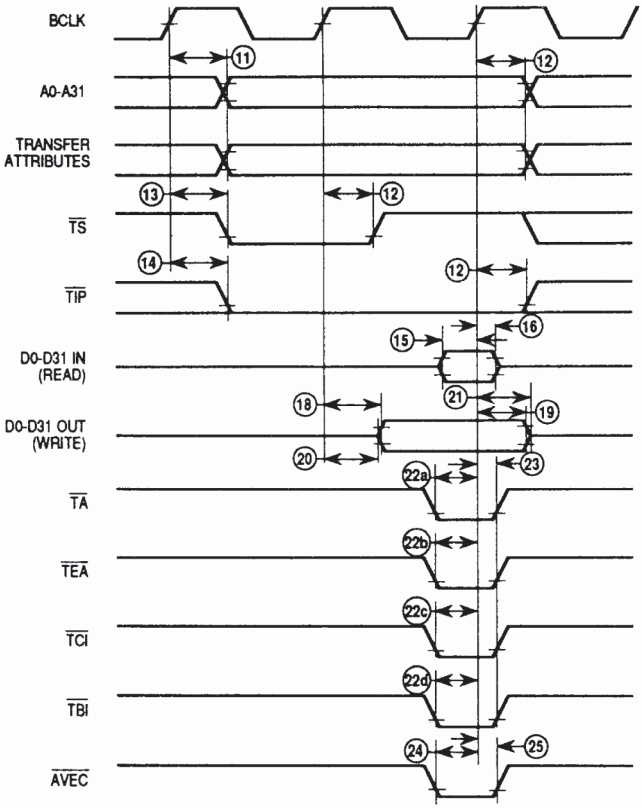
Table 9-4. Input AC Timing Specifications (Figure 8-2 to Figure 8-8) (Continued)
$-55°C \le T_C \le T_{Jmax}$; $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified[1][2][3][4]

Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
51	$\overline{RSTI}$ Valid to BCLK	5		4		ns
52	BCLK to $\overline{RSTI}$ Invalid	2		2		ns
53	Mode Select Setup to $\overline{RSTI}$ Negated[4]	20		20		ns
54	$\overline{RSTI}$ Negated to Mode Selects Invalid[4]	2		2		ns

Notes:
1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. The following pins are active low: $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.
3. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
4. The levels on $\overline{CDIS}$, $\overline{MDIS}$, and the $\overline{IPL2}$-$\overline{IPL0}$ signals enable or disable the multiplexed bus mode, data latch enable mode, and driver impedance selection respectively.

Figure 9-2. Read/Write Timing



Note: Transfer attribute signals UPAN, SIZN, TTN, TMN, TLNN, R/$\overline{W}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{CIOUT}$

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Table 9-5. JTAG Timing Application (Figure 8-9 to Figure 8-12)
$-55°C \le T_C \le T_J max$; $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified[1][2]

Num	Characteristic	Min	Max	Unit
	TCK Frequency	0	10	MHz
1	TCK Cycle Time	100		ns
2	TCK Clock Pulse Width Measured at 1.5V	40		ns
3	TCK Rise and Fall Times	0	10	ns
4	$\overline{TRST}$ Setup Time to TCK Falling Edge	40		ns
5	$\overline{TRST}$ Assert Time	100		ns
6	Boundary Scan Input Data Setup Time	50		ns
7	Boundary Scan Input Data Hold Time	50		ns
8	TCK to Output Data Valid	0	50	ns
9	TCK to Output High Impedance	0	50	ns
10	TMS, TDI Data Setup Time	20		ns
11	TMS, TDI Data Hold Time	5		ns
12	TCK to TDO Data Valid	0	20	ns
13	TCK to TDO High Impedance	0	20	ns

Notes: 1. All testing to be performed using worst-case test conditions unless otherwise specified.

2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125° and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Table 9-6. Boundary Scan Instruction Codes

Bit 2	Bit 1	Bit 0	Instruction Selected	Test Data Register Accessed
0	0	0	Extest	Boundary Scan
0	0	1	Highz	Bypass
0	1	0	Sample/Preload	Boundary Scan
0	1	1	DRVCTLT	Boundary Scan
1	0	0	Shutdown	Bypass
1	0	1	Private	Bypass
1	1	0	DRVCTLS	Boundary Scan
1	1	1	Bypass	Bypass

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9.4 Switching Test Circuit and Waveforms

Figure 9-3. Address and Data Bus Timing — Multiplexed Bus Mode

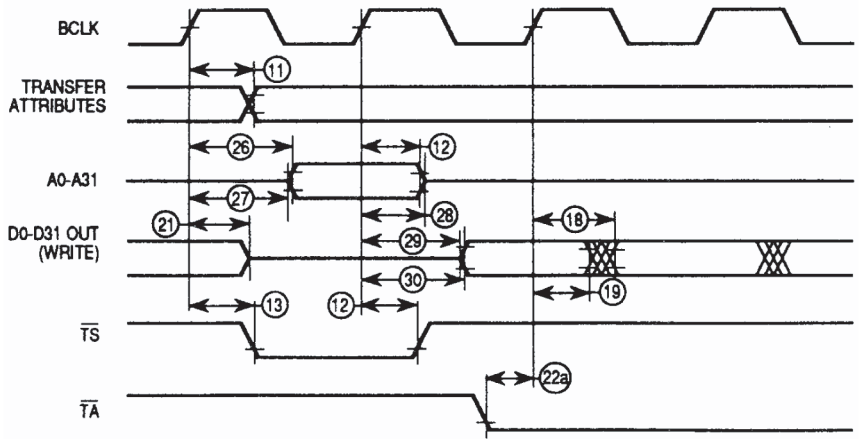

Figure 9-4. DLE Timing Burst Access

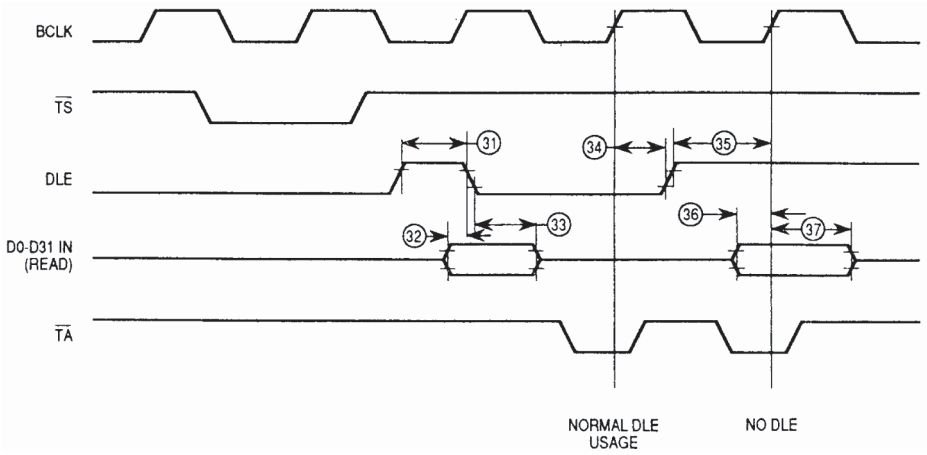

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Figure 9-5. Bus Arbitration Timing

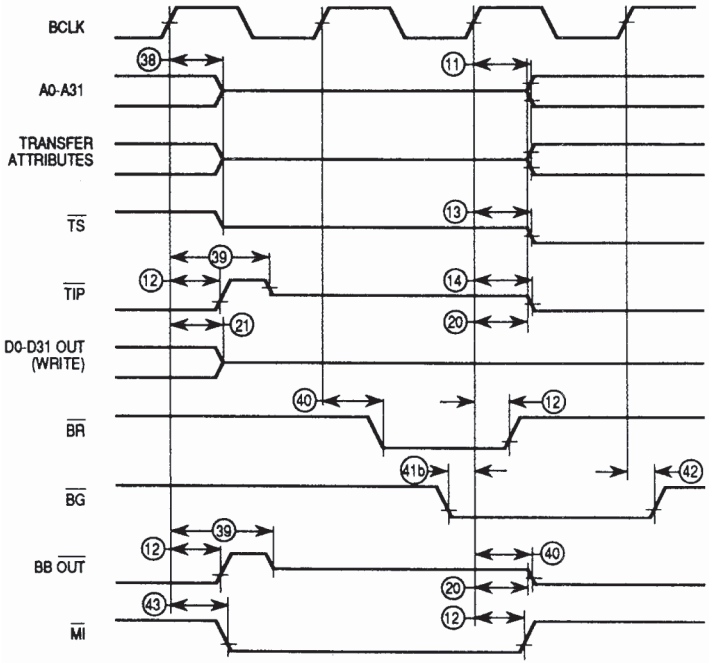

Figure 9-6. Snoop Hit Timing

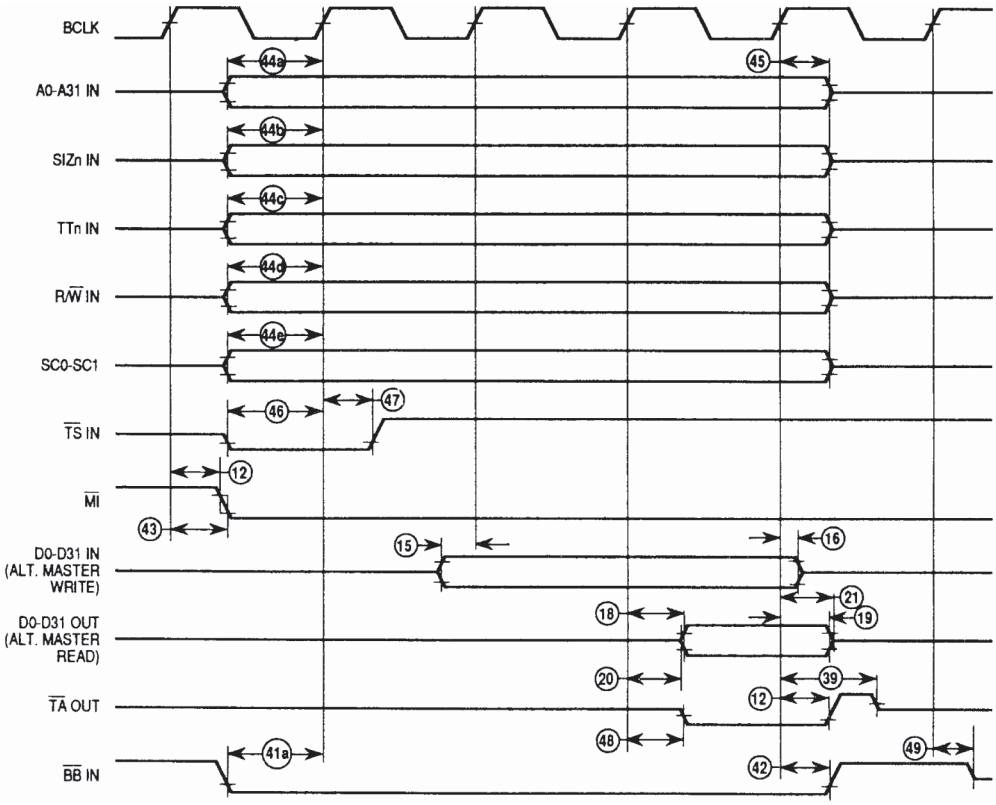

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Figure 9-7. Snoop Miss Timing

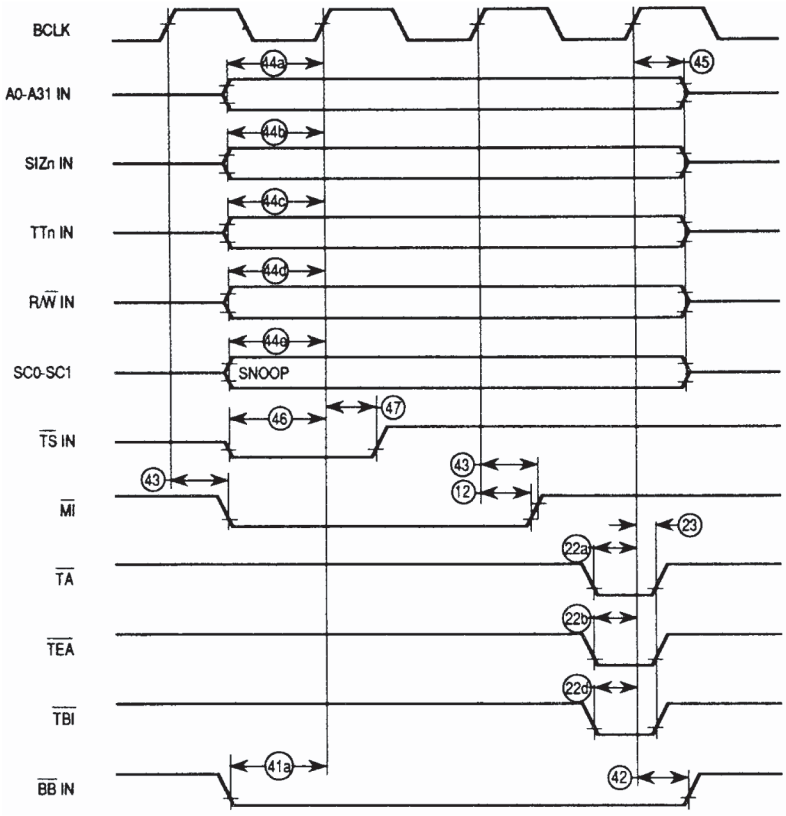

Figure 9-8. Other Signal Timing

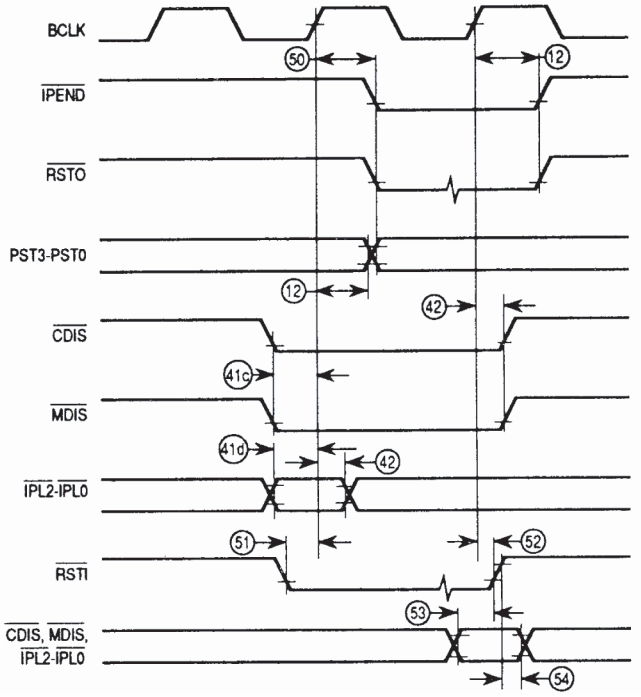

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Figure 9-9. Clock Input Timing Diagram

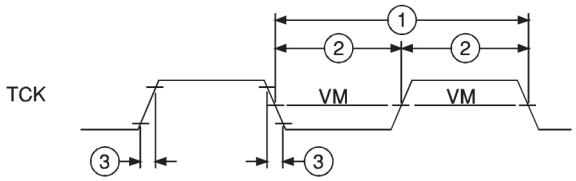


Figure 9-10. $\overline{\text{TRST}}$ Timing Diagram

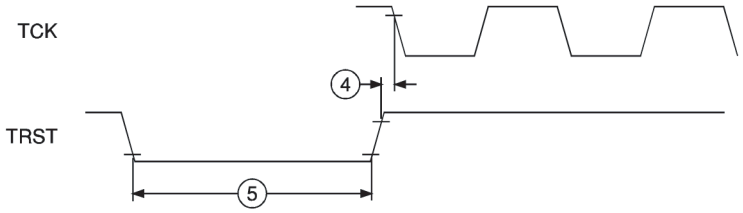


Figure 9-11. Boundary Scan Timing Diagram

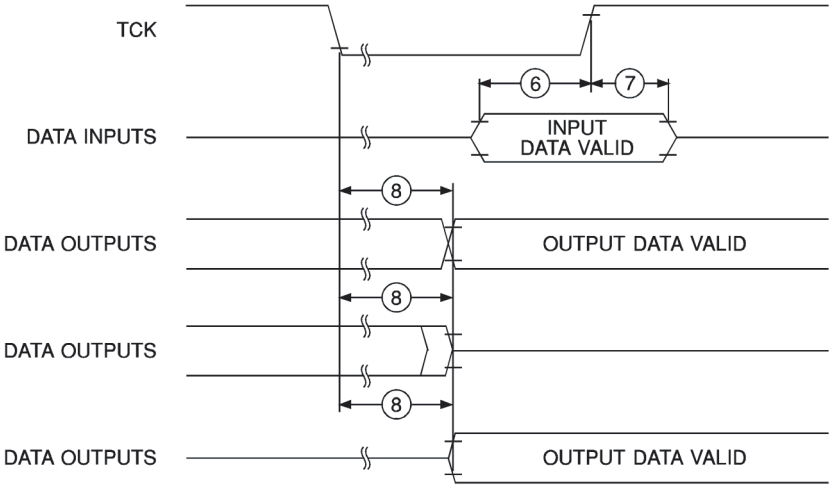
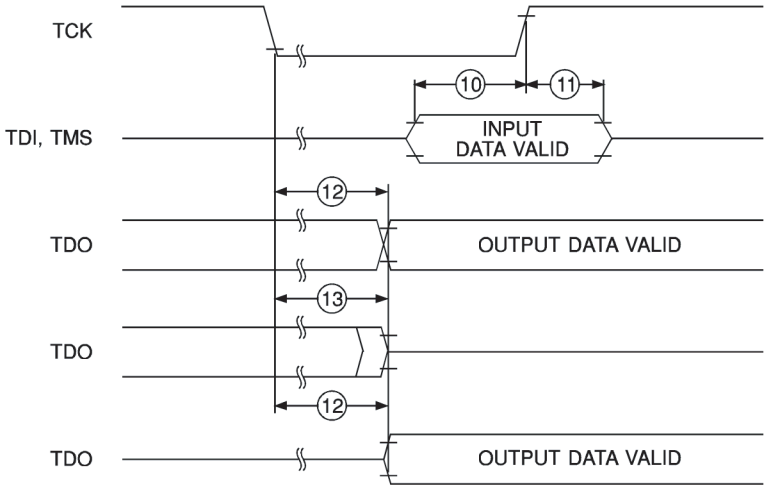


Figure 9-12. Test Access Port Timing Diagram



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10. Functional Description

10.1 Programming Model

The TS68040 integrates the functions of the integer unit, MMU, and FPU. As shown in Figure 9-1, the registers depicted in the programming model provide access and control for the three units. The registers are partitioned into two levels of privilege: user and supervisor. User programs, executing in the user mode, can only use the resources of the user model. System software, executing in the supervisor mode, has unrestricted access to all processor resources.

The integer portion of the user programming model, consisting of 16, general-purpose, 32-bit registers and two control registers, is the same as the user programming model of the TS68030. The TS68040 user programming model also incorporates the TS68882 programming model consisting of eight, floating-point, 80-bit data registers, a floating-point control register, a floating-point status register, and a floating-point instruction address register.

The supervisor programming model is used exclusively by TS68040 system programmers to implement operating system functions, I/O control, and memory management subsystems. This supervisor/user distinction in the TS68000 architecture was carefully planned so that all application software can be written to execute in the nonprivileged user mode and migrate to the TS68040 from any TS68000 platform without modification. Since system software is usually modified by system designers when porting to a new design, the control features are properly placed in the supervisor programming model. For example, the transparent translation registers of the TS68040 can only be read or written by the supervisor software; the programming resources of user application programs are unaffected by the existence of the transparent translation registers

Registers D0-D7 are data registers containing operands for bit and bit field (1- to 32-bit), byte (8-bit), word (16-bit), long-word (32-bit), and quad-word (64-bit) operations. Registers A0-A6 and the stack pointer registers (user, interrupt, and master) are address registers that may be used as software stack pointers or base address registers. Register A7 is the user stack pointer in user mode, and is either the interrupt or master stack pointer (A7’ or A7’’) in supervisor mode. In supervisor mode, the active stack pointer (interrupt or master) is selected based on a bit in the status register (SR). The address registers may be used for word and long-word operations, and all of the 16 general-purpose registers (D0-D7, A0-A7 in Figure 9-1) may be used as index registers.

The eight, 80-bit, floating-point data registers (FP0-FP7) are analogous to the integer data registers (D0-D7) of all TS68000 Family processors. Floating-point data registers always contain extended-precision numbers. All external operands, regardless of the data format, are converted to extended-precision values before being used in any floating-point calculation or stored in a floating-point data register.

The program counter (PC) usually contains the address of the instruction being executed by the TS68040. During instruction execution and exception processing, the processor automatically increments the contents of the PC or places a new value in the PC, as appropriate. The status register (SR in the supervisor programming model) contains the condition codes that reflect the results of a previous operation and can be used for conditional instruction execution in a program. The lower byte of the SR is accessible in user mode as the condition code register (CCR). Access to the upper byte of the SR is restricted to the supervisor mode.

As part of exception processing, the vector number of the exception provides an index into the exception vector table. The base address of the exception vector table is stored in the vector base register (VBR). The displacement of an exception vector is added to the value in the VBR when the TS68040 accesses the vector table during exception processing.

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Alternate function code registers, SFC and DFC (source and destination), contain 3-bit function codes. Function codes can be considered extensions of the 32-bit linear address. Function codes are automatically generated by the processor to select address spaces for data and program accesses at the user and supervisor modes. The alternate function code registers are used by certain instructions to explicitly specify the function codes for various operations. The cache control register (CACR) controls enabling of the on-chip instruction and data caches of the TS68040.

The supervisor root pointer (SRP) and user root pointer (URP) registers point to the root of the address translation table tree to be used for supervisor mode and user mode accesses. The URP is used if FC2 of the logical address is zero, and the SRP is used if FC2 is one.

The translation control register (TC) enables logical-to-physical address translation and selects either 4K or 8K page sizes. As shown in Figure 9-1, there are four transparent translation registers - ITT0 and ITT1 for instruction accesses and DTT0 and DTT1 for data accesses. These registers allow portions of the logical address space to be transparently mapped and accessed without the use of resident descriptors in an ATC. The MMU status register (MMUSR) contains status information from the execution of a PTEST instruction. The PTEST instruction searches the translation tables for the logical address as specified by this instruction's effective address field and the DFC.

The 32-bit floating-point control register (FPCR) contains an exception enable byte that enables disables traps for each class of floating-point exceptions and a mode byte that sets the user-selectable modes. The FPCR can be read or written to by the user and is cleared by a hardware reset or a restore operation of the null state. When cleared, the FPCR provides the IEEE 754 standard defaults. The floating-point status register (FPSR) contains a condition code byte, quotient bits, an exception status byte, and an accrued exception byte. All bits in the FPSR can be read or written by the user. Execution of most floating-point instructions modifies this register.

For the subset of the FPU instructions that generate exception traps, the 32-bit floating-point instruction address register (FPIAR) is loaded with the logical address of an instruction before the instruction is executed. This address can then be used by a floating-point exception handler to locate a floating-point instruction that has caused an exception. The move floating-point data register (FMOVE) instruction (to from the FPCR, FPSR, or FPIAR) and the move multiple data registers (FMOVEN) instruction cannot generate floating-point exceptions; therefore, these instructions do not modify the FPIAR. Thus, the FMOVE and FMOVEM instructions can be used to read the FPIAR in the trap handler without changing the previous value.

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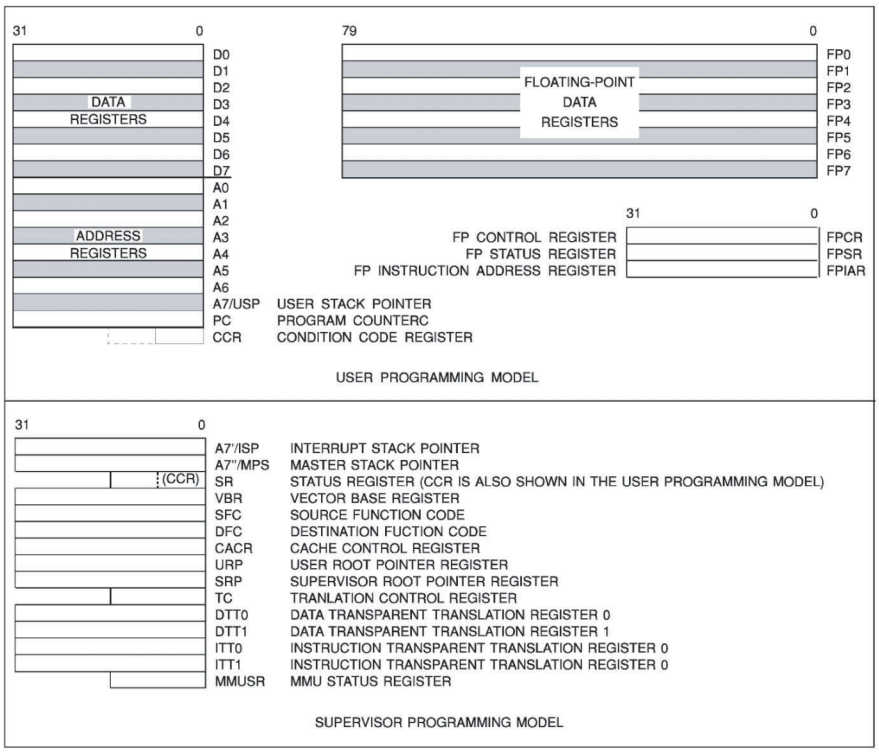
Figure 10-1. Programming Model



10.2 Data Types and Addressing Modes

The TS68040 supports the basic data types shown in Table 9-1. Some data types apply only to the integer unit, some only to the FPU, and some to both the integer unit and the FPU. In addition, the instruction set supports operations on other data types such as memory addresses.

Table 10-1. Data Types

Operand Data Type	Size	Execution Unit (IU[1], FPU)	Notes
Bit	1-bit	IU	
Bit Field	1-32 bits	IU	Field of consecutive bits
BCD	32 bits	IU	Packaged: 2 digits byte Unpacked: 1 digit byte
Byte Integer	8 bits	IU, FPU	
Word Integer	16 bits	IU, FPU	
Long-word Integer	32 bits	IU, FPU	
Quad-word Integer	64 bits	IU	Any two data registers
16-byte	128 bits	IU	Memory-only, aligned 16-byte boundary
Single-precision Real	32 bits	FPU	1-bit sign, 8-bit exponent, 23-bit mantissa
Double-precision Real	64 bits	FPU	1-bit sign, 11-bit exponent, 52-bit mantissa
Extended-precision Real	80 bits	FPU	1-bit sign, 15-bit exponent, 64-bit mantissa

Note: 1. IU = Integer Unit.

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The three integer data formats that are common to both the integer unit and the FPU (byte, word, and long word) are the standard twos-complement data formats defined in the TS68000 Family architecture. Whenever an integer is used in a floating-point operation, the integer is automatically converted by the FPU to an extended-precision floating-point number before being used. The ability to effectively use integers in floating-point operations saves user memory because an integer representation of a number usually requires fewer bits than the equivalent floating-point representation.

Single- and double-precision floating-point data formats are implemented in the FPU as defined by the IEEE standard. These data formats are the main floating-point formats and should be used for most calculations involving real numbers.

The extended-precision data format is also in conformance with the IEEE standard, but the standard does not specify this format to the bit level as it does for single- and double-precision. The memory format for the FPU consists of 96 bits (three long words). Only 80 bits are actually used; the other 16 bits are reserved for future use and for long-word alignment of the floating-point data structures in memory. The extended-precision format has a 15-bit exponent, a 64-bit mantissa, and a 1-bit mantissa sign. Extended-precision numbers are intended for use as temporary variables, intermediate values, or where extra precision is needed.

The TS68040 addressing modes are shown in Table 9-2. The register indirect addressing modes support post-increment, predecrement, offset, and indexing, which are particularly useful for handling data structures common to sophisticated applications and high-level languages. The program counter indirect mode also has indexing and offset capabilities; this addressing mode is typically required to support position-independent software. In addition to these addressing modes, the TS68040 provides index sizing and scaling features that enhance software performance. Data formats are supported orthogonally by all arithmetic operations and by all appropriate addressing modes.

Table 10-2. Addressing Modes

Addressing Modes	Syntax
Register Direct	
Date Register Direct	Dn
Address Register Direct	An
Register Indirect	
Address Register Indirect	(An)
Address Register Indirect With Postincrement	(An)
Address Register Indirect With Predecrement	(An)
Address Register Indirect With Displacement	(d_{16}, An)
Register Indirect With Index	
Address Register Indirect With Index (8-bit Displacement)	(d_8, An, Xn)
Address Register Indirect With Index (Base Displacement)	(bd, An, Xn)
Memory Indirect	
Memory Indirect Postincrement	([bd, An], Xn, od)
Memory Indirect Preindexed	([bd, An, Xn], od)
Program Counter Indirect With Displacement	(d_{16}, PC)
Program Counter Indirect With Index	
PC Indirect With Index (8-bit Displacement)	(d_8, PC, Xn)
PC Indirect With Index (Base Displacement	(bd, PC, Xn)

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Table 10-2. Addressing Modes (Continued)

Addressing Modes	Syntax
Program Counter Memory Indirect	
PC Memory Indirect Postindexed	([bd, PC], Xn, od)
PC Memory Indirect Preindexed	([bd, PC, Xn], od)
Absolute	
Absolute Short	xxx.W
Absolute Long	xxx.L
Immediate	# (data)

Note:

DN = Data register, D0-D7

AN = Address register, A0-A7

d_8, d_{16} = A twos-complement or sign-extended displacement; added as part of the effective address calculation; size is 8 (d_8) or 16 (d_{16}) bits; when omitted, assemblers use a value of zero.

Xn = Address or data register used as an index register; form is Xn, SIZE*SCALE, where SIZE is W or L (indicates index register size) and SCALE is 1, 2, 4 or 8 (index register os multiplied by SCALE); use of SIZE and or SCALE is optional.

bd = A twos-complement base displacement; when present, size can be 16 or 32 bits.

od = Outer displacement added as part of effective address calculation after any memory indirection; use is optional with a size of 16 or 32 bits.

PC = Program counter.

(data) = Immediate value of 8, 16 or 32 bits.

( ) = Effective address.

[ ] = Used as indirect address to long-word address.

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– Instruction Set Overview

The instruction provided by the TS68040 are listed in Table 9-3 on page 34. The instruction set has been tailored to support high-level languages and is optimized for those instructions most commonly executed (however, all instructions listed are fully supported). Many instructions operate on bytes, words, and long words, and most instructions can use any of the addressing modes of Table 9-2 on page 32.

Table 10-3. Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal With Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add With Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left And Right
Bcc	Branch Conditionally
BCHG	Test Bit And Change
BCLR	Test Bit And Clear
BFCHG	Test Bit Field And Change
BFCLR	Test Bit Field And Clear
BFEXTS	Signed Bit Field Extract
BFEXTU	Unsigned Bit Field Extract
BFFFO	Bit Field Find First One
BFINS	Bit Field Insert
BFSET	Test Bit Field And Set
BFTST	Test Bit Field
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit And Set
BSR	Branch To Subroutine
BTST	Test Bit
CAS	Compare And Swap Operands
CAS2	Compare And Swap Dual Operands
CHK	Check Register Against Bounds
CHK2	Check Register Against Upper And Lower Bounds
CINV[(1)]	Invalidate Cache Entries
CLR	Clear
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory To Memory
CMP2	Compare Register Against Upper And Lower Bounds
CPUSH[(1)]	Push Then Invalidate Cache Entries
DB_{CC}	Test Condition, Decrement And Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide

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Table 10-3. Instruction Set Summary (Continued)

Mnemonic	Description
EOR EORI EXG EXT, EXTB	Logical Exclusive OR Logical Exclusive OR Immediate Exchange Registers Sign Extend
ILLEGAL	Take Illegal Instruction Trap
JMP JSR	Jump Jump To Subroutine
LEA LINK LSL, LSR	Load Effective Address Link And Allocate Logical Shift Left And Right
MOVE MOVE16(1) MOVEA MOVE CCR MOVE SR MOVE USP MOVEC(1) MOVEM MOVEP MOVEQ MOVES(1) MULS MULU	Move 16-byte Block Move Move Address Move Condition Code Register Move Status Register Move User Stack Pointer Move Control Register Move Peripheral Move Quick Move Alternate Address Space Move Multiply Signed Multiply Unsigned Multiply
NBCD NEG NEGX NOP NOT	Negate decimal with extend Negate Negate with extend No operation Logical complement
OR ORI	Logical Inclusive OR Logical Inclusive OR Immediate
PACK PEA PFLUSH(1) PTEST(1)	Pack BCD Push Effective Address Flush Entry(ies) In The ATCs Test A Logical Address
RESET ROL, ROR ROXL, ROXR RTD RTE RTR RTS	Reset External Devices Rotate Left And Right Rotate With Extend Left And Right Return And Deallocate Return From Exception Return And Restore Codes Return From Subroutine

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Table 10-3. Instruction Set Summary (Continued)

Mnemonic	Description
SBCD	Substract Decimal With Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract With Extend
SWAP	Swap Register Words
TAS	Test Operand And Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap On Overflow
TST	Trap Operand
UNLK	Unlink
UNPK	Unpack BCD

Note: 1. TS6840 additions or alterations to the TS68030 and TS68881/TS68882 instructions sets.

Table 10-4. Floating-point instructions

Mnemonic	Description
FABS(1)	Floating-point Absolute Value
FADD(1)	Floating-point Add
FBcc	Branch On Floating-point Condition
FCMP	Floating-point Compare
FDBcc	Floating-point Decrement And Branch
FDIV(1)	Floating-point Divide
FMOVE(1)	Move Floating-point Register
FMOVEM	Move Multiple Floating-point Registers
FMUL(1)	Floating-point Multiply
FNEG(1)	Floating-point Negate
FRESTORE	Restore Floating-point Internal State
FSAVE	Save Floating-point Internal State
FScc	Set According To Floating-point Condition
FSQRT(1)	Floating-point Square Root
FSUB(1)	Floating-point Substract
FTRAPcc	Trap On Floating-point Condition
FTST	Floating-point Test

Note: 1. TS6840 additions or alterations to the TS68030 and TS68881/TS68882 instructions sets.

The TS68040 floating-point instructions, a commonly used subset of the TS68882 instruction set, are implemented in hardware. The remaining unimplemented instructions are less frequently used and are efficiently emulated in software, maintaining compatibility with the TS68881/TS68882 floating-point coprocessors.

The TS68040 instruction set includes MOVE16, a new user instruction that allows high-speed transfers of 16-byte blocks between external devices such as memory to memory or coprocessor to memory.

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10.3 Instruction and Data Caches

Studies have shown that typical programs spend much of their execution time in a few main routines or tight loops. Earlier members of the TS68000 Family took advantage of this locality of reference phenomenon to varying degrees. The TS68040 takes further advantage of cache technology with its two, independent, on-chip, physical address space caches, one for instructions and one for data. The caches reduce the processor's external bus activity and increase CPU throughput by lowering the effective memory access time. For a typical system design, the large caches of the TS68040 yield a very high hit rate, providing a substantial increase in system performance. Additionally, the caches are automatically burstfilled from the external bus whenever a cache miss occurs.

The autonomous nature of the caches allows instruction-stream fetches, data-stream fetches, and a third external access to occur simultaneously with instruction execution. For example, if the TS68040 requires both an instruction-stream access and an external peripheral access and if the instruction is resident in the on-chip cache, the peripheral access proceeds unimpeded rather than being queued behind the instruction fetch. If a data operand is also required and if it is resident in the data cache, it can also be accessed without hindering either the instruction access from its cache or the peripheral access external to the chip. The parallelism inherent in the TS68040 also allows multiple instructions that do not require any external accesses to execute concurrently while the processor is performing an external access for a previous instruction.

10.3.1 Cache Organization

The instruction and data caches are four-way set-associative with 64 sets of four, 16-byte lines for a total cache storage of 4K bytes each. As shown in Figure 9-2, each 16-byte line contains an address tag and state information. State information for each entry consists of a valid flag for the entire line in both instruction and data caches and write status for each long word in the data cache. The write status in the data cache signifies whether or not the long-word data is dirty (meaning that the data in the cache has been modified but has not been written back to external memory) for data in copyback pages.

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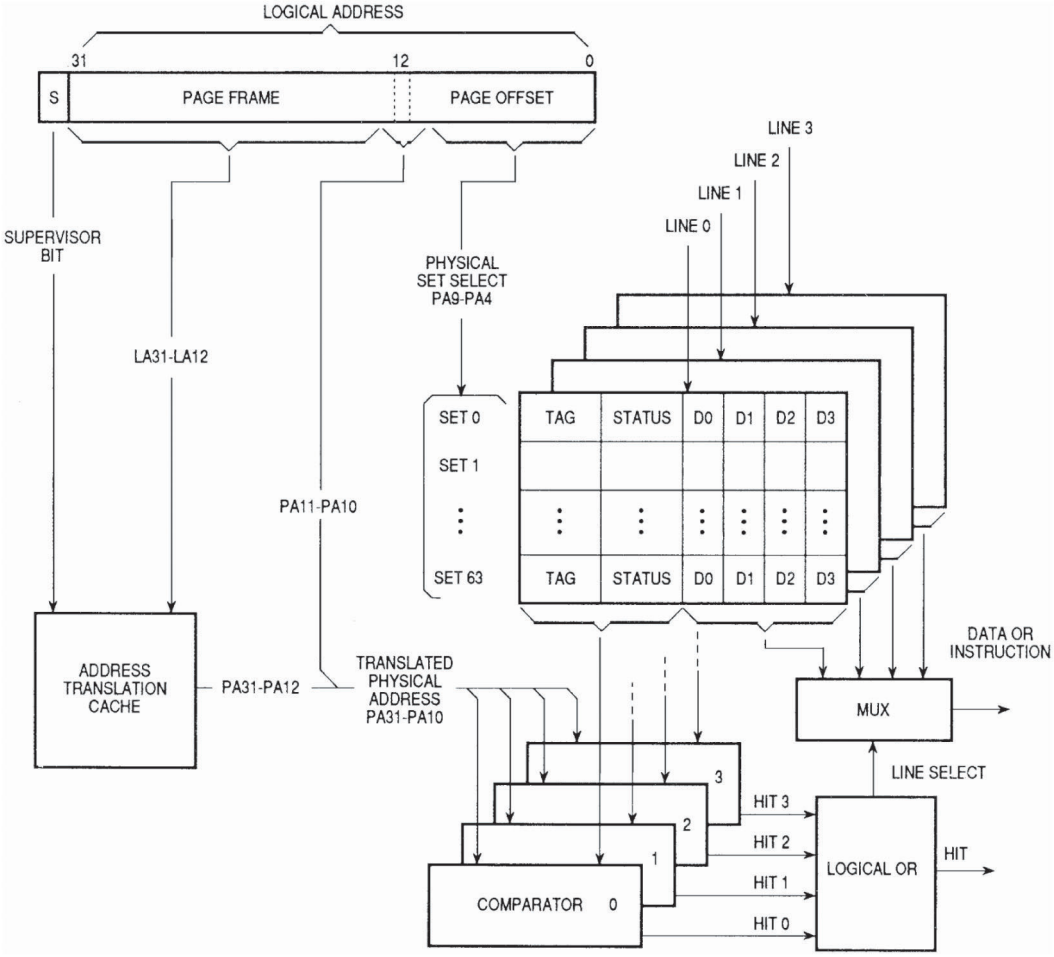
Figure 10-2. Cache Organization Overview



The caches are accessed by physical addresses from the on-chip MMUs. The translation of the upper bits of the logical address occurs concurrently with the accesses into the set array in the cache by the lower address bits. The output of the ATC is compared with the tag field in the cache to determine if one of the lines in the selected set matches the translated physical address. If the tag matches and the entry is valid, then the cache has a hit.

If the cache hits and the access is a read, the appropriate long word from the cache line is multiplexed onto the appropriate internal bus. If the cache hits and the access is a write, the data, regardless of size, is written to the appropriate portion of the corresponding longword entry in the cache.

When a data cache miss occurs and a previously valid cache line is needed to cache the new line, any dirty data in the old line will be internally buffered and copied back to memory after the new cache line has been loaded.

Pushing of dirty data can be forced by the CPUSH instruction.

Cachability of data in each memory page is controlled by two bits in the page descriptor for each page. Cachable pages may be either write through or copyback, with no write-allocate for misses to write through pages. Non-cachable pages may also be specified as non-cachable I/O, forcing accesses to these pages to occur in order of instruction execution.

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10.3.2 Cache Coherency

The TS68040 has the ability to snoop the external bus during accesses by other bus masters to maintain coherency between the TS68040's caches and external memory systems. External write cycles are snooped by both the instruction cache and data cache; whereas, external read cycles are snooped only by the data cache. In addition, external cycles can be flagged on the bus as snoopable or non snoopable. When an external cycle is marked as snoopable, the bus snooper checks the caches for a coherency conflict based on the state of the corresponding cache line and the type of external cycle.

Although the internal execution units and the bus snooper circuit all have access to the on-chip caches, the snooper has priority over the execution units to allow the snooper to resolve coherency discrepancies immediately.

10.3.3 Cache Instructions

The TS68040 supports the following instructions for cache maintenance. Both instructions may selectively operate on the data or instruction cache.

CINV: Invalidates a single line, all lines in a physical page, or the entire cache.

CPUSH: Pushes selected dirty data cache lines to memory, then invalidates all selected lines.

10.4 Operand Transfer Mechanisms

The TS68040 external synchronous bus supports multiple masters and overlaps arbitration with data transfers. The bus is optimized to perform high-speed transfers to and from an external cache or memory. The data and address buses are each 32 bits wide.

10.4.1 Transfer Types

The TS68040 provides two signals (TT1-TT0) that define four types of bus transfers: normal access, MOVE16 access, alternate access, and interrupt acknowledge access. Normal accesses identify normal memory references: MOVE16 accesses are memory accesses by a MOVE16 instruction; and alternate accesses identify accesses to the undefined address spaces (function code values of 0, 3, 4, 7). The interrupt acknowledge access is used to fetch an interrupt vector during interrupt exception processing.

10.4.2 Burst Transfer Operation

During burst read write to cache transfers, the values on the address and transfer type signals do not change; they are the address of the first requested item of the cache line. When the TS68040 request a burst read transfer of a cache line, the address bus indicates the address of the long word in the line needed first, but the memory system is expected to provide data in the following order (modulo 4): 0, 1, 2, 3 (long-word offsets). The first address needed may not be from offset 0; nevertheless, all four long words must be transferred. Burst writes occur in a similar manner.

10.4.3 Bus Snooping

Bus snooping ensures that data in main memory is consistent with data in the on-chip caches. If an alternate bus master is performing a read transfer on the bus and snooping is enabled, and if the snoop logic determines that the on-chip data cache has dirty data (data valid but not consistent with memory) for this transfer, the memory is prevented from responding to the read request, and the TS68040 supplies the data directly to the master. If the alternate master is performing a write transfer on the bus and snooping is enabled, and if the snooper determines that one of the on-chip caches has a valid line for this request, then the snooper may either invalidate or update the line as selected by the snoop control signals.

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10.5 Exception Processing

The TS68040 provides the same extensions to the exception stacking process as the TS68030. If the M bit in the status register is set, the master stack pointer is used for all task-related exceptions. When a nontask-related exception occurs (i.e., an interrupt), the M bit is cleared, and the interrupt stack pointer is used. This feature allows a task's stack area to be carried within a single processor control block, and new tasks may be initiated by simply reloading the master stack pointer and setting the M bit.

The externally generated exceptions are interrupts, bus errors, and reset conditions. The interrupts are requests from external devices for processor action; whereas, the bus error and reset signals are used for access control and processor initialization. The internally generated exceptions come from instructions, address errors, tracing, or breakpoints. The TRAP, TRAPcc, TRAPVcc, FTRAPcc, CHK, CHK2, and DIV instructions can all generate exceptions as part of their instruction execution. Tracing behaves like a very high-priority, internally generated interrupt whenever it is processed. The other internally generated exceptions are caused by unimplemented floating-point instructions, illegal instructions, instruction fetches from odd addresses, and privilege violations. Finally, the MMU can generate exceptions, for access violations and for when invalid descriptors are encountered during table searches.

Exception processing for the TS68040 occurs on the following sequence:

1. an internal copy is made of the status register,
2. the vector number of the exception is determined,
3. current processor status is saved,
4. the exception vector offset is determined by multiplying the vector number by four.

This offset is then added to the contents of the VBR to determine the memory address of the exception vector. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

10.6 Memory Management Units

The full addressing range of the TS68040 is 4G bytes (4,294,967,296 bytes). However, most TS68040 systems implement a much smaller physical memory. Nonetheless, by using virtual memory techniques, the system can be made to appear to have a full 4G bytes of physical memory available to each user program. The independent instruction and data MMUs fully support demand paged virtual-memory operating systems with either 4K or 8K page sizes. In addition to its main function of memory management, each MMU protects supervisor areas from accesses by user programs and also provides write protection on a page-by-page basis. For maximum efficiency, each MMU operates in parallel with other processor activities.

10.6.1 Translation Mechanism

Because logical-to-physical address translation is one of the most frequently executed operations of the TS68040 MMUs, this task has been optimized. Each MMU initiates address translation by searching for a descriptor containing the address translation information in the ATC. If the descriptor does not reside in the ATC, then the MMU performs external bus cycles via the bus controller to search the translation tables in physical memory. After being located, the page descriptor is loaded into the ATC, and the address is correctly translated for the access, provided no exception conditions are encountered.

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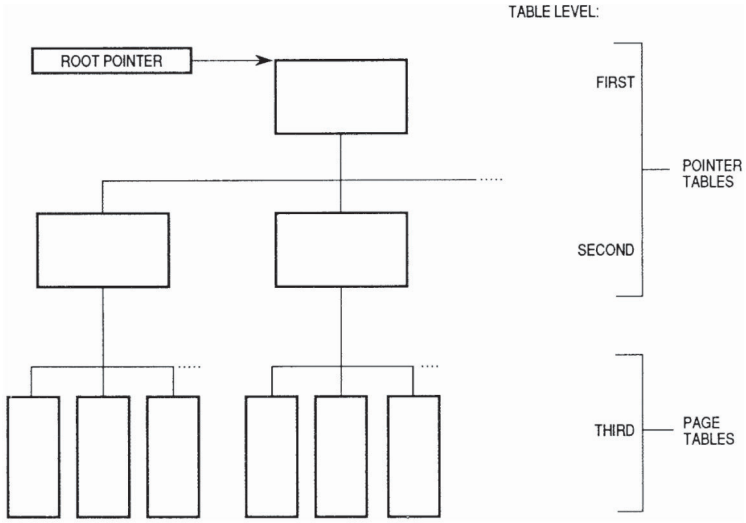
10.6.2 Address Translation Cache

An integral part of the translation function previously described is the dual cache memory that stores recently used logical-to-physical address translation information (page descriptors) for instruction and date accesses. These caches are 64-entry, four-way, set associative. Each ATC compare the logical address of the incoming access against its entries. If one of the entries matches, there is a hit, and the ATC sends the physical address to the bus controller, which then starts the external bus cycle (provided there was no hit in the corresponding cache for the access).

10.6.3 Translation Tables

The translation tables of the TS68040 have a three level tree structure and reside in main memory. Since only a portion of the complete tree needs to exist at any one time, the tree structure minimizes the amount of memory necessary to set up the tables for most programs. As shown in Figure 9-1, either the user root pointer or the supervisor root pointer points to the first level table, depending on the values of the function code for an access. Table entries at the second level of the tree (pointer tables) contain pointers to the third level (page tables). Entries in the page tables contain either page descriptors or indirect pointers to page descriptors. The mechanism for performing table search operations uses portions of the logical address (as indices) at each level of the search. All addresses in the translation table entries are physical addresses.

Figure 10-3. Translation Table Structure



There are two variations of table searches for both 4K and 8K page sizes: normal searches and indirect searches. An indirect search differs in that the entry in the third level page table contains a pointer to a page descriptor rather than the page descriptor itself.

Entries in the translation tables contain control and status information on addition to the physical address information. Control bits specify write protection, limit access to supervisor only, and determine cachability of data in each memory page. Each page descriptor also has two user-programmable bits that appear on the UPA0 and UPA1 signals during an external access for use as address modifier bits.

A global bit can be set in each page descriptor to prevent flushing of the ATC entry for that page by some PFLUSH instruction variants, allowing system ATC entries to remain resident during task swaps. If these special PFLUSH instructions are not used, this bit can be user defined. The MMUs automatically maintain access history information for the pages by updating the used (U) and modified (M) status bits.

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10.6.4 MMU Instructions

The MMU instructions supported by the TS68040 are as follows:

PFLUSH: Allows flushing of either selected ATC entries by function code and logical address or the entire ATCs.

PTEST: Takes an address and function code and searches the translation tables for the corresponding entry, which is then loaded into the ATC. The results of the search are available in the MMU status register and are often useful in determining the cause of a fault.

All of the TS68040 MMU instructions are privileged and can only be executed from the supervisor mode.

10.6.5 Transparent Translation

Four transparent translation registers, two each for instruction and data accesses, have been provided on the TS68040 MMU to allow portions of the logical address space to be transparently mapped and accessed without the need for corresponding entries resident in the ATC. Each register can be used to define a range of logical addresses from 16M bytes to 4G bytes with a base address and a mask. All addresses within these ranges are not mapped, and are optionally protected against user or supervisor accesses and write accesses. Logical addresses in these areas become the physical addresses for memory access. The transparent translation feature allows rapid movement of large blocks of data in memory or I/O space without disturbing the context of the on-chip ATCs or incurring delays associated with translation table searches.

11. Preparation For Delivery

11.1 Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or e2v standard.

11.2 Certificate of Compliance

e2v offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or e2v standard and guarantying the parameters not tested at temperature extremes for the entire temperature range.

12. Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50 percent if practical.

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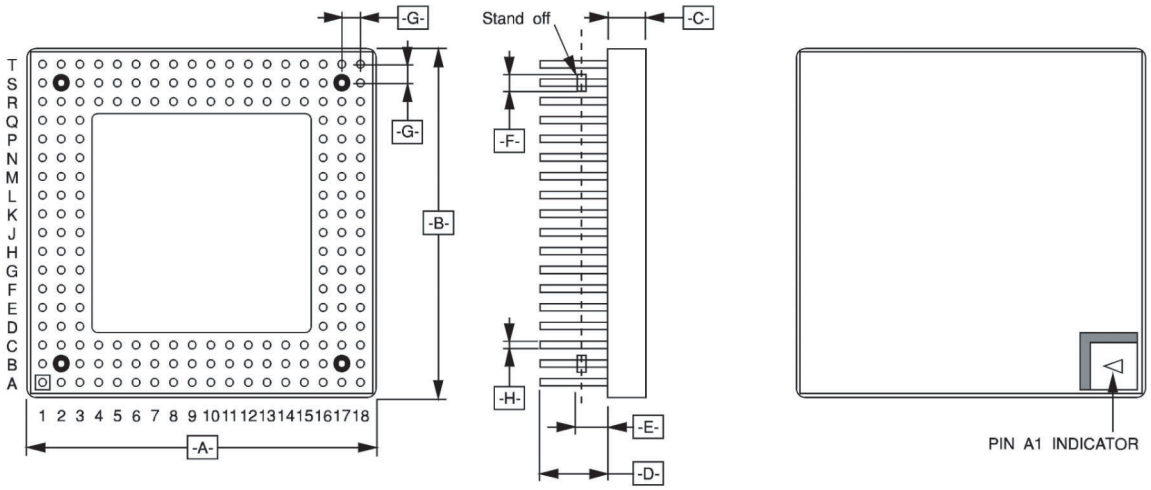
13. Package Mechanical Data

13.1 179 pins – PGA



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	46.863	47.625	1.845	1.875
B	46.863	47.625	1.845	1.875
C	2.3876	1.875	0.094	0.116
D	4.318	4.826	0.170	0.190
E	1.143	1.4	0.045	0.055
F	1.143	1.4	0.045	0.055
G	2.54 BSC		0.100 BSC	
H[(1)]	0.432	0.483	0.017	0.019

Note: 1. For untinned leads (gold)

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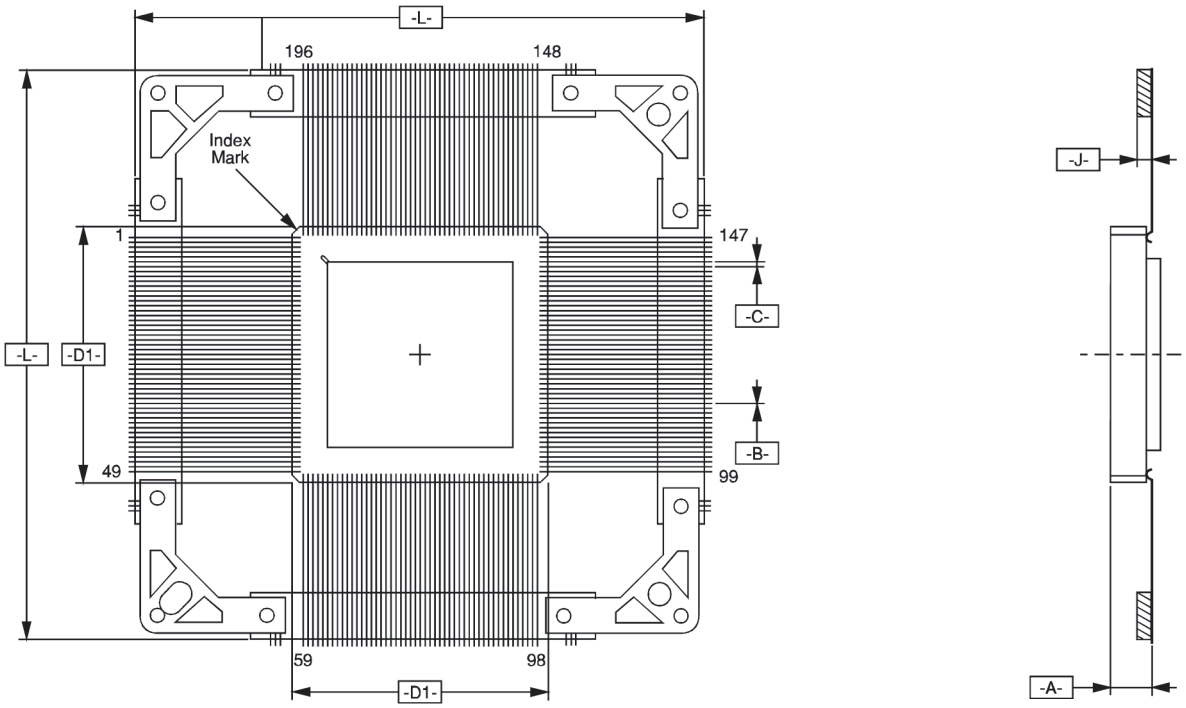
13.2 196 pins – Tie Bar CQFP Cavity Up (on request)



Dim	Millimeters	Inches
A	3.30 max	0.130 max
B	0.23 +0.05 0.23 -0.038	0.009 +0.002 0.009 -0.015
C	0.635 typ.	.025 typ.
D1	33.91 ± 0.25	1.335 ± 0.01
J	0.89 ± 0.13	0.035 ± 0.005
L	63.5 ± 0.51	2.5 ± 0.02

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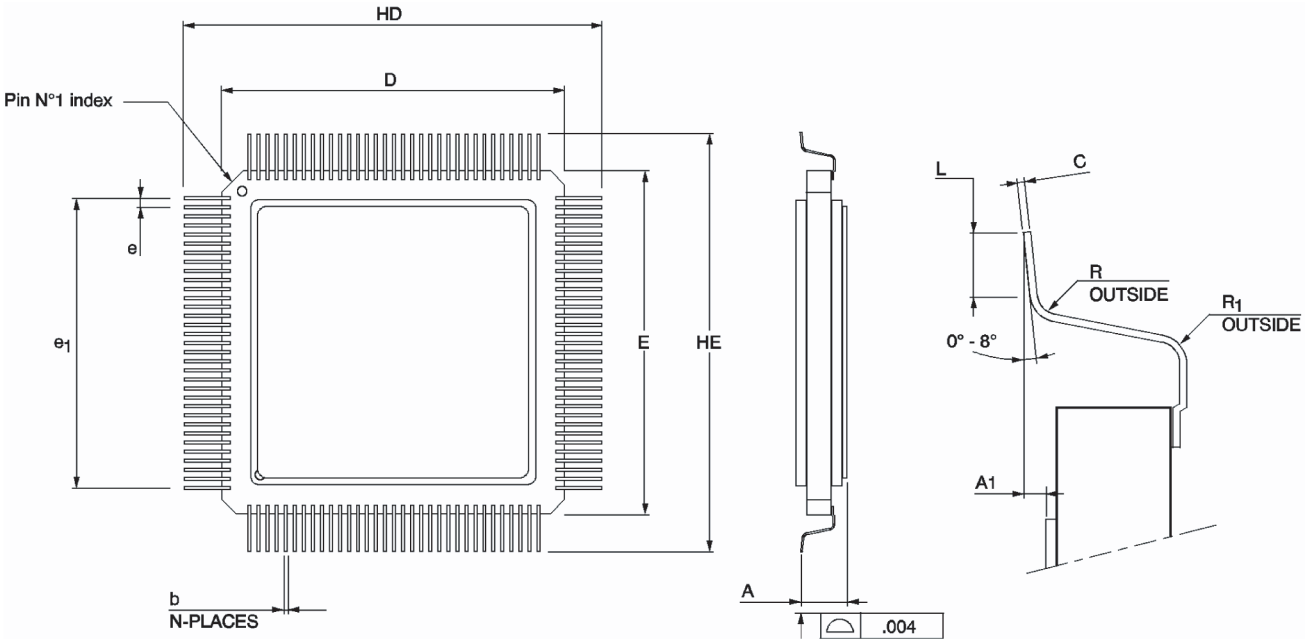
13.3 196 pins – Gullwing CQFP cavity up



* Reduce pin count shown for clarity, 49 pins per side

Symbol	Millimeters	Inches
A	4.19 max	0.165 max
A1	0.673 ± 0.2	.0265 ±.008
b	0.23 +0.05 0.23 -0.038	.009 +.002 .009 -.0015
c	0.127 +0.05 0.127 -0.025	.005 +.002 .005 -.001
D/E	33.91 ±0.25	1.335 ±.01
e	.635 BSC	.025 BSC
e1	30.48 ±0.13	1.2 ±.005
HD/HE	38.8 ±0.18	1.528 ±.007
L	0.813 ±0.2	.032 ±.008
N	196	196
R	0.55 ±0.25	.022 ±.01
R1	0.23 min	.009 min

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14. Ordering Information

14.1 MIL-STD-883 C and Internal Standard

TS 68040 x xx y x nnn A

Product Code (1)	Part Identifier	Temperature Range (1)	Package (1)	Lead finish	Screening Level	Operating Frequency	Revision Level (1)
TS(X)(2)	68040	M: Tc = -55; T_J = +125˚C V: Tc = -40; T_J = +110˚C	F: CQFP/Gullwing leads R: PGA FT: CQFP Flat tie-bar	1: Hot solder dip(1) Blank: Gold	BC: QML class Q Blank: Internal standard	25: 25 MHz 33: 33 MHz	A

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

Table 14-1. Standard Microcircuit Drawing (SMD) Cross-Reference

e2v Orderable Part-Number	Standard Microcircuit Drawing (SMD) Number	Standard	Package	Lead-Finish	Temperature	Frequency (MHz)
TS68040MRB/C25A	5962-9314301MXC	MIL-PRF-38535	PGA 179	Gold	-55°C/+125°C	25
TS68040MRB/C33A	5962-9314302MXC	MIL-PRF-38535	PGA 179	Gold	-55°C/+125°C	33
TS68040MR1B/C25A	5962-9314301MXA	MIL-PRF-38535	PGA 179	Sn63Pb37	-55°C/+125°C	25
TS68040MR1BC33A	5962-9314302MXA	MIL-PRF-38535	PGA 179	Sn63Pb37	-55°C/+125°C	33
TS68040MFTBC25A	5962-9314301MYC	MIL-PRF-38535	CQFP 196 Flat+ Tie-Bar	Gold	-55°C/+125°C	25
TS68040MFTBC33A	5962-9314302MYC	MIL-PRF-38535	CQFP 196 Flat+ Tie-Bar	Gold	-55°C/+125°C	33
TS68040MFB/C25A	5962-9314301MZC	MIL-PRF-38535	CQFP 196	Gold	-55°C/+125°C	25
TS68040MFB/C33A	5962-9314302MZC	MIL-PRF-38535	CQFP 196	Gold	-55°C/+125°C	33
TS68040MF1B/C25A	5962-9314301MZA	MIL-PRF-38535	CQFP 196	Sn63Pb37	-55°C/+125°C	25
TS68040MF1B/C33A	5962-9314302MZA	MIL-PRF-38535	CQFP 196	Sn63Pb37	-55°C/+125°C	33

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15. Document Revision History

Table 14-1 provides a revision history for this hardware specification.

Table 15-1. Document Revision History

Revision Number	Date	Substantive Change(s)
B	04/2007	Name change from Atmel to e2v Ordering information update
A	09/2002	Initial revision

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