REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct title to accurately describe the device function. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG	06-07-31	Thomas M. Hess
B	Correct footnote 4 in table I. - LTG	07-01-24	Thomas M. Hess

REV																			
SHEET																			
REV	A	A	A	A															
SHEET	15	16	16	17															

REV STATUS	REV	B	A	A	A	A	A	A	B	A	A	A	A	A	A	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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92-04-07

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, 8-BIT DIAGNOSTIC REGISTER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

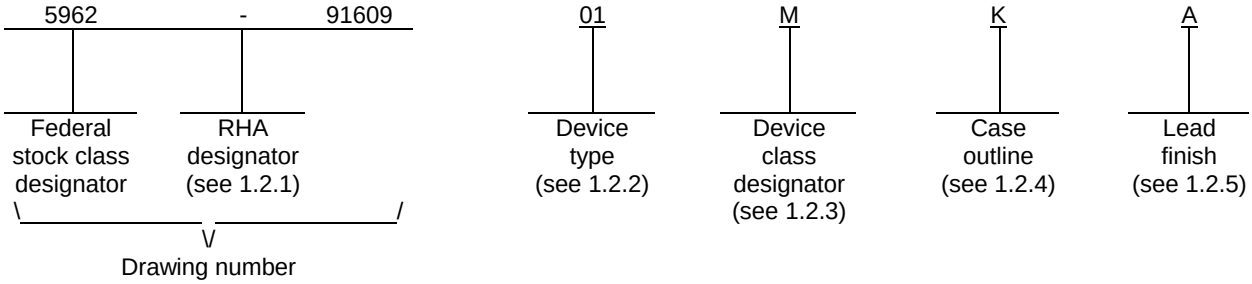
SIZE	CAGE CODE	
A	**67268**	**5962-91609**

SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT818	8-bit diagnostic register with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ±20 mA
DC output current (I_{OUT}) (per pin) ..... ±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) (per pin) ..... ±450 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C 3/

1.4 Recommended operating conditions. 2/ 4/

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall times:
  V_{CC} = 4.5 V, 5.5 V ..... 8 ns/V
Minimum setup time, Dn to PCLK (t_{s1}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 4.0 ns
  T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 6.0 ns
Minimum setup time, MODE to PCLK (t_{s2}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 4.5 ns
  T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 6.0 ns
Minimum setup time, Yn to DCLK (t_{s3}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 2.5 ns
  T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 2.5 ns
Minimum setup time, MODE to DCLK (t_{s4}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 4.0 ns
  T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 4.5 ns
Minimum setup time, SDI to DCLK (t_{s5}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 3.5 ns
  T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 4.5 ns
Minimum setup time, DCLK to PCLK (t_{s6}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 9.0 ns
  T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 11.5 ns
Minimum setup time, PCLK to DCLK (t_{s7}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 11.0 ns
  T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 12.5 ns
Minimum hold time, Dn to PCLK (t_{h1}):
  T_C = +25°C, V_{CC} = 4.5 V ..... 1.0 ns
  T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 1.0 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to GND.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.
4/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

1.4 Recommended operating conditions – Continued. 2/ 4/

Minimum hold time, MODE to PCLK (t_{h2}):
T_C = +25°C, V_{CC} = 4.5 V ..... 0.0 ns
T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 0.0 ns
Minimum hold time, Yn to DCLK (t_{h3}):
T_C = +25°C, V_{CC} = 4.5 V ..... 1.0 ns
T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 1.5 ns
Minimum hold time, MODE to DCLK (t_{h4}):
T_C = +25°C, V_{CC} = 4.5 V ..... 1.0 ns
T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 1.0 ns
Minimum hold time, SDI to DCLK (t_{h5}):
T_C = +25°C, V_{CC} = 4.5 V ..... 1.0 ns
T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 1.0 ns
Minimum PCLK pulse width, high, low (t_{w1}):
T_C = +25°C, V_{CC} = 4.5 V ..... 3.0 ns
T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 3.5 ns
Minimum DCLK pulse width, high, low (t_{w2}):
T_C = +25°C, V_{CC} = 4.5 V ..... 3.0 ns
T_C = -55°C, +125°C, V_{CC} = 4.5 V ..... 3.0 ns
Maximum clock frequency (f_{MAX}):
T_C = +25°C, -55°C, +125°C, V_{CC} = 4.5 V ..... 100 MHz
T_C = +25°C, -55°C, +125°C, V_{CC} = 4.5 V ..... 100 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage, Y0-Y7 outputs 1/	V_{OH1}	$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OH} = -50\ \mu A$	$V_{CC} = 4.5\ V$	1, 2, 3	All	4.4		V
			$V_{CC} = 5.5\ V$			5.4		
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OH} = -24\ mA$	$V_{CC} = 4.5\ V$			3.7		
			$V_{CC} = 5.5\ V$			4.7		
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OH} = -50\ mA$	$V_{CC} = 5.5\ V$			3.85		
High level output voltage D0-D7, SDO outputs 1/	V_{OH2}	$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OH} = -8\ mA$	$V_{CC} = 4.5\ V$	1, 2, 3	All	3.7		V
			$V_{CC} = 5.5\ V$			4.7		
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OH} = -32\ mA$	$V_{CC} = 5.5\ V$			3.85		
Low level output voltage, Y0-Y7 outputs 1/	V_{OL1}	$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OL} = 50\ \mu A$	$V_{CC} = 4.5\ V$	1, 2, 3	All		0.1	V
			$V_{CC} = 5.5\ V$				0.1	
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OL} = 24\ mA$	$V_{CC} = 4.5\ V$				0.5	
			$V_{CC} = 5.5\ V$				0.5	
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OL} = 50\ mA$	$V_{CC} = 5.5\ V$				1.65	
Low level output voltage D0-D7, SDO outputs 1/	V_{OL2}	$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OL} = 8\ mA$	$V_{CC} = 4.5\ V$	1, 2, 3	All		0.5	V
			$V_{CC} = 5.5\ V$				0.5	
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OL} = 32\ mA$	$V_{CC} = 5.5\ V$				1.65	
High level input voltage 2/	V_{IH}		$V_{CC} = 4.5\ V$	1, 2, 3	All	2.0		V
			$V_{CC} = 5.5\ V$			2.0		
Low level input voltage 2/	V_{IL}		$V_{CC} = 4.5\ V$	1, 2, 3	All		0.8	V
			$V_{CC} = 5.5\ V$				0.8	
Input leakage current low, SDI, DCLK, MODE, PCLK, $\overline{OEY}$	I_{IL}	$V_{IN} = 0.0\ V$	$V_{CC} = 5.5\ V$	1, 2, 3	All		-10.0	µA
Input leakage current high, SDI, DCLK, MODE, PCLK, $\overline{OEY}$	I_{IH}	$V_{IN} = 5.5\ V$					10.0	µA
Quiescent supply current, output high	I_{CCH}	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5\ V$		1, 2, 3	All		160	µA
Quiescent supply current, output low	I_{CCL}						160	µA
Quiescent supply current, output three-state	I_{CCZ}						160	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Maximum I_{CC}/input current SDI, Dn, DCLK, MODE, OEY 3/	ΔI_{CC}	V_{CC} = 5.5 V, V_{IL} = 0.0 V $V_{IH} = V_{CC} - 2.1$ V		1, 2, 3	All		1.6	mA
Three-state output leakage current, Dn, Yn, high	I_{OZH}	$\overline{OEY} = V_{IH}$ min or V_{IL} max V_{OUT} = 5.5 V, V_{CC} = 5.5 V All other inputs = V_{CC} or GND		1, 2, 3	All		+10.0	µA
Three-state output leakage current, Dn, Yn, low	I_{OZL}	$\overline{OEY} = V_{IH}$ min or V_{IL} max V_{OUT} = 0.0 V, V_{CC} = 5.5 V All other inputs = V_{CC} or GND					-10.0	
Input capacitance	C_{IN}	See 4.3.1c		4	All		8.0	pF
Output capacitance	C_{OUT}	See 4.3.1c		4	All		15.0	pF
Input/output capacitance	C_{IO}	See 4.3.1c		4	All		15.0	pF
Power dissipation capacitance 4/	C_{PD}	See 4.3.1c		4	All		110	pF
Functional tests		Tested at V_{CC} = 4.5 V and repeated at V_{CC} = 5.5 V For all inputs V_{IN} = 2.4 V or 0.4 V See 4.3.1d		7, 8	All			
Propagation delay time, PCLK to Yn 5/	t_{PHL1}	C_L = 50 pF minimum R_L = 500Ω See figure 4	V_{CC} = 4.5 V	9	All	1.0	8.0	ns
				10, 11		1.0	10.0	
	t_{PLH1}		V_{CC} = 4.5 V	9		1.0	8.5	
				10, 11		1.0	10.0	
Propagation delay time, MODE to SDO 5/	t_{PHL2}		V_{CC} = 4.5 V	9	All	1.0	10.0	ns
				10, 11		1.0	12.0	
	t_{PLH2}		V_{CC} = 4.5 V	9		1.0	11.0	
				10, 11		1.0	13.5	
Propagation delay time, SDI to SDO 5/	t_{PHL3}		V_{CC} = 4.5 V	9	All	1.0	9.5	ns
				10, 11		1.0	11.5	
	t_{PLH3}		V_{CC} = 4.5 V	9		1.0	10.0	
				10, 11		1.0	12.0	
Propagation delay time, DCLK to SDO 5/	t_{PHL4}		V_{CC} = 4.5 V	9	All	1.0	11.5	ns
				10, 11		1.0	14.0	
	t_{PLH4}		V_{CC} = 4.5 V	9		1.0	12.0	
				10, 11		1.0	15.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, output enable, $\overline{OEY}$ to Yn 5/	t_{PZH1}	C_L = 50 pF minimum R_L = 500Ω See figure 4	V_{CC} = 4.5 V	9	All	1.0	9.5	ns
				10, 11		1.0	11.0	
	t_{PZL1}		V_{CC} = 4.5 V	9		1.0	10.5	
				10, 11		1.0	12.0	
Propagation delay time, output disable, $\overline{OEY}$ to Yn 5/	t_{PHZ1}		V_{CC} = 4.5 V	9	All	1.0	10.5	ns
				10, 11		1.0	12.0	
	t_{PLZ1}		V_{CC} = 4.5 V	9		1.0	8.5	
				10, 11		1.0	10.0	
Propagation delay time, output enable, DCLK to Dn 5/	t_{PZH2}		V_{CC} = 4.5 V	9	All	1.0	11.0	ns
				10, 11		1.0	13.5	
	t_{PZL2}		V_{CC} = 4.5 V	9		1.0	11.5	
				10, 11		1.0	14.0	
Propagation delay time, output disable, DCLK to Dn 5/	t_{PHZ2}		V_{CC} = 4.5 V	9	All	1.0	12.0	ns
				10, 11		1.0	13.5	
	t_{PLZ2}		V_{CC} = 4.5 V	9		1.0	10.5	
				10, 11		1.0	12.0	

1/ V_{OH} and V_{OL} tests will be tested at V_{CC} = 4.5 V. All other voltages are guaranteed, but not tested. Limits shown apply to operation at V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

2/ V_{IH} and V_{IL} tests are guaranteed by the V_{OH} and V_{OL} tests.

3/ ΔI_{CC} (max)/pin ≤ 1.6 mA (preferred method), or ΔI_{CC}/package ≤ 1.6 mA x the number of input pins/package where ΔI_{CC} (max)/data pin ≤ 1.6 mA and ΔI_{CC} (max)/control pin ≤ 3.0 mA (alternate method).

4/ Power dissipation capacitance (C_{PD}) determines both the dynamic power consumption (P_D) and the dynamic current consumption (I_S). Where:
$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$
$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$
For both P_D and I_S, n is number of device inputs at TTL levels; f is the frequency of the input signal; d is duty cycle of the input signal; and C_L is the external output load capacitance.

5/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns.

Device type	All	
Case outlines	K and L	3
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{OEY}$	NC
2	DCLK	$\overline{OEY}$
3	D0	DCLK
4	D1	D0
5	D2	D1
6	D3	D2
7	D4	D3
8	D5	NC
9	D6	D4
10	D7	D5
11	SDI	D6
12	GND	D7
13	PCLK	SDI
14	SDO	GND
15	Y7	NC
16	Y6	PCLK
17	Y5	SDO
18	Y4	Y7
19	Y3	Y6
20	Y2	Y5
21	Y1	Y4
22	Y0	NC
23	MODE	Y3
24	V_{CC}	Y2
25	---	Y1
26	---	Y0
27	---	MODE
28	---	V_{CC}

NC = No connection

Terminal symbol	Description
D0 – D7	Data inputs
Y0 – Y7	Data outputs
$\overline{OEY}$	Output enable input
MODE	Control input
SDI	Serial data input
DCLK	Diagnostics clock
PCLK	Pipeline register clock
SDO	Serial data output

FIGURE 1. Terminal connections.

Inputs				Outputs			Operation
SDI	MODE	DCLK	PCLK	SDO	Diagnostic register	Pipeline register	
X	L	↑	X	S7	S1<S1 – 1, S0<SDI	N/A	Serial shift; D7-D0 disabled
X	L	X	↑	S7	N/A	P1<D1	Normal load pipeline register
L	H	↑	X	L	S1<Y1	N/A	Load diagnostic register from Y; D1 disabled
X	H	X	↑	SDI	N/A	P1<S1	Load pipeline register from diagnostic register
H	H	↑	X	H	Hold	N/A	Hold diagnostic register; D1 enabled

H = High voltage level
L = Low voltage level
↑ = Low-to-high clock transition
X = Irrelevant

FIGURE 2. Truth table.

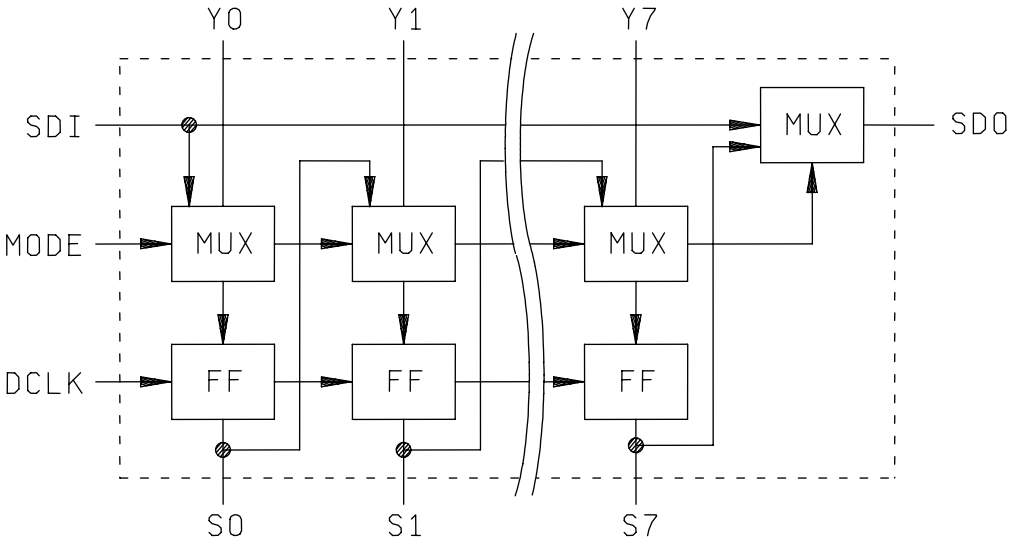


FIGURE 3. Block diagram.

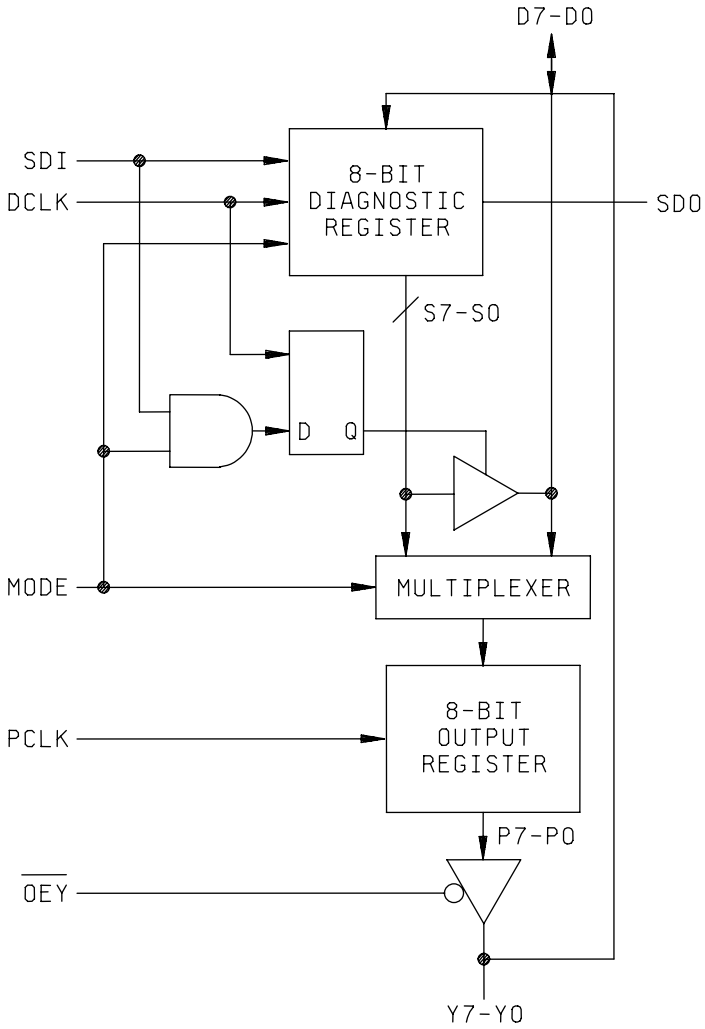


FIGURE 3. Block diagram – Continued.

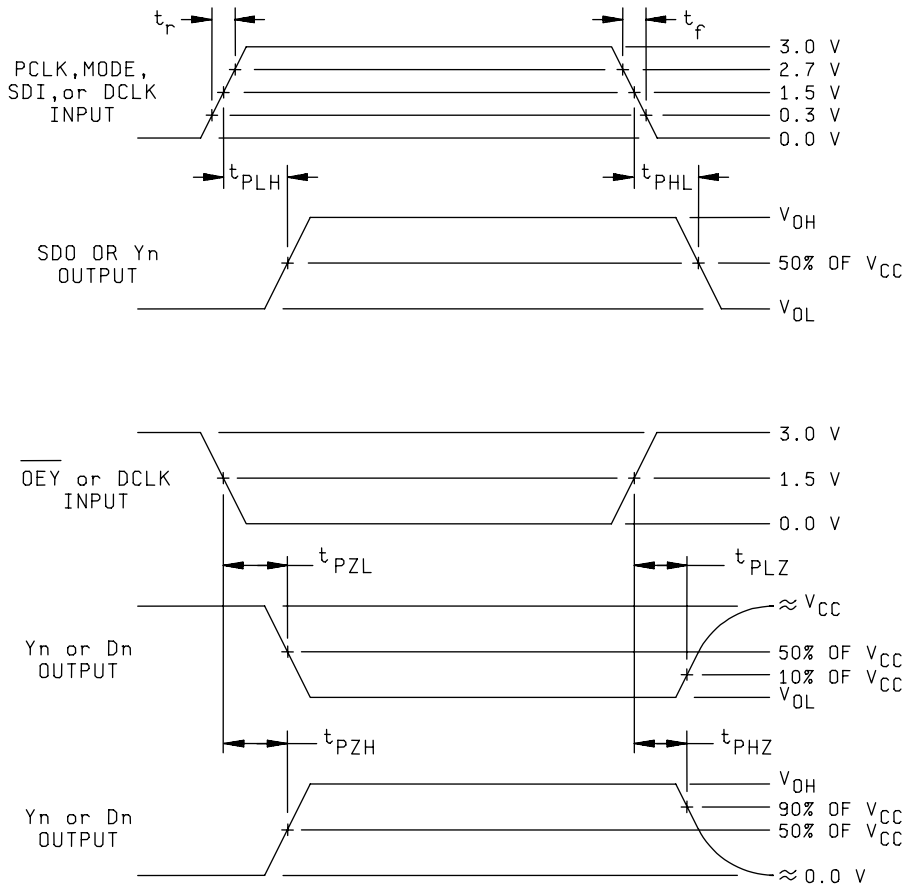
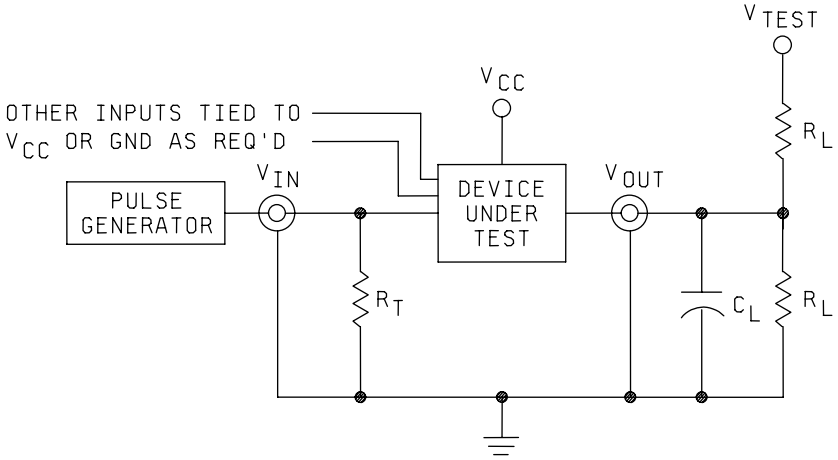


FIGURE 4. Switching waveforms and test circuit.



NOTES:

1. When measuring t_{PLZ} and t_{PZL}: $V_{TEST} = 2 \times V_{CC}$.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL};
   the preferred method is: V_{TEST} = GND for (t_{PHZ} and t_{PZH}) and open for (t_{PLH} and t_{PHL}),
   the alternate method is: V_{TEST} = Open for (t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}).
3. The t_{PZL} and t t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent; R_T = 50Ω or equivalent.
6. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; $t_r \leq 3.0$ ns; $t_f \leq 3.0$ ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
7. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
8. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, $C_{IN/OUT}$, and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with zero failures.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table as specified on figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-01-24

Approved sources of supply for SMD 5962-91609 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9160901MKA	0C7V7	54ACT818FMQB
5962-9160901MLA	0C7V7	54ACT818SDMQB
5962-9160901M3A	0C7V7	54ACT818LMQB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.