REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. - CFS	06-06-15	Thomas M. Hess

REV	A	A	A	A	A	A														
SHEET	35	36	37	38	39	40														
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
93-05-19

REVISION LEVEL
A

MICROCIRCUIT, DIGITAL, CMOS, UNIVERSAL SERIAL CONTROLLER, MONOLITHIC SILICON

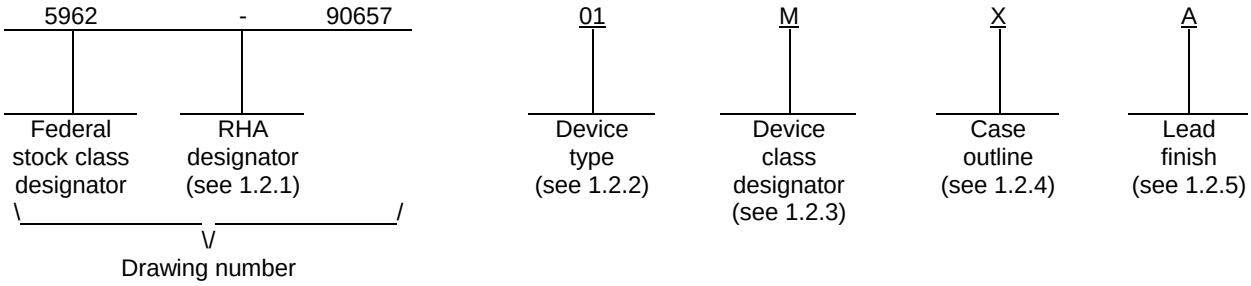
SIZE	CAGE CODE	
A	**67268**	**5962-90657**

SHEET 1 OF 40

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	16C30	Universal serial controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P68	68	Pin grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V to +7.0 V dc
Voltages on all pins with respect to V_{SS} (except V_{CC})	-0.3 V dc to V_{CC} + 0.3 V dc
Power dissipation (P_D)	350 mW
Lead temperature (soldering, 10 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+145°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}		1, 2, 3	All	2.2	V_{CC} + 0.3	V
Input low voltage	V_{IL}				-0.3	0.8	V
Output high voltage	V_{OH1}	I_{OH} = -1.6 mA, V_{CC} = 4.5 V			2.4		V
Output high voltage	V_{OH2}	I_{OH} = -250 µA, V_{CC} = 4.5 V			V_{CC} – 0.8		V
Output low voltage	V_{OL}	I_{OL} = +2 mA, V_{CC} = 4.5 V				0.4	V
Input leakage current	I_{IL}	$0.4\ V < V_{IN} < 2.4\ V$ V_{CC} = 5.5 V				10	µA
Output leakage current	I_{OL}	$0.4\ V < V_{IN} < 2.4\ V$ V_{CC} = 5.5 V				10	µA
V_{CC} supply current	I_{CCI}	V_{CC} = 5.0 V V_{IH} = 4.8 V, V_{IL} = -0.2 V				50	mA
Input capacitance	C_{IN}	See 4.4.1.c	4	All		10	pF
Output capacitance	C_{OUT}	See 4.4.1.c				15	pF
Bidirectional capacitance	$C_{I/O}$	See 4.4.1.c				20	pF
Functional testing		See 4.4.1.b	7, 8	All			
Bus cycle time	1	V_{CC} = 4.5 V See figure 3.	9, 10, 11	All	160		ns
$\overline{AS}$ low width	2				40		ns
$\overline{AS}$ high width	3				90		ns
$\overline{DS}$ low width	4				70		ns
$\overline{DS}$ high width	5				60		ns
$\overline{AS}\uparrow$ to $\overline{DS}\downarrow$ delay time	6				5		ns
$\overline{DS}\uparrow$ to $\overline{AS}\downarrow$ delay time	7				5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{DS}\downarrow$ to data active delay	8	V_{CC} = 4.5 V See figure 3.	9, 10, 11	All	0		ns
$\overline{DS}\downarrow$ to data valid delay	9					85	ns
$\overline{DS}\uparrow$ to data not valid delay	10				0		ns
$\overline{DS}\uparrow$ to data float delay	11					20	ns
$\overline{CS}$ to $\overline{AS}\uparrow$ setup time	12				15		ns
$\overline{CS}$ to $\overline{AS}\uparrow$ hold time	13				0		ns
Direct address to $\overline{AS}\uparrow$ setup time 2/	14				15		ns
Direct address to $\overline{AS}\uparrow$ hold time 2/	15				5		ns
$\overline{SITACK}$ to $\overline{AS}\uparrow$ setup time	16				15		ns
$\overline{SITACK}$ to $\overline{AS}\uparrow$ hold time	17				5		ns
Address to $\overline{AS}\uparrow$ setup time	18				15		ns
Address to $\overline{AS}\uparrow$ hold time	19				5		ns
R/$\overline{W}$ to $\overline{DS}\downarrow$ setup time	20				0		ns
R/$\overline{W}$ to $\overline{DS}\downarrow$ hold time	21				25		ns
$\overline{DS}\downarrow$ to $\overline{RxREQ}$ inactive delay 3/	22					60	ns
$\overline{DS}\uparrow$ to $\overline{RxREQ}$ active delay	23				0		ns
Write data to $\overline{DS}\uparrow$ setup time	24				30		ns
Write data to $\overline{DS}\uparrow$ hold time	25				0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{DS}\downarrow$ to $\overline{TxREQ}$ inactive delay 4/	26	V_{CC} = 4.5 V See figure 3.	9, 10, 11	All		70	ns
$\overline{DS}\uparrow$ to $\overline{TxREQ}$ active delay	27				0		ns
$\overline{RD}$ low width	28				70		ns
$\overline{RD}$ high width	29				60		ns
$\overline{AS}\uparrow$ to $\overline{RD}\downarrow$ delay time	30				5		ns
$\overline{RD}\uparrow$ to $\overline{AS}\downarrow$ delay time	31				5		ns
$\overline{RD}\downarrow$ to data active delay	32				0		ns
$\overline{RD}\downarrow$ to data valid delay	33					85	ns
$\overline{RD}\uparrow$ to data non valid delay	34				0		ns
$\overline{RD}\uparrow$ to data float delay	35					20	ns
$\overline{RD}\downarrow$ to $\overline{RxREQ}$ inactive delay 3/	36					60	ns
$\overline{RD}\uparrow$ to $\overline{RxREQ}$ active delay	37				0		ns
$\overline{WR}$ low width	38				70		ns
$\overline{WR}$ high width	39				60		ns
$\overline{AS}\uparrow$ to $\overline{WR}\downarrow$ delay time	40				5		ns
$\overline{WR}\uparrow$ to $\overline{AS}\downarrow$ delay time	41				5		ns
Write data to $\overline{WR}\uparrow$ setup time	42				30		ns
Write data to $\overline{WR}\uparrow$ hold time	43				0		ns
$\overline{WR}\downarrow$ to $\overline{TxREQ}$ inactive delay 4/	44					70	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{WR}\uparrow$ to $\overline{TxREQ}$ active delay	45	V_{CC} = 4.5 V See figure 3.	9, 10, 11	All	0		ns
$\overline{CS}$ to $\overline{DS}\downarrow$ setup time 5/	46				0		ns
$\overline{CS}$ to $\overline{DS}\downarrow$ hold time 5/	47				25		ns
Direct address to $\overline{DS}\downarrow$ setup time 2/ 5/	48				5		ns
Direct address to $\overline{DS}\downarrow$ hold time 2/ 5/	49				25		ns
$\overline{SITACK}$ to $\overline{DS}\downarrow$ setup time 5/	50				5		ns
$\overline{SITACK}$ to $\overline{DS}\downarrow$ hold time 5/	51				25		ns
$\overline{CS}$ to $\overline{RD}\downarrow$ setup time 5/	52				0		ns
$\overline{CS}$ to $\overline{RD}\downarrow$ hold time 5/	53				25		ns
Direct address to $\overline{RD}\downarrow$ setup time 2/ 5/	54				5		ns
Direct address to $\overline{RD}\downarrow$ hold time 2/ 5/	55				25		ns
$\overline{SITACK}$ to $\overline{RD}\downarrow$ setup time 5/	56				5		ns
$\overline{SITACK}$ to $\overline{RD}\downarrow$ hold time 5/	57				25		ns
$\overline{CS}$ to $\overline{WR}\downarrow$ setup time 5/	58				0		ns
$\overline{CS}$ to $\overline{WR}\downarrow$ hold time 5/	59				25		ns
Direct address to $\overline{WR}\downarrow$ setup time 2/ 5/	60				5		ns
Direct address to $\overline{WR}\downarrow$ hold time 2/ 5/	61				25		ns
$\overline{SITACK}$ to $\overline{WR}\downarrow$ setup time 5/	62				5		ns
$\overline{SITACK}$ to $\overline{WR}\downarrow$ hold time 5/	63				25		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{\text{RxACK}}$ low width 5/	64	V_{CC} = 4.5 V See figure 3.	9, 10, 11	All	70		ns
$\overline{\text{RxACK}}$ high width 5/	65				60		ns
$\overline{\text{RxACK}}\downarrow$ to data active delay	66				0		ns
$\overline{\text{RxACK}}\downarrow$ to data valid delay	67					85	ns
$\overline{\text{RxACK}}\uparrow$ to data not valid delay	68				0		ns
$\overline{\text{RxACK}}\uparrow$ to data float delay	69					20	ns
$\overline{\text{RxACK}}\downarrow$ to $\overline{\text{RxREQ}}$ inactive delay 3/	70					60	ns
$\overline{\text{RxACK}}\uparrow$ to $\overline{\text{RxREQ}}$ active delay	71				0		ns
$\overline{\text{TxACK}}$ low width	72				70		ns
$\overline{\text{TxACK}}$ high width	73				60		ns
Write data to $\overline{\text{TxACK}}\uparrow$ setup time	74				30		ns
Write data to $\overline{\text{TxACK}}\uparrow$ hold time	75				0		ns
$\overline{\text{TxACK}}\downarrow$ to $\overline{\text{TxREQ}}$ inactive delay 4/	76					60	ns
$\overline{\text{TxACK}}\uparrow$ to $\overline{\text{TxREQ}}$ active delay	77				0		ns
$\overline{\text{DS}}\downarrow$ (intack) to $\overline{\text{READY}}\downarrow$ delay	78					200	ns
$\overline{\text{READY}}\downarrow$ to data valid delay	79					40	ns
$\overline{\text{D}}\uparrow$ to $\overline{\text{READY}}\uparrow$ delay	80					40	ns
IEI to $\overline{\text{DS}}\downarrow$ (intack) setup time	81				60		ns
IEI to $\overline{\text{DS}}\uparrow$ (intack) hold time	82				0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
IEI to IEO delay	83	V_{CC} = 4.5 V See figure 3.	9, 10, 11	All		60	ns
$\overline{AS}\uparrow$ (intack) to IEO delay	84					60	ns
$\overline{DS}\downarrow$ (intack) to $\overline{INT}$ inactive delay	85					200	ns
$\overline{DS}\downarrow$ (intack) to $\overline{WAIT}\downarrow$ delay	86					40	ns
$\overline{DS}\downarrow$ (intack) to $\overline{WAIT}\uparrow$ delay	87					200	ns
$\overline{WAIT}\uparrow$ to data valid delay	88					40	ns
$\overline{RD}\downarrow$ (intack) to $\overline{READY}\downarrow$ delay	89					200	ns
$\overline{RD}\uparrow$ to $\overline{READY}\uparrow$ delay	90					40	ns
IEI to $\overline{RD}\downarrow$ (intack) setup time	91				60		ns
IEI to $\overline{RD}\uparrow$ (intack) hold time	92				0		ns
$\overline{RD}\downarrow$ (intack) to $\overline{INT}$ inactive delay	93					200	ns
$\overline{RD}\downarrow$ (intack) to $\overline{WAIT}\downarrow$ delay	94					40	ns
$\overline{RD}\downarrow$ (intack) to $\overline{WAIT}\uparrow$ delay	95					200	ns
$\overline{PITACK}$ low width	96				70		ns
$\overline{PITACK}$ high width	97				60		ns
$\overline{AS}\uparrow$ to $\overline{PITACK}\downarrow$ delay time	98				5		ns
$\overline{PITACK}\uparrow$ to $\overline{AS}\downarrow$ delay time	99				5		ns
$\overline{PITACK}\downarrow$ to data active delay	100				0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{PITACK}\uparrow$ to data not valid delay	101	V_{CC} = 4.5 V See figure 3.	9, 10, 11	All	0		ns
$\overline{PITACK}\uparrow$ to data float delay	102					20	ns
IEI to $\overline{PITACK}\downarrow$ setup time	103				60		ns
IEI to $\overline{PITACK}\uparrow$ hold time	104				0		ns
$\overline{PITACK}\downarrow$ to IEO delay	105					60	ns
$\overline{PITACK}\downarrow$ to $\overline{INT}$ inactive delay	106					200	ns
$\overline{PITACK}\downarrow$ to $\overline{READY}\downarrow$ delay	107					200	ns
$\overline{PITACK}\uparrow$ to $\overline{READY}\uparrow$ delay	108					40	ns
$\overline{PITACK}\downarrow$ to $\overline{WAIT}\downarrow$ delay	109					40	ns
$\overline{PITACK}\downarrow$ to $\overline{WAIT}\uparrow$ delay	110					200	ns
$\overline{SITACK}\downarrow$ to IEO inactive delay 5/	111					200	ns
$\overline{Strobe}$ high width 6/	112				60		ns
$\overline{Reset}$ low width	113				170		ns
$\overline{Reset}$ high width	114				60		ns
$\overline{Reset}\uparrow$ to $\overline{Strobe}\downarrow$ 6/	115				60		ns
$\overline{DS}\downarrow$ to $\overline{READY}\downarrow$ delay	116					50	ns
$\overline{WR}\downarrow$ to $\overline{READY}\downarrow$ delay	117					50	ns
$\overline{WR}\uparrow$ to $\overline{READY}\uparrow$ delay	118					40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{RD}\downarrow$ to $\overline{READY}\downarrow$ delay	119	V_{CC} = 4.5 V See figure 3.	9, 10, 11	All		50	ns
$\overline{RxACK}\downarrow$ to $\overline{READY}\downarrow$ delay	120					50	ns
$\overline{RxACK}\uparrow$ to $\overline{READY}\uparrow$ delay	121					40	ns
$\overline{TxACK}\downarrow$ to $\overline{READY}\downarrow$ delay	122					50	ns
$\overline{TxACK}\uparrow$ to $\overline{READY}\uparrow$ delay	123					40	ns

1/ All testing to be performed at worst-case test conditions unless otherwise specified.

2/ Direct address is any of A/$\overline{B}$, D/$\overline{C}$ or AD15 – AD8 used as an address bus.

3/ Parameter applies only if read empties the receive FIFO.

4/ Parameter applies only if write fills the transmit FIFO.

5/ The parameter applies only when $\overline{AS}$ is not present.

6/ Strobe is any of $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, $\overline{PITACK}$, $\overline{RxACK}$, or $\overline{TxACK}$.

Case X

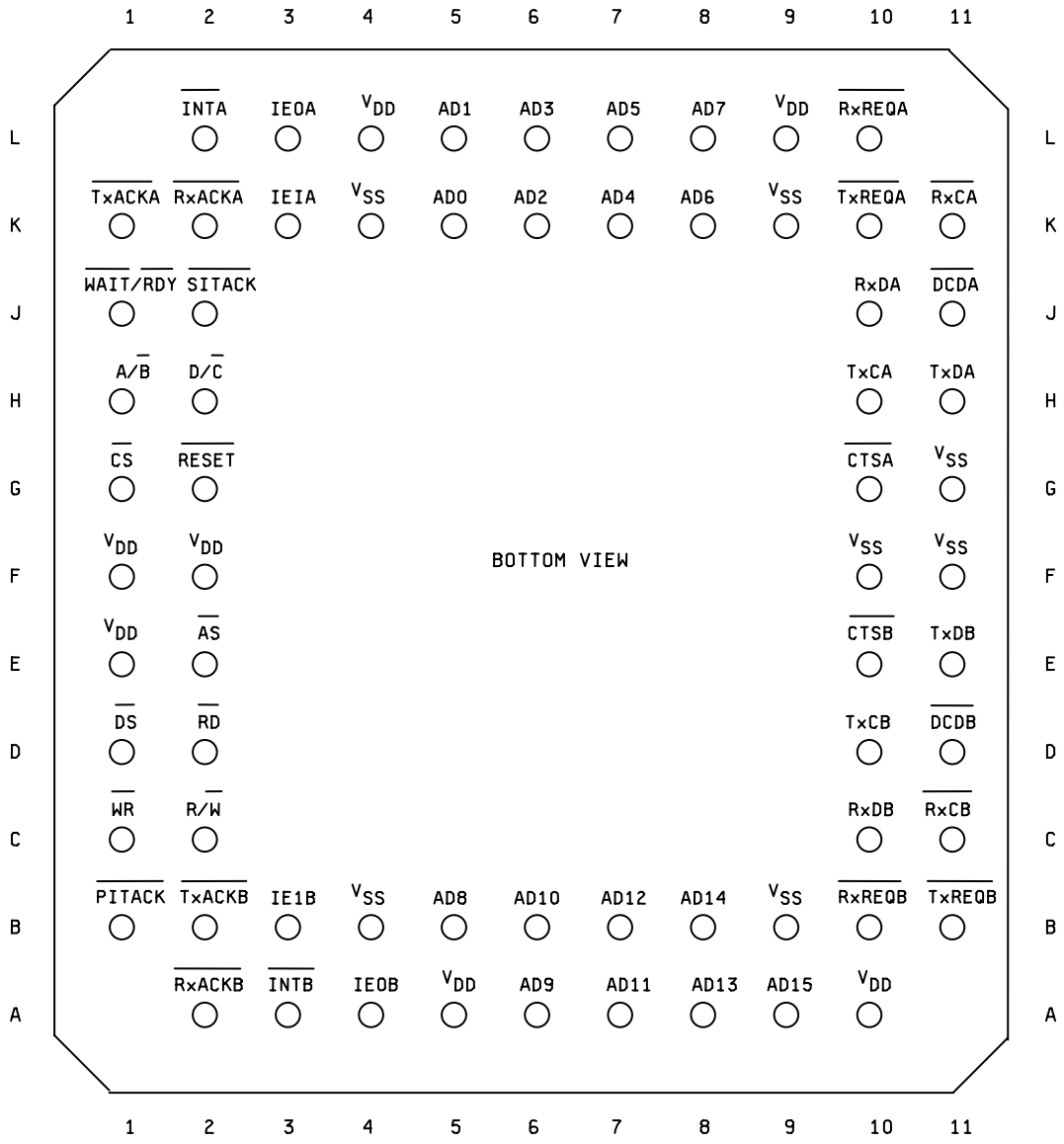


FIGURE 1. Terminal connections.

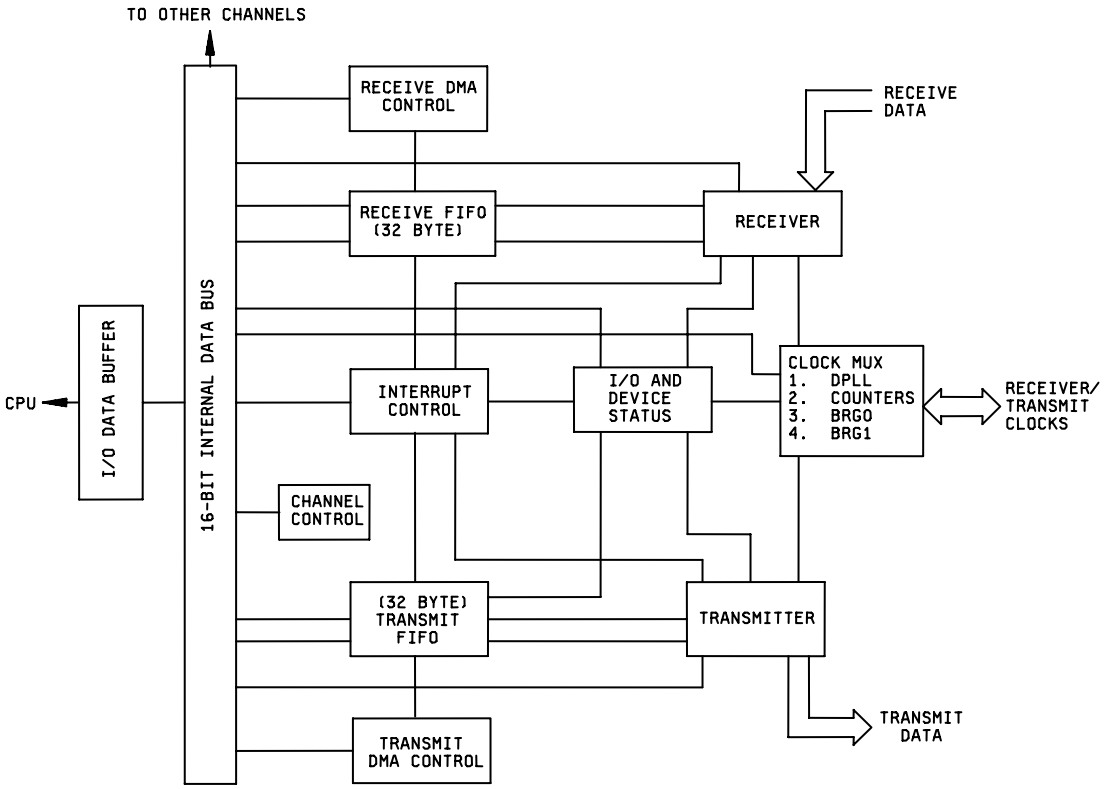
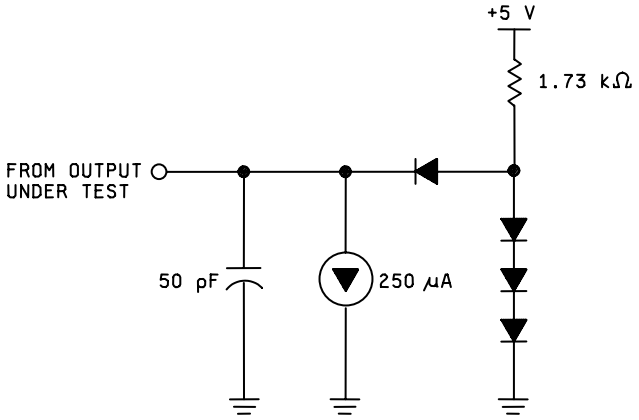
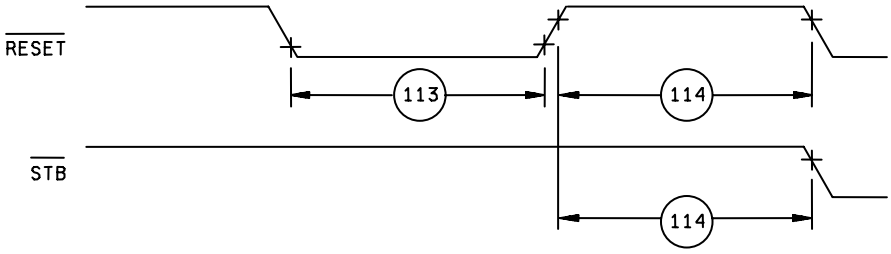


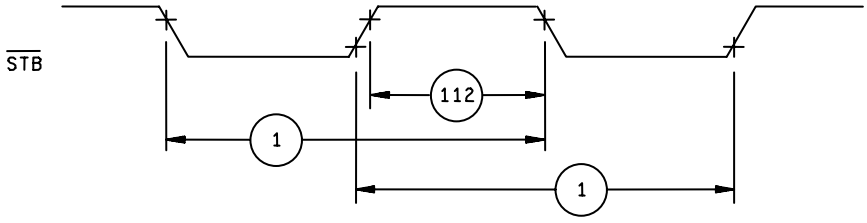
FIGURE 2. Block diagram.



STANDARD TEST LOAD

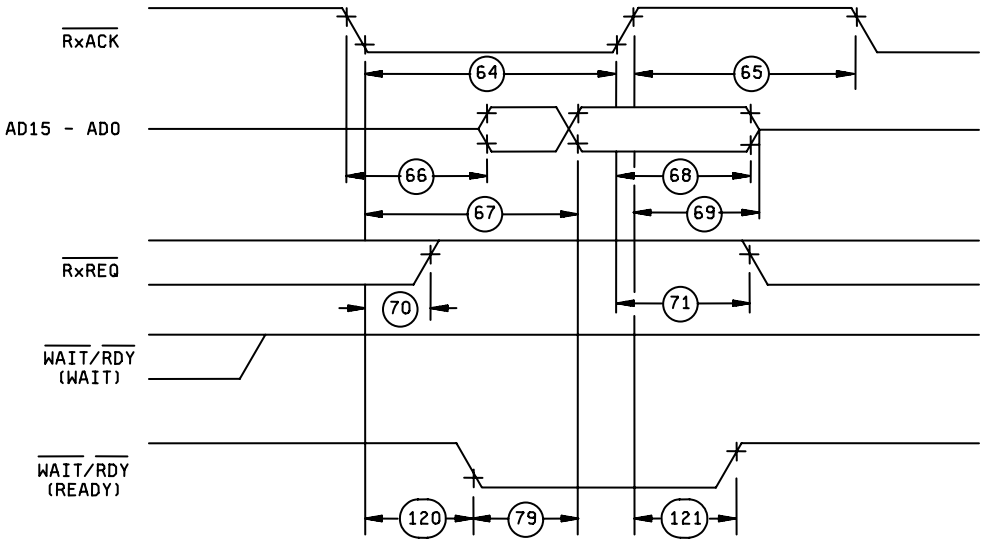


RESET TIMING

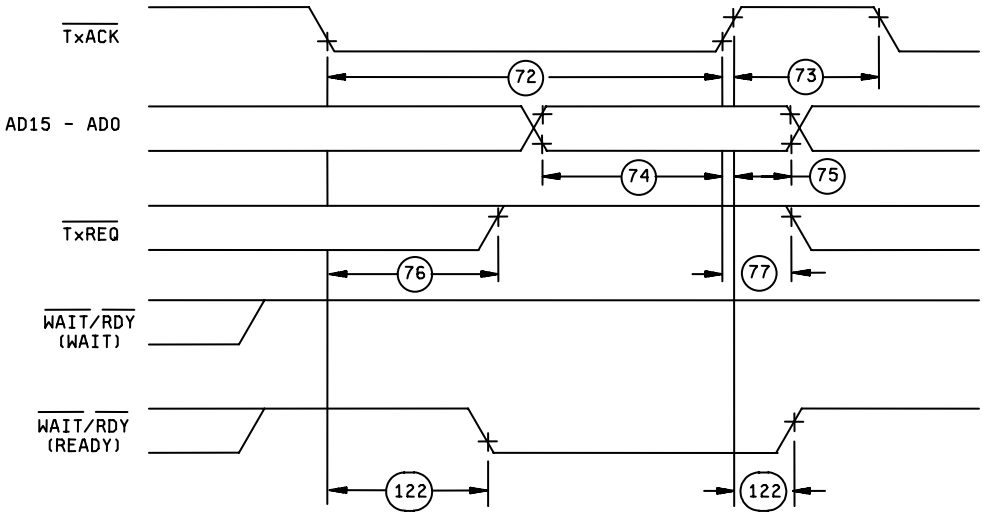


BUS CYCLE TIMING

FIGURE 3. Timing waveforms and test circuit.

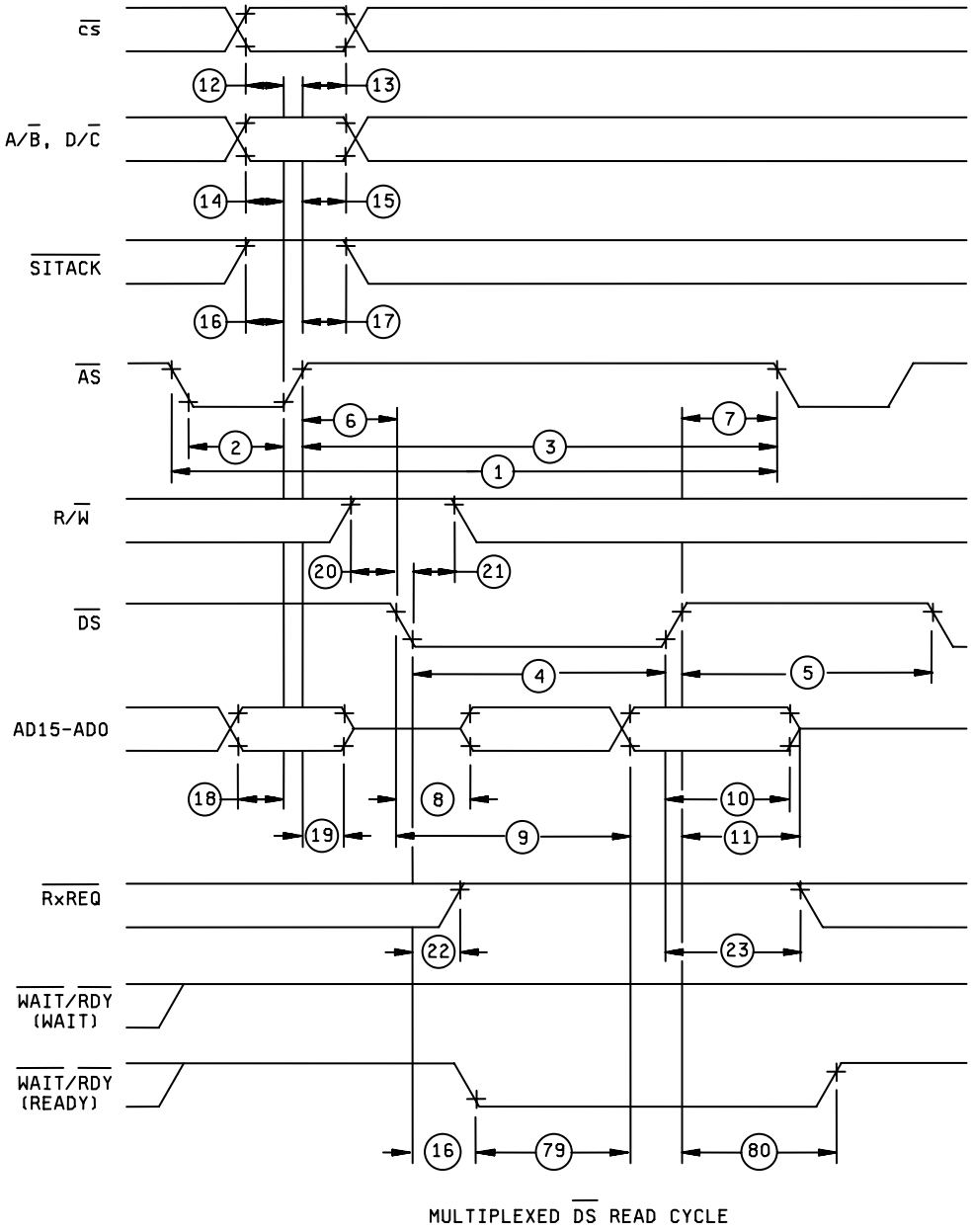


DMA READ CYCLE



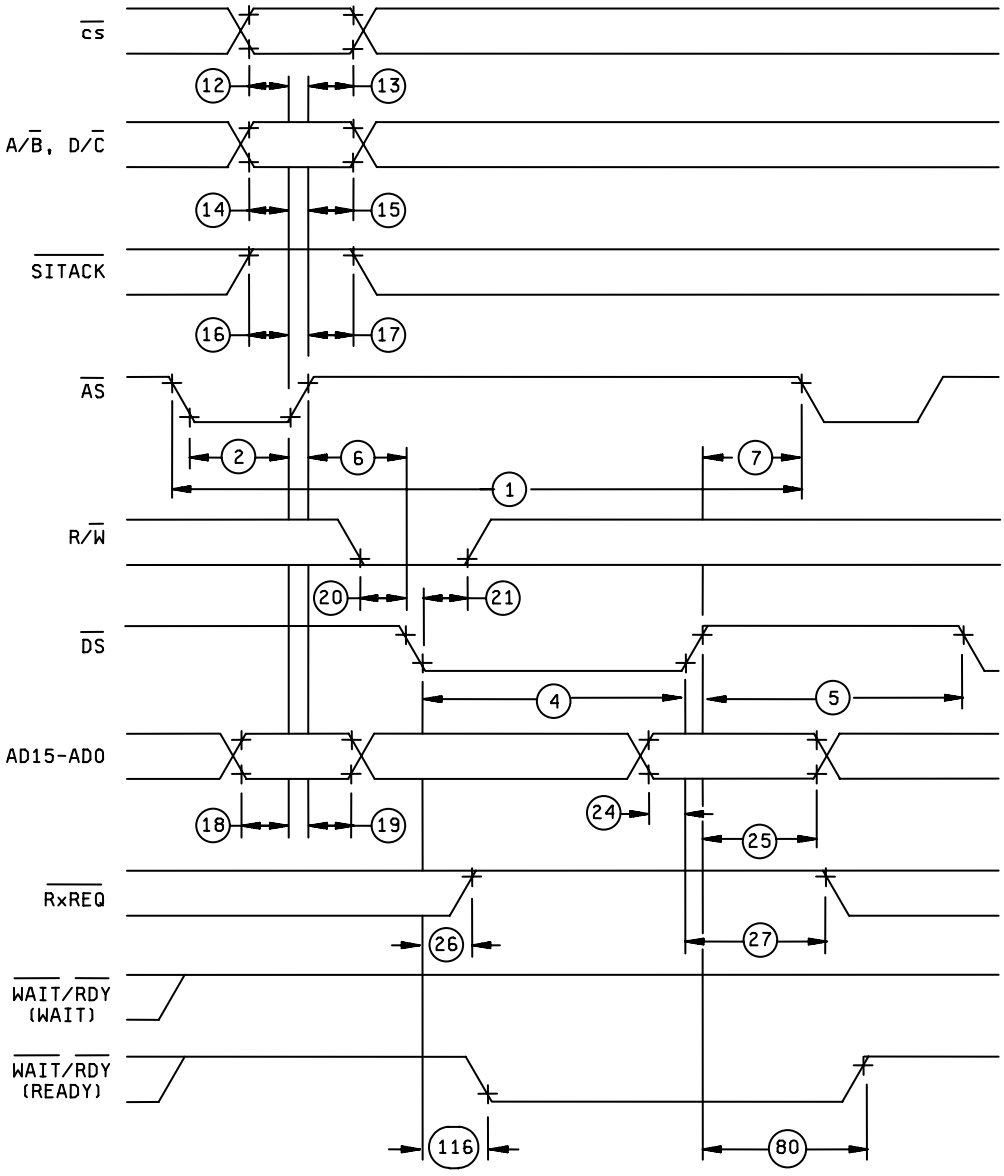
DMA WRITE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



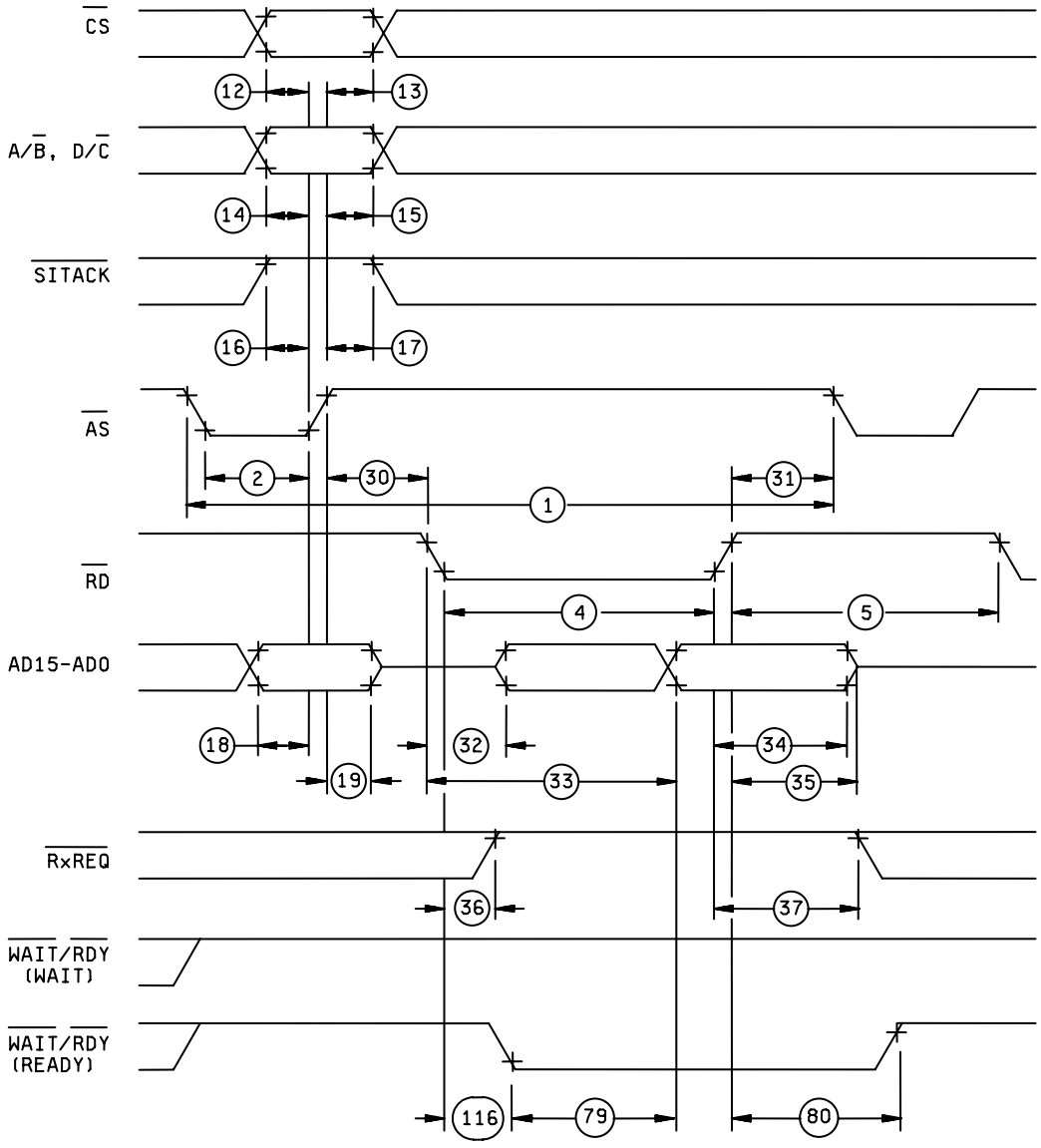
MULTIPLEXED $\overline{DS}$ READ CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



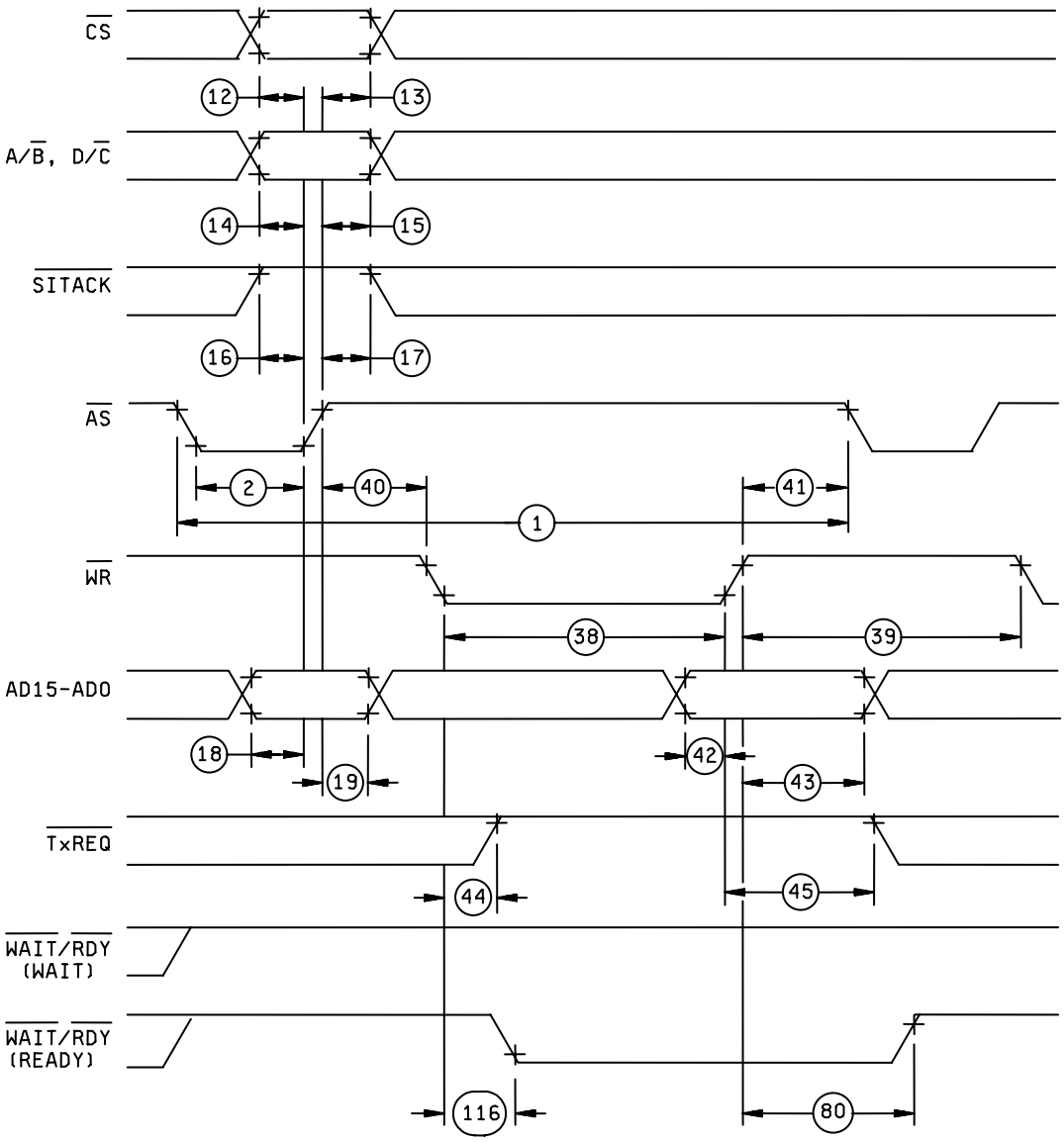
MULTIPLEXED DS WRITE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



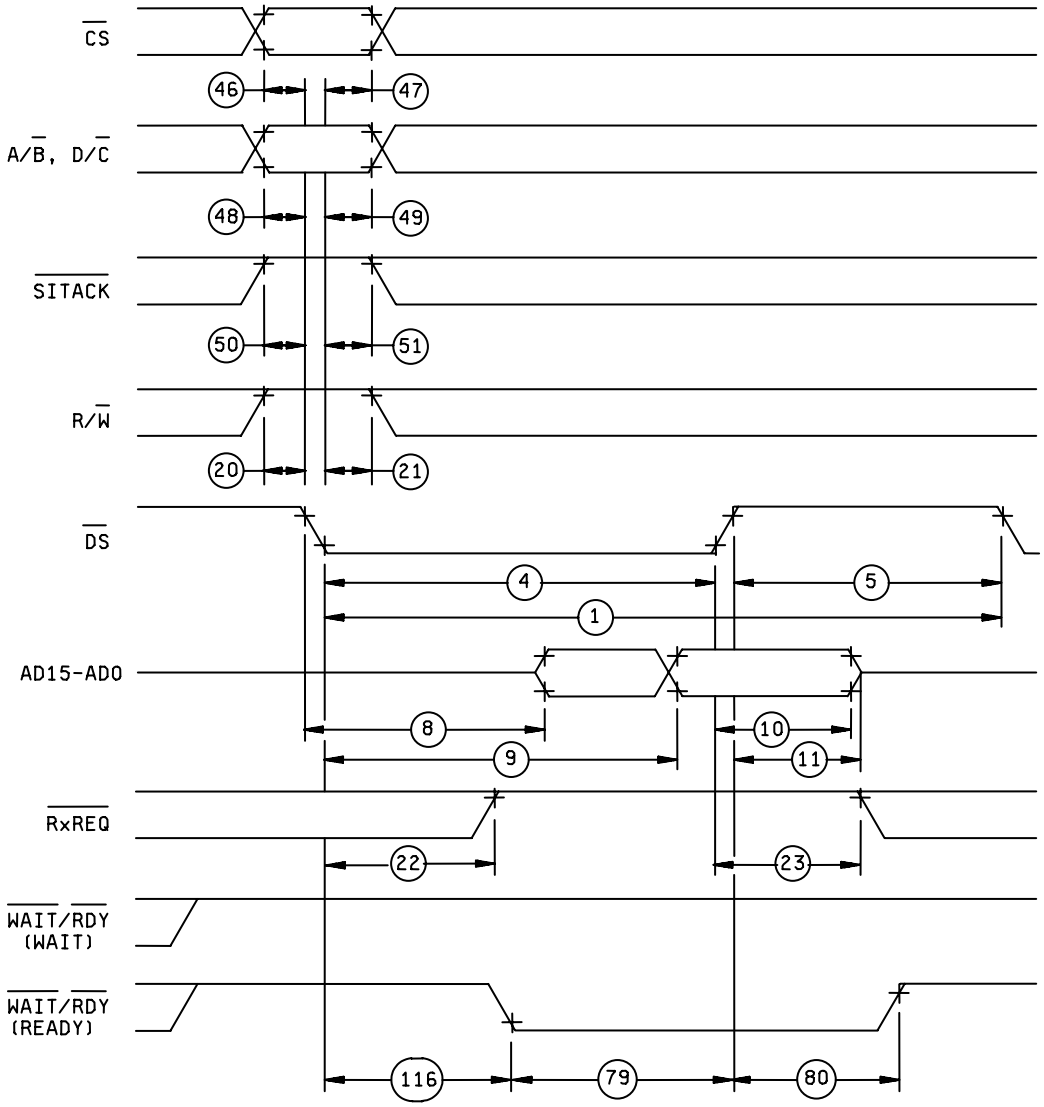
MULTIPLEXED $\overline{RD}$ READ CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



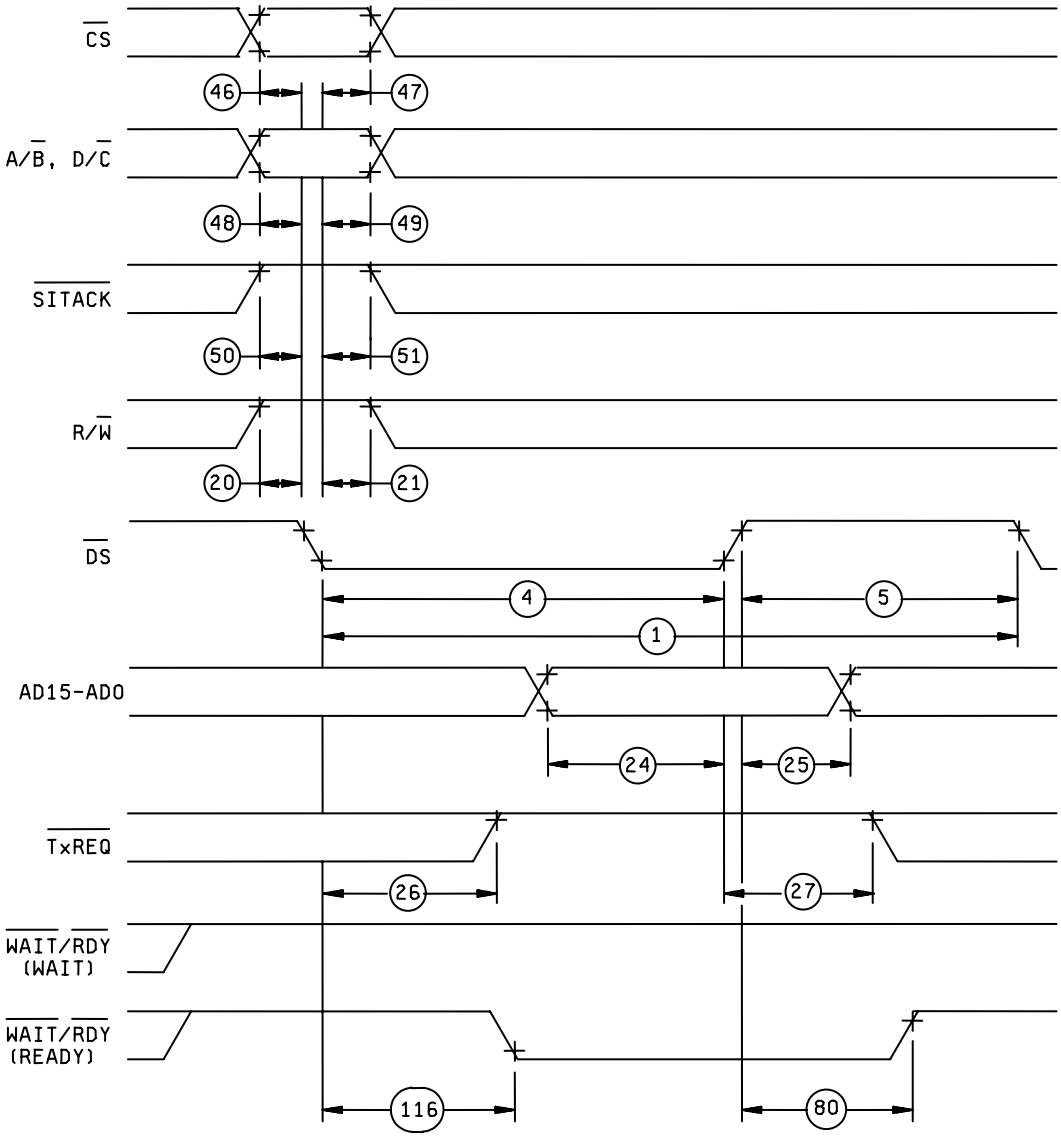
MULTIPLEXED WR WRITE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



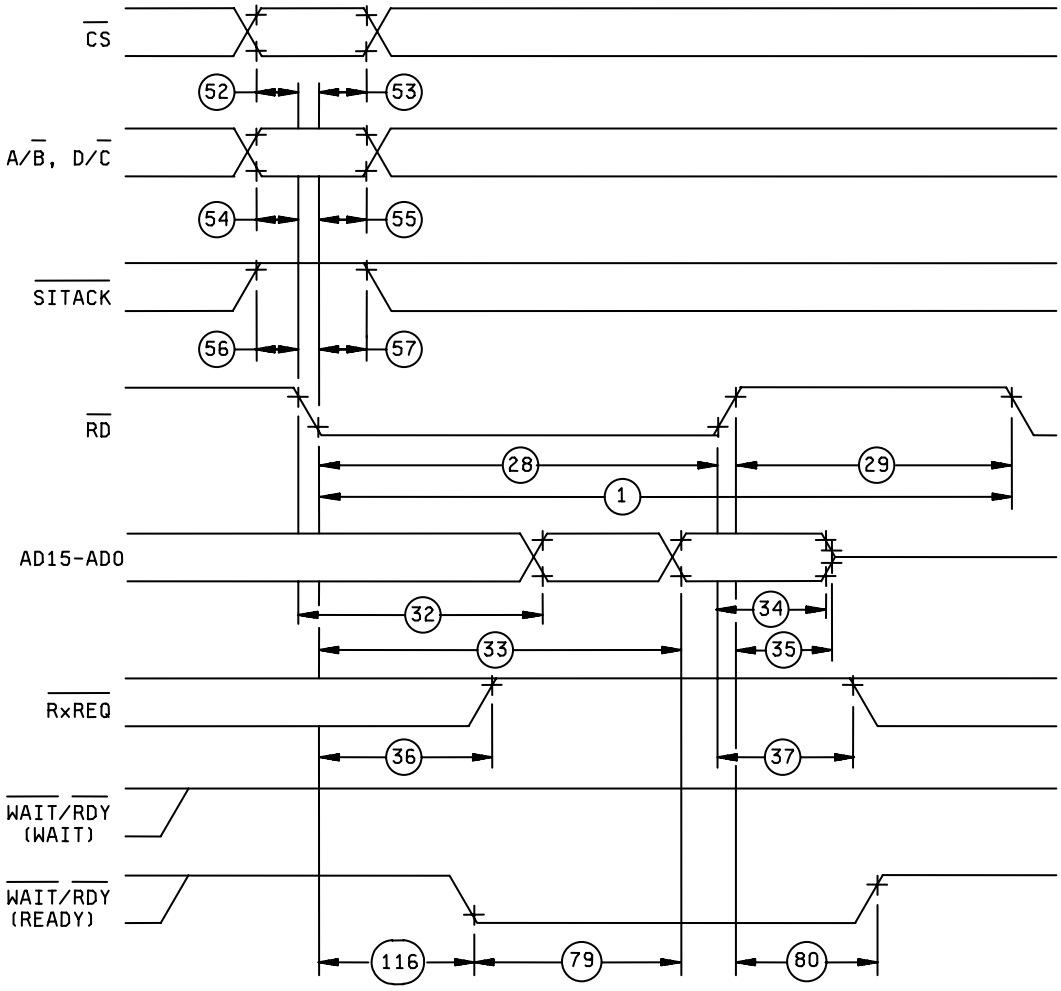
NON-MULTIPLEXED DS READ CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



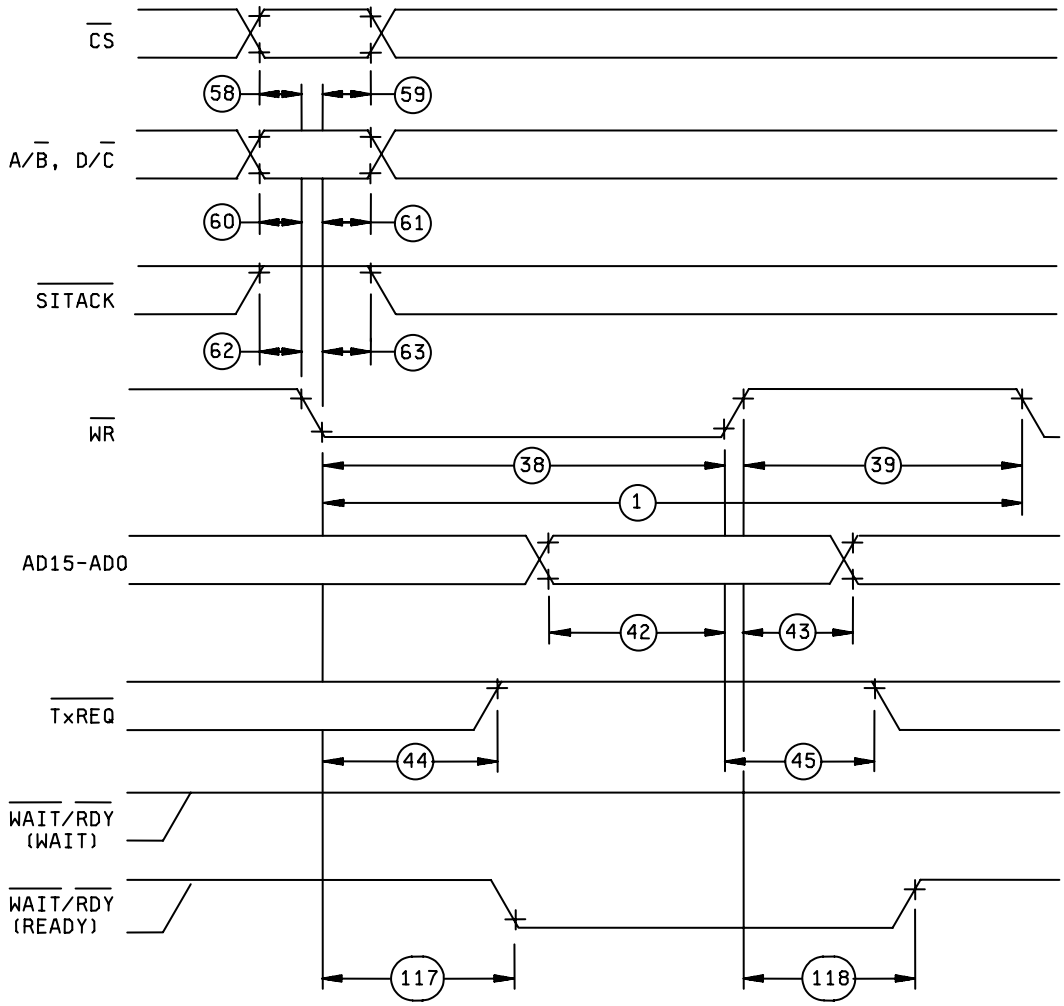
NON-MULTIPLEXED DS WRITE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



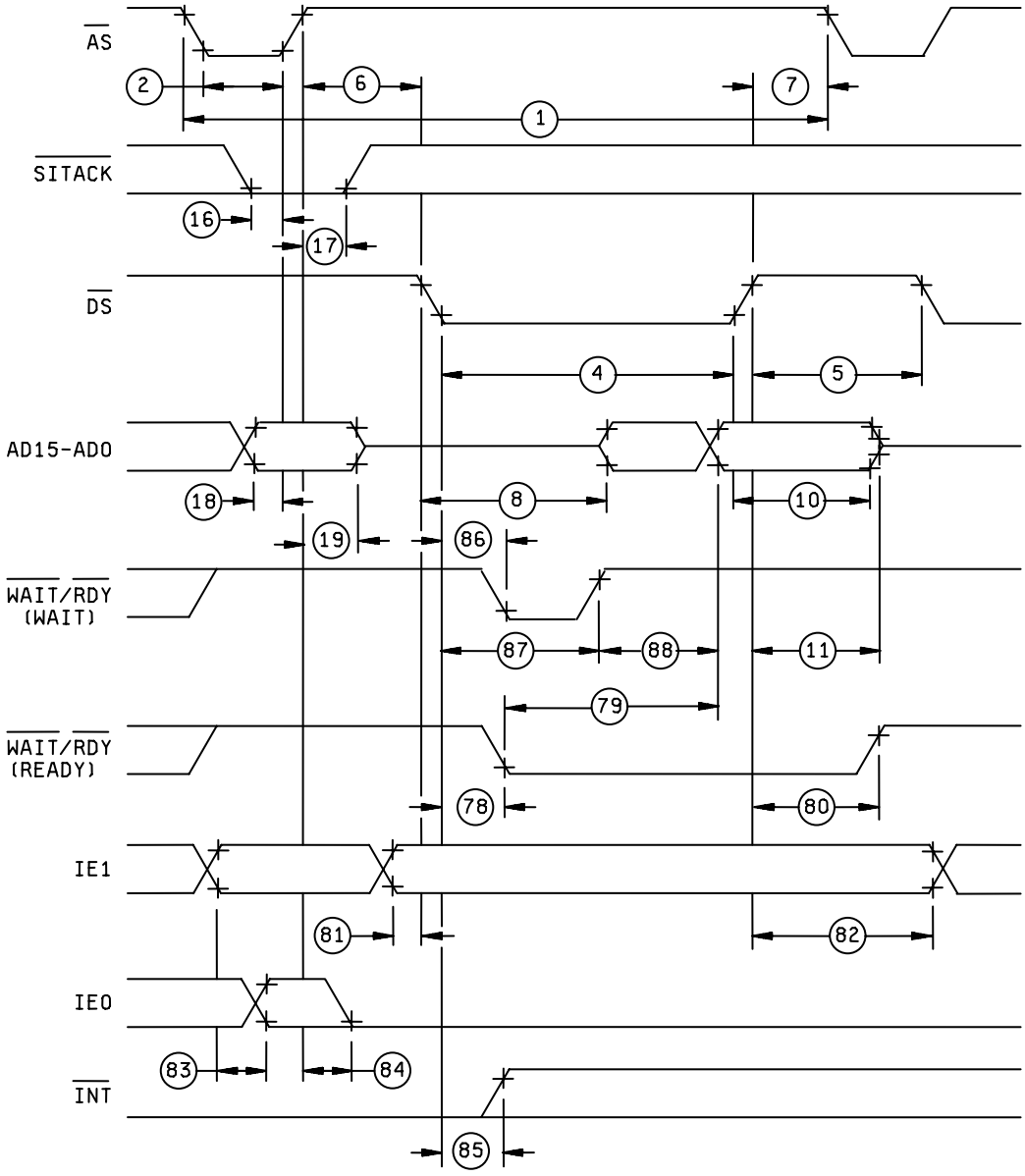
NON-MULTIPLEXED RD READ CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



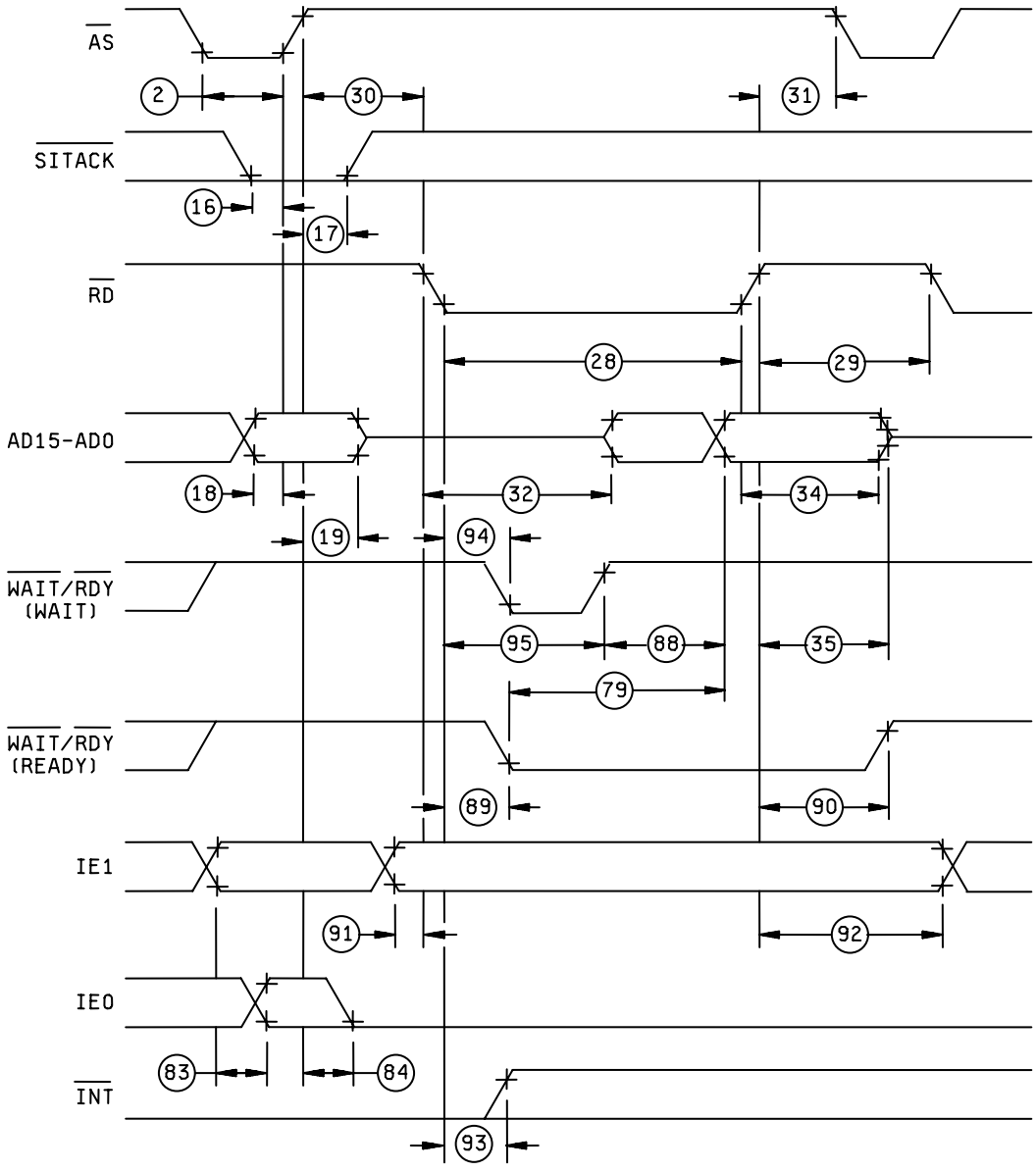
NON-MULTIPLEXED WR WRITE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



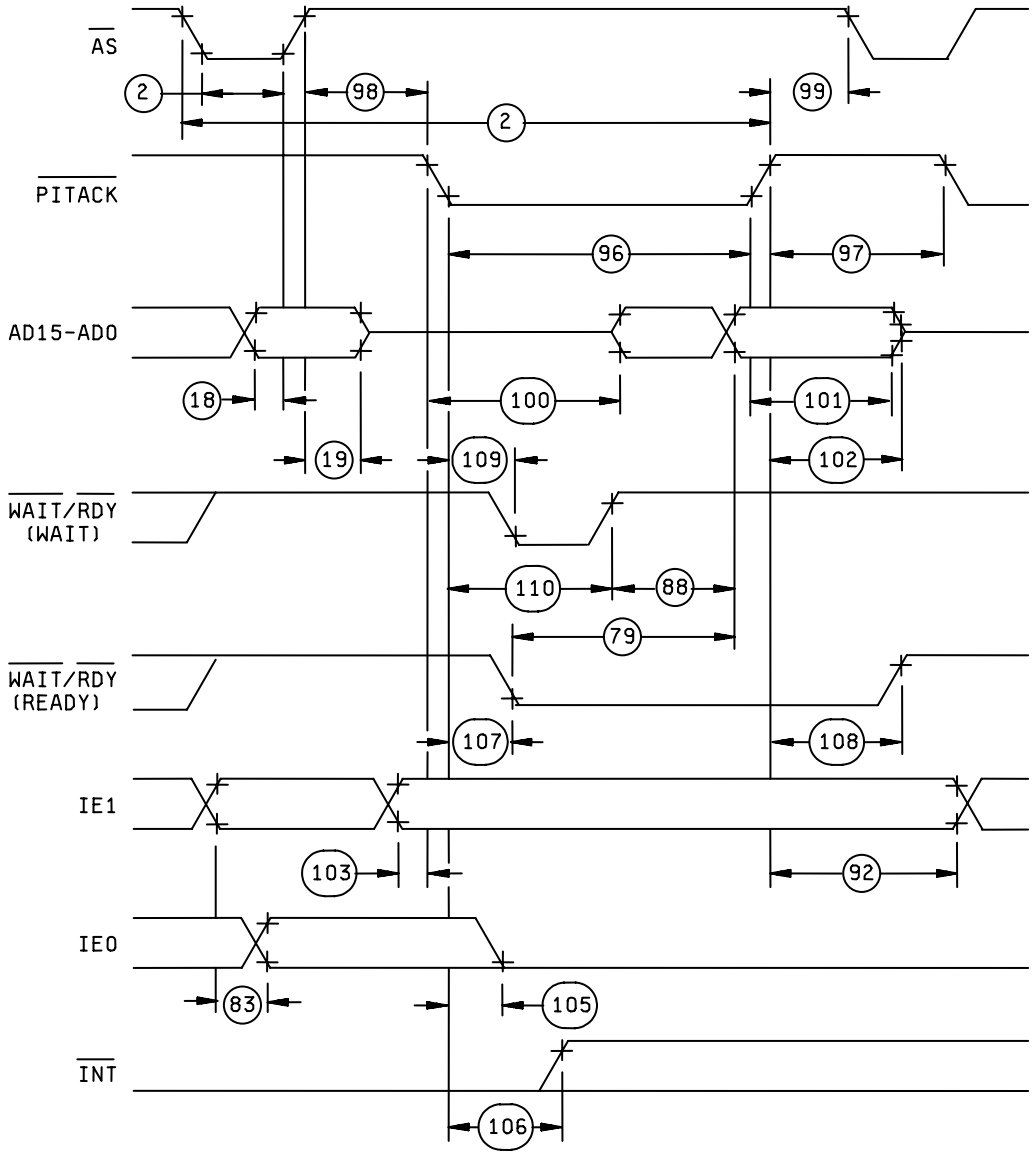
MULTIPLEXED $\overline{DS}$ INTERRUPT ACKNOWLEDGE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



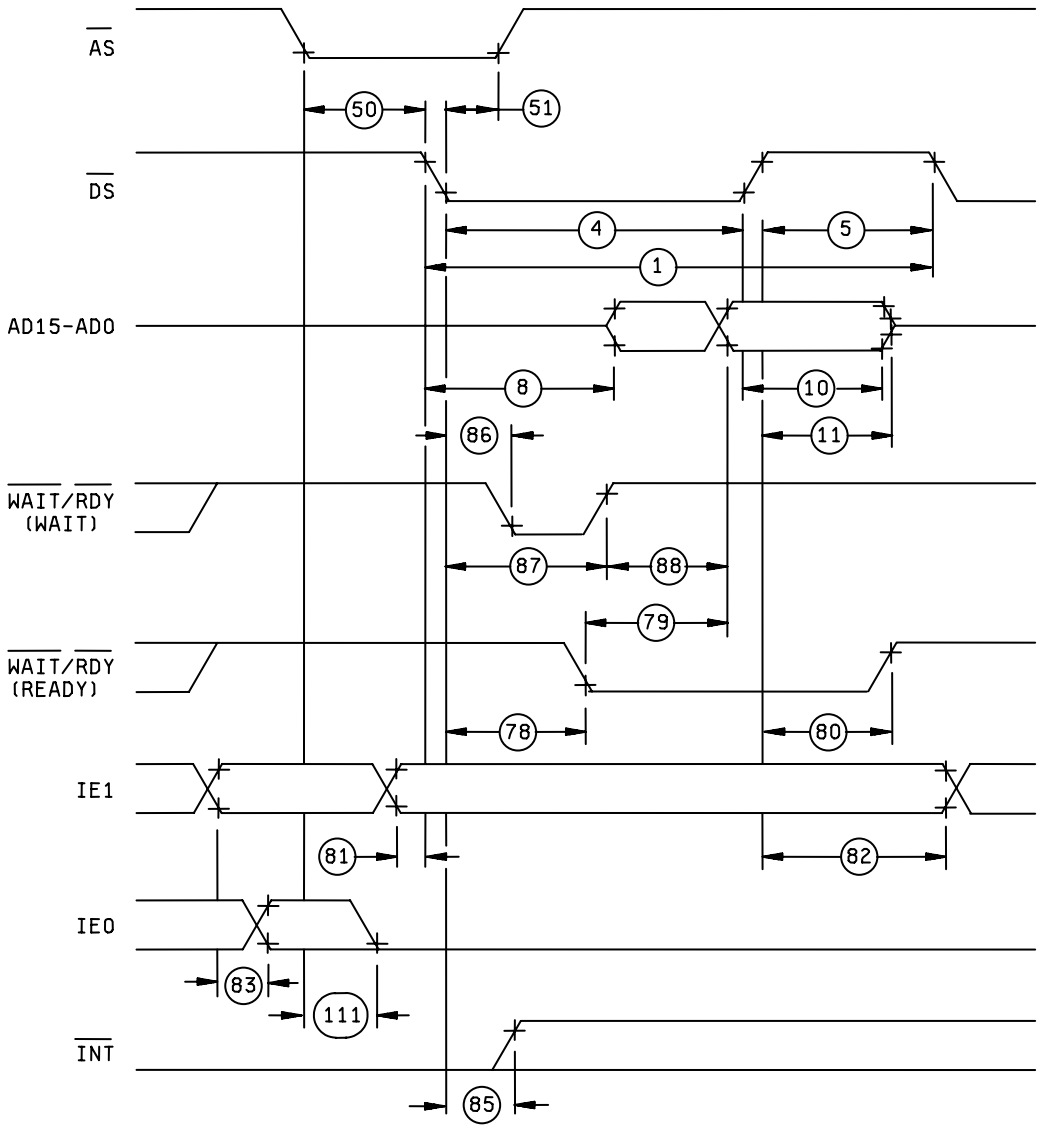
MULTIPLEXED $\overline{RD}$ INTERRUPT ACKNOWLEDGE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



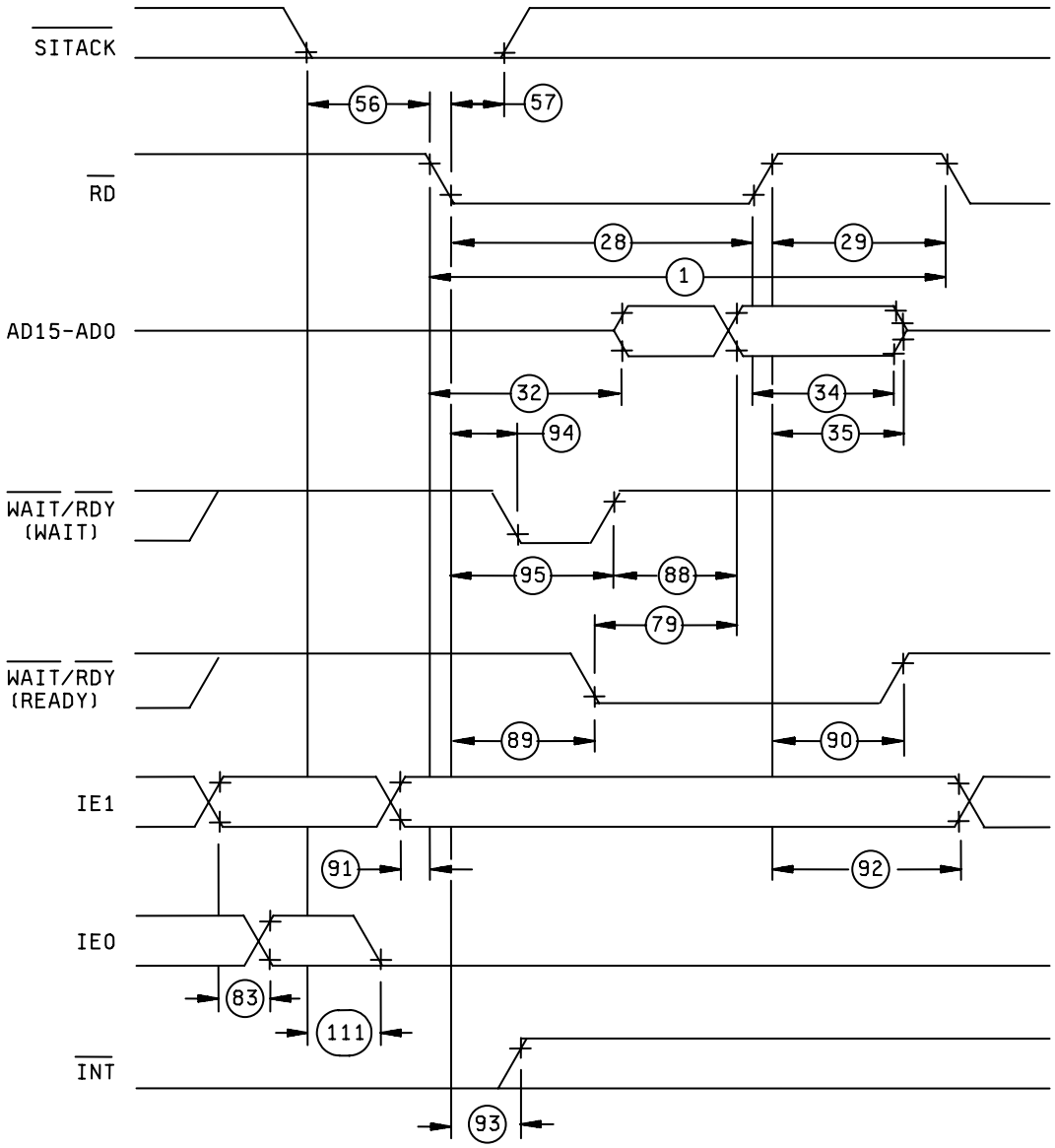
MULTIPLEXED PULSED INTERRUPT ACKNOWLEDGE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



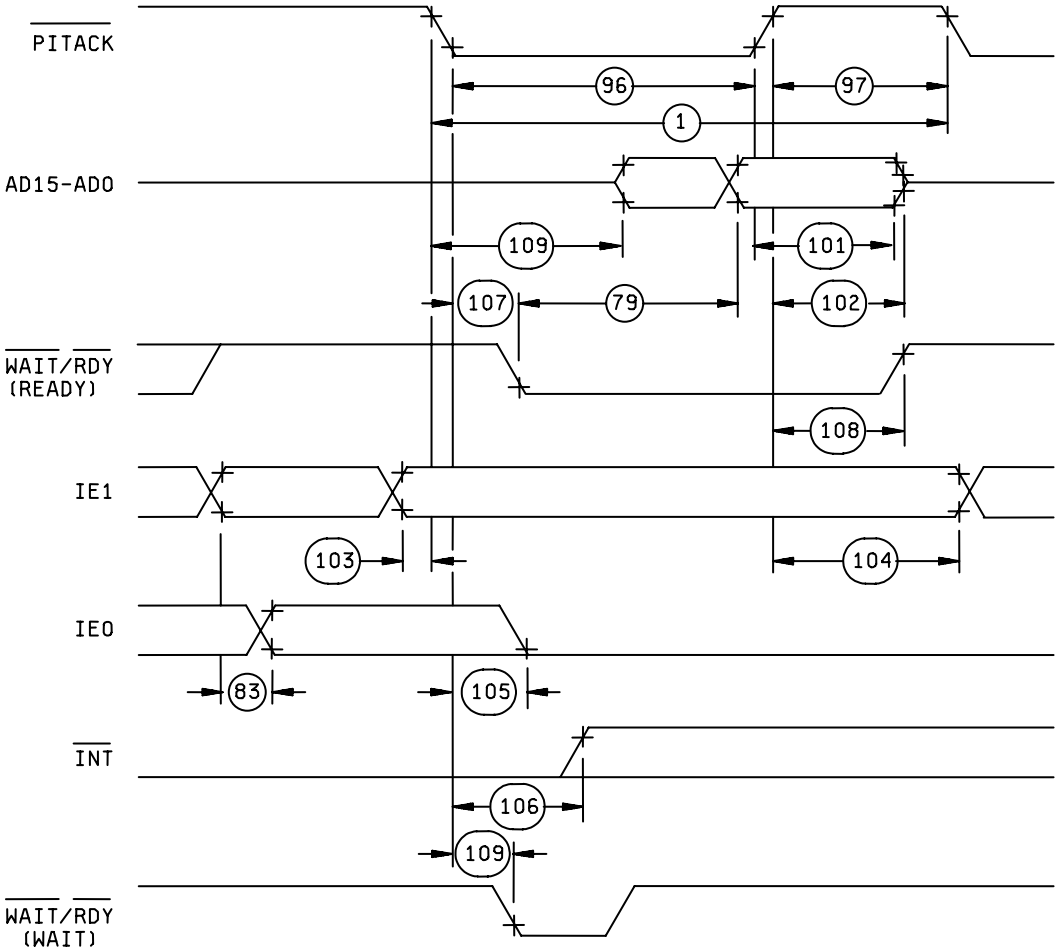
NON-MUX $\overline{DS}$ INTERRUPT ACKNOWLEDGE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



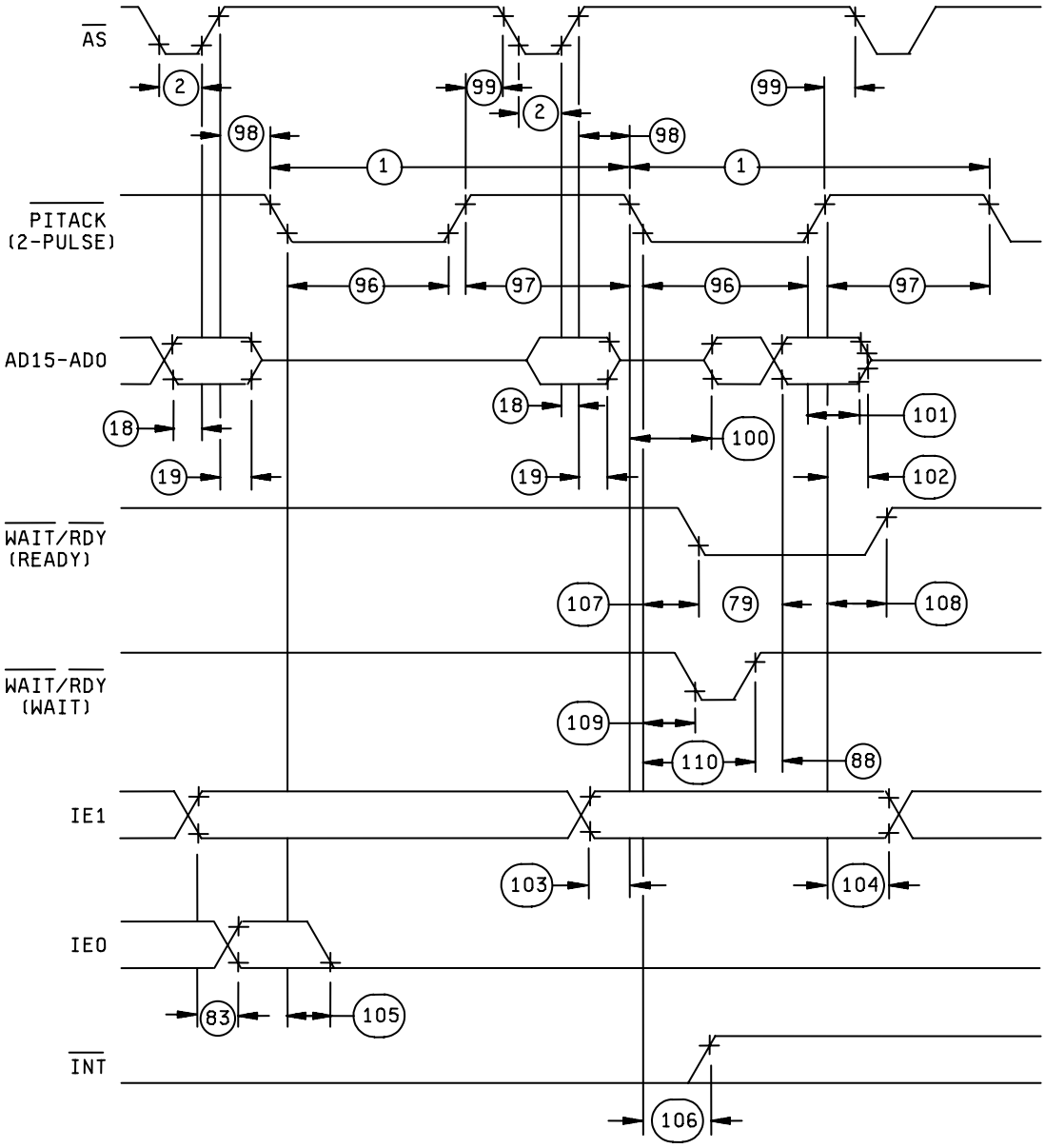
NON-MUX PULSED INTERRUPT ACKNOWLEDGE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



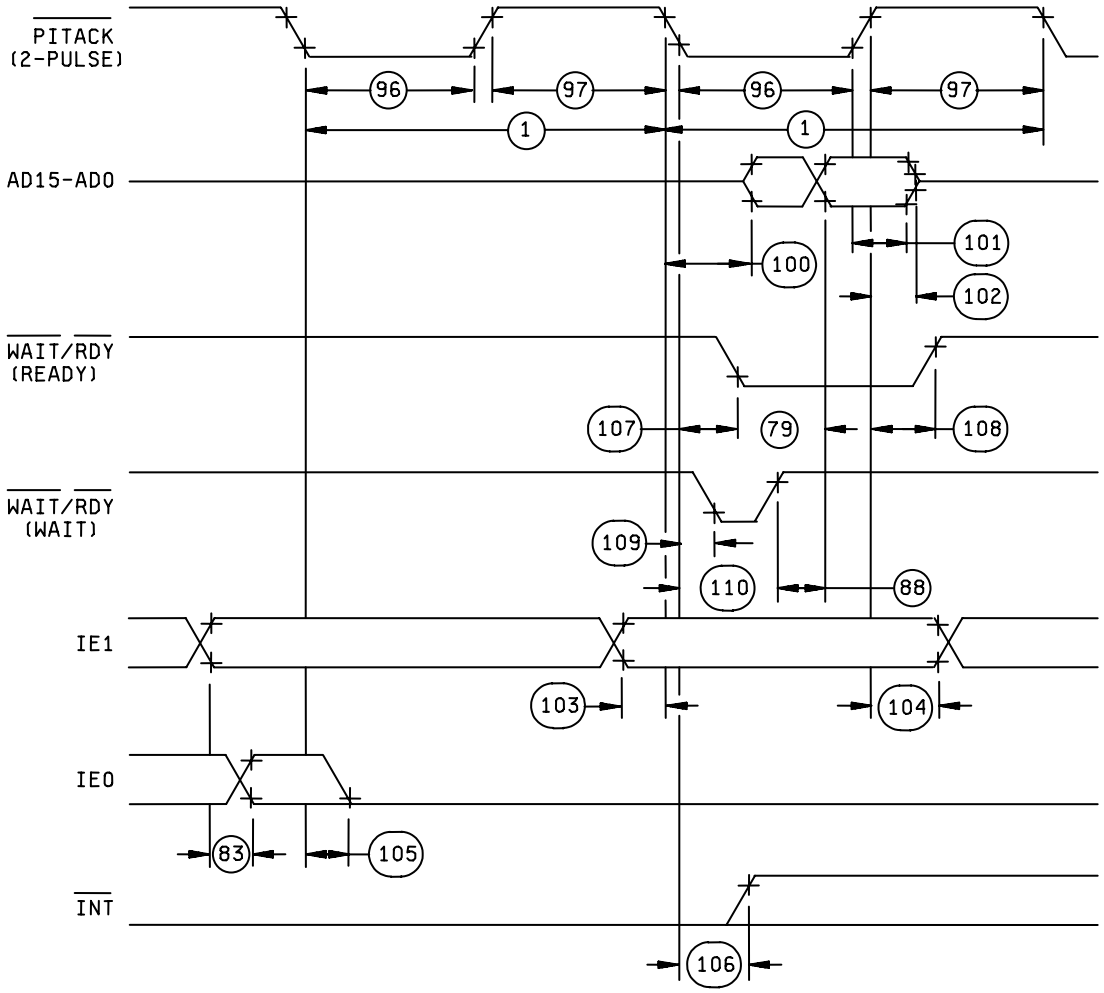
NON-MUX $\overline{RD}$ INTERRUPT ACKNOWLEDGE CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



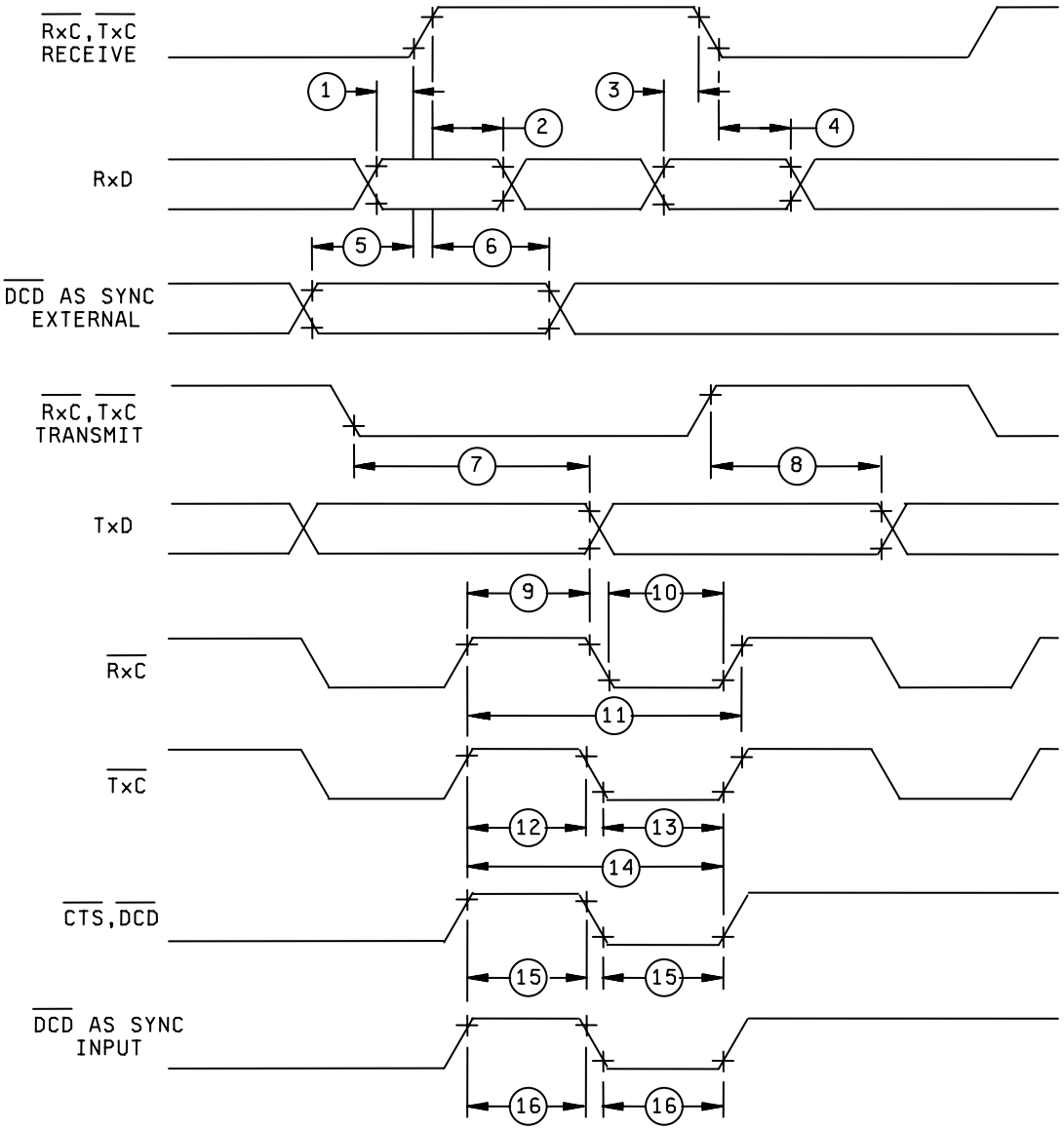
MULTILPEXED DOUBLE-PULSE INTACK CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



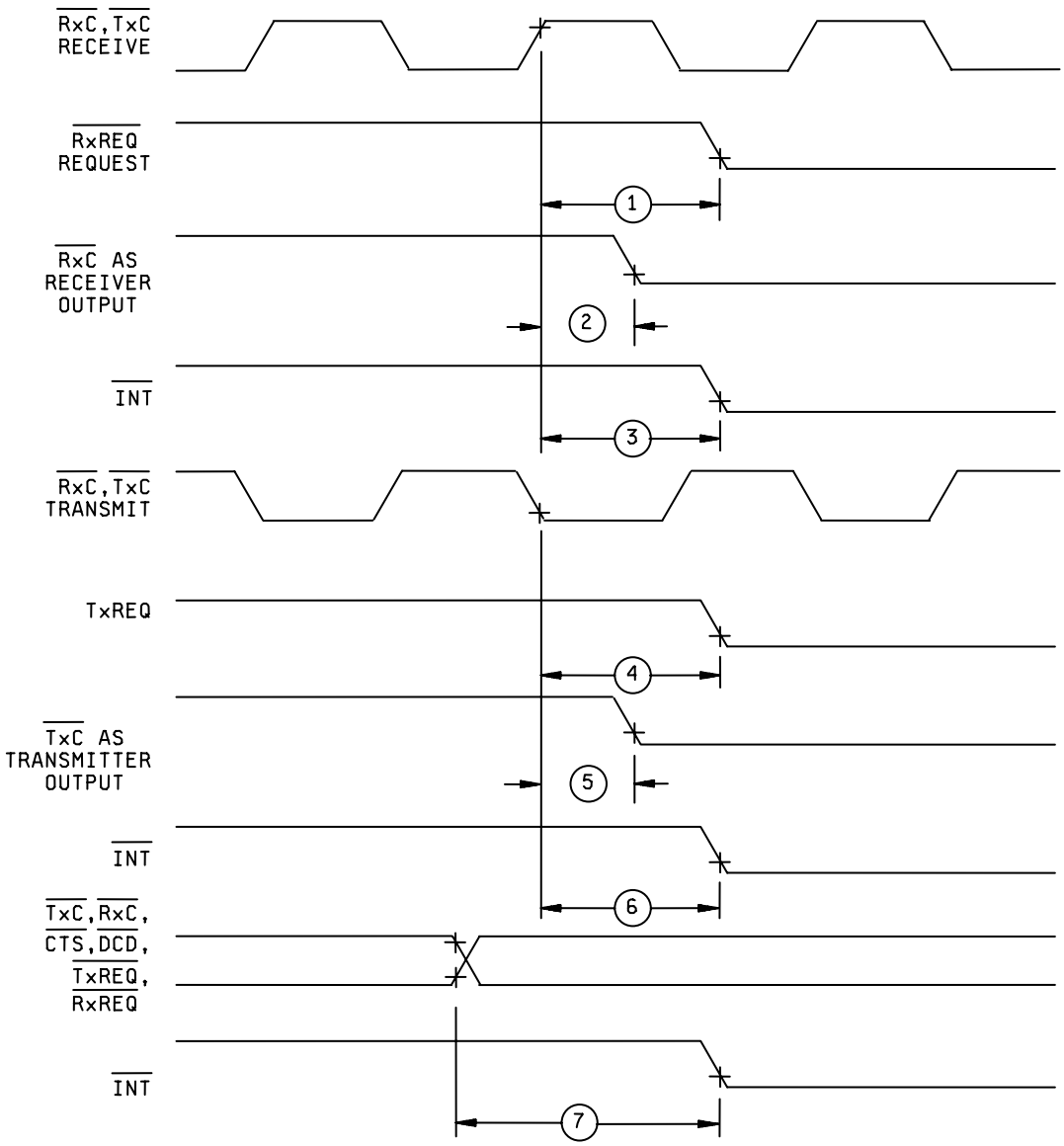
NON-MULTILPEXED DOUBLE-PULSE INTACK CYCLE

FIGURE 3. Timing waveforms and test circuit - Continued.



GENERAL TIMING

FIGURE 3. Timing waveforms and test circuit - Continued.



SYSTEM TIMING

FIGURE 3. Timing waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows in table III.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin descriptions.

Symbol	Function
$\overline{\text{RESET}}$	Reset (input, active low). This signal resets the device to a known state. The first write to the USC after a reset accesses the BCR to select additional bus options for the device.
$\overline{\text{AS}}$	Address Strobe (input, active low). This signal is used in the multiplexed bus modes to latch the address on the AD lines. The AS signal is not used in the non-multiplexed bus modes and should be tied to V_{DD} in these cases.
$\overline{\text{DS}}$	Data Strobe (input, active low). This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle. DS also strobes data into the device during the active state of R/W.
$\overline{\text{RD}}$	Read strobe (input, active low). This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle.
$\overline{\text{WR}}$	Write strobe (input, active low). This signal strobes data into the device during a write.
R/$\overline{\text{W}}$	Read/Write (input). This signal determines the direction of data transfer for a read or write cycle in conjunction with DS.
$\overline{\text{CS}}$	Chip Select (input, active low). This signal selects the device for access and must be asserted for read and write cycles, but is ignored during interrupt acknowledge and fly-by DMA transfers. In the case of a multiplexed bus interface, CS is latched by the rising edge of AS.
A/$\overline{\text{B}}$	Channel A/Channel B select (input). This signal selects between the two channels in the device. High selects channel A and low selects channel B. This signal is sampled and the result is latched during the BCR (Bus Configuration Register) write. It programs the sense of the WAIT/$\overline{\text{RDY}}$ signal appropriate for different bus interfaces. (See WAIT/$\overline{\text{RDY}}$ below.)
D/$\overline{\text{C}}$	Data/Control select (input). This signal, when high, provides for direct access to the RDR and TDR. In the case of a multiplexed bus interface, D/C high overrides the address provided to the device.
$\overline{\text{SITACK}}$	Status Interrupt Acknowledge (input, active low). This signal is a status signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle. This signal is compatible with 680x0 family microprocessors.
$\overline{\text{PITACK}}$	Pulsed Interrupt Acknowledge (input, active low). This is a strobe signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle. PITACK may be programmed to accept a single pulse or double pulse acknowledge type. This programming is done in the BCR. With the double pulse type selected, the first PITACK is recognized but no action takes place. The interrupt vector is returned on the second pulse if the no-vector option is not selected. The double pulse type is compatible with 8x86 family microprocessors.

TABLE III. Pin descriptions - Continued.

Symbol	Function
$\overline{WAIT}/\overline{RDY}$	Wait data Ready (output, active low). This signal indicates when the data is available during a read cycle, when the device is ready to receive data during a write cycle, and when a valid vector is available during an interrupt acknowledge cycle. It may be programmed to function either as a Wait signal or a Ready signal using the state of the A/B pin during the BCR write. When A/B is high during the BCR write, this signal functions as a wait output and thus supports the READY function of 8x86 family microprocessors. When A/B is low during the BCR write, this signal functions as a ready output and this supports the DTACK function of 680x0 family microprocessors.
AD15 – AD0	Address/Data bus (bidirectional, active high, three-state). The AD signals carry addresses to, and data to and from, the device. When the 16-bit non-multiplexed bus is selected, AD15 – 0 carry data to and from the device. Addresses are provided using a pointer within the device that is loaded with the desired register address. When the 8-bit non-multiplexed bus is selected without separate address, only AD7 – 0 are used to transfer data. The pointer is used for addressing; AD15 – 8 are unused. When the 8-bit non-multiplexed bus is selected with separate address, AD7 – 0 are used to transfer data, while AD15 – 8 are used as an address bus. When the 16-bit multiplexed bus is selected, addresses are latched from AD7 – 0 and data transfers are sixteen bits wide. When the 8-bit multiplexed bus is selected without separate address, only AD7 – 0 are used to transfer addresses and data; AD15 – 8 are unused. When the 8-bit multiplexed bus with separate address is selected, only AD7 – 0 are used to transfer data, while AD15 – 8 are used as an address bus.
$\overline{INTA}$, $\overline{INTB}$	Interrupt request (outputs, active low). These signals indicate that the channel has an interrupt condition pending and is requesting service. These outputs are NOT open-drained.
IEIA, IEIB	Interrupt Enable In (inputs, active high). The IEI signal for each channel is used with the accompanying IEI signal to form an interrupt daisy chain. An active IEI indicates that no device having higher priority is requesting or servicing an interrupt.
IEOA, IEOB	Interrupt Enable Out (outputs, active high). The IEO signal for each channel is used with the accompanying IEI signal to form an interrupt daisy chain. IEO is low of IEI is low, an interrupt is under service in the channel, or an interrupt is pending during an interrupt acknowledge cycle.
$\overline{TxACKA}$, $\overline{TxACKB}$	Transmit Acknowledge (inputs or outputs, active low). The primary function of these signals is to perform fly-by DMA transfers to the transmit FIFO's. Also, they can be used as bit inputs or outputs.
$\overline{RxACKA}$, $\overline{RxACKB}$	Receive Acknowledge (inputs or outputs, active low). The primary function of these signals is to perform fly-by DMA transfers from the receive FIFO's. Also, they can be used as bit inputs or outputs.
TxDA, TxDB	Transmit Data (outputs, active high, three-state). These signals carry the serial transmit data for each channel.
RxDA, RxDB	Receive Data (inputs, active high). These signals carry the serial receive data for each channel.

TABLE III. Pin descriptions - Continued.

Symbol	Function
$\overline{\text{TxCA}}$, $\overline{\text{TxCB}}$	Transmit Clock (inputs or outputs, active low). These signals are used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various transmitter signals or internal clock signals.
$\overline{\text{RxCA}}$, $\overline{\text{RxCB}}$	Receive Clock (inputs or outputs, active low). These signals are used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various receiver signals or internal clock signals.
$\overline{\text{TxREQA}}$, $\overline{\text{TxREQB}}$	Transmit Request (inputs or outputs, active low). The primary function of these signals is to request DMA transfers to the transmit FIFO's. They may also be used as simple inputs or outputs.
$\overline{\text{RxREQA}}$, $\overline{\text{RxREQB}}$	Receive Request (inputs or outputs, active low). The primary function of these signals is to request DMA transfers from the receive FIFO's. They may also be used as simple inputs or outputs.
$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$	Clear to Send (inputs or outputs, active low). These signals are used as enables for the respective transmitters. They may also be programmed to generate interrupts on either transition or be used as simple inputs or outputs.
$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$	Data Carrier Detect (inputs or outputs, active low). These signals are used as enables for the respective receivers. Also, they may be programmed to generate interrupts on either transition or be used as simple inputs or outputs.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-15

Approved sources of supply for SMD 5962-90657 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9065701MXC	0C7V7	Z16C3010GMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.