REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 and 04. Add vendor CAGE 01295. Technical and editorial changes throughout.	91-02-26	M. A. Frye
B	Correct title to accurately describe devices. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG	06-08-09	Thomas M. Hess
C	Correct footnote 3 in table I. - LTG	06-12-20	Thomas M. Hess

REV																				
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REV STATUS				REV			C	B	B	B	B	C	B	B	B	B	B	B		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

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DRAWING APPROVAL DATE
90-01-17

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, 8-BIT IDENTITY COMPARATOR, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89793**

SHEET 1 OF 12

DSCC FORM 2233
APR 97

5962-E133-07

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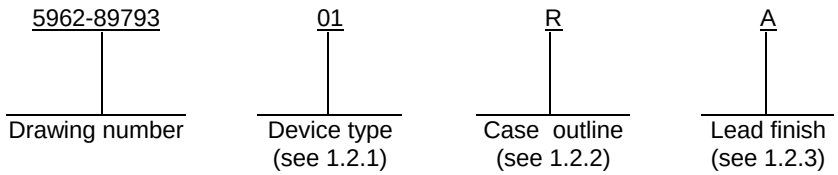
1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT520	8-bit identity comparator, TTL compatible inputs
02	54ACT521	8-bit identity comparator, TTL compatible inputs
03	54ACT11520	8-bit identity comparator, TTL compatible inputs
04	54ACT11521	8-bit identity comparator, TTL compatible inputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current (I_{IK}) ..... ±20 mA
DC output diode current (I_{OK}) (per output pin) ..... ±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) ..... ±100 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C 2/

1/ Unless otherwise specified, all voltages are referenced to GND.
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.

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1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall times (t_r, t_f):
V_{CC} = 4.5 V to 5.5 V ..... 0 to 8 ns/V

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

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3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage 1/	V_{OH}	$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OH} = -50\ \mu A$	$V_{CC} = 4.5\ V$	1, 2, 3	All	4.4		V
			$V_{CC} = 5.5\ V$			5.4		
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OH} = -24\ mA$	$V_{CC} = 4.5\ V$			3.7		
			$V_{CC} = 5.5\ V$			4.7		
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OH} = -50\ mA$	$V_{CC} = 5.5\ V$			3.85		
Low level output voltage 1/	V_{OL}	$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OL} = 50\ \mu A$	$V_{CC} = 4.5\ V$	1, 2, 3	All		0.1	V
			$V_{CC} = 5.5\ V$				0.1	
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OL} = 24\ mA$	$V_{CC} = 4.5\ V$				0.5	
			$V_{CC} = 5.5\ V$				0.5	
		$V_{IN} = V_{IH}$ min or V_{IL} max $I_{OL} = 50\ mA$	$V_{CC} = 5.5\ V$				1.65	
High level input voltage 2/	V_{IH}		$V_{CC} = 4.5\ V$	1, 2, 3	All	2.0		V
			$V_{CC} = 5.5\ V$			2.0		
Low level input voltage 2/	V_{IL}		$V_{CC} = 4.5\ V$	1, 2, 3	All		0.8	V
			$V_{CC} = 5.5\ V$				0.8	
Input leakage current, B inputs, low	I_{IL1}	$V_{IN} = 0.0\ V$	$V_{CC} = 5.5\ V$	1, 2, 3	01, 03		-1.0	mA
					02, 04		-1.0	µA
Input leakage current, B inputs, high	I_{IH1}	$V_{IN} = 5.5\ V$			01, 03		10.0	µA
					02, 04		1.0	µA
Input leakage current, other inputs, low	I_{IL2}	$V_{IN} = 0.0\ V$	$V_{CC} = 5.5\ V$	1, 2, 3	01, 03		-1.0	µA
					02, 04		-1.0	µA
Input leakage current, other inputs, high	I_{IH2}	$V_{IN} = 5.5\ V$			01, 03		1.0	µA
					02, 04		1.0	µA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5\ V$		1, 2, 3	01, 02, 04		160	µA
Quiescent supply current	I_{CC}	B inputs at GND	Other inputs = V_{CC} or GND $V_{CC} = 5.5\ V$	1, 2, 3	03		8.0	mA
		B inputs open			03		160	µA
Maximum I_{CC}/TTL inputs high, supply current	ΔI_{CC}	One input at 3.4 V, $V_{CC} = 5.5\ V$ Other inputs = V_{CC} or GND		1, 2, 3	All		1.6	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance	C_{IN}	See 4.3.1c	4	All		10	pF
Power dissipation capacitance 3/	C_{PD}	See 4.3.1c	4	All		60	pF
Functional tests		Tested at V_{CC} = 4.5 V and repeated at V_{CC} = 5.5 V See 4.3.1d	7, 8	All			
Propagation delay time, An or Bn to $\overline{O}_{A=B}$ 4/	t_{PHL1}	V_{CC} = 4.5 V C_L = 50 pF R_L = 500Ω See figure 4	9	01, 02	1.5	11.0	ns
			10, 11		1.5	12.5	
			9	03, 04	1.5	12.4	
			10, 11		1.5	14.8	
	t_{PLH1}		9	01, 02	1.5	12.0	
			10, 11		1.5	12.0	
			9	03, 04	1.5	13.0	
			10, 11		1.5	15.9	
Propagation delay time, $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ 4/	t_{PHL2}		9	01, 02	1.5	8.5	ns
			10, 11		1.5	9.0	
			9	03, 04	1.5	9.0	
			10, 11		1.5	10.4	
	t_{PLH2}		9	01, 02	1.5	8.5	
			10, 11		1.5	8.5	
			9	03, 04	1.5	9.3	
			10, 11		1.5	11.2	

1/ V_{OH} and V_{OL} will be tested at V_{CC} = 4.5 V. V_{OH} and V_{OL} are guaranteed, if not tested, for V_{CC} = 5.5 V. Limits shown apply to operation at V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

2/ The V_{IH} and V_{IL} tests are not required, and shall be applied as forcing functions for the V_{OH} and V_{OL} tests.

3/ Power dissipation capacitance (C_{PD}) determines both the dynamic power consumption (P_D) and the dynamic current consumption (I_S).
Where:
$P_D = (C_{PD} + C_L)\ (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$
$I_S = (C_{PD} + C_L)\ V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$
For both P_D and I_S, n is number of device inputs at TTL levels; f is the frequency of the input signal; d is duty cycle of the input signal; and C_L is the external output load capacitance.

4/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns.

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Device types	01 and 02	03 and 04	
Case outlines	R, S, and 2	R	2
Terminal number	Terminal symbol	Terminal symbol	Terminal symbol
1	$\overline{I_{A=B}}$	B1	B3
2	A0	A1	A3
3	B0	B0	B2
4	A1	A0	$\overline{A2}$
5	B1	GND	$\overline{I_{A=B}}$
6	A2	$\overline{O_{A=B}}$	B1
7	B2	B7	A1
8	A3	A7	B0
9	B3	B6	A0
10	GND	A6	GND
11	A4	B5	$\overline{O_{A=B}}$
12	B4	A5	B7
13	A5	B4	A7
14	B5	A4	B6
15	A6	V_{CC}	A6
16	B6	B3	B5
17	A7	A3	A5
18	$\overline{B7}$	B2	B4
19	$\overline{O_{A=B}}$	$\overline{A2}$	A4
20	V_{CC}	$\overline{I_{A=B}}$	V_{CC}

A0 – A7 = Word A inputs
$\overline{B0}$ – B7 = Word B inputs
$\overline{I_{A=B}}$ =Expansion or enable inputs
$\overline{O_{A=B}}$ = Identity output

FIGURE 1. Terminal connections.

Device types 01, 02, 03, and 04

Inputs		Outputs
$\overline{I_{A=B}}$	A, B	$\overline{O_{A=B}}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = High voltage level
L = Low voltage level
* = A0 = B0, A1 = B1, A2 = B2, . . ., A7 = B7

FIGURE 2. Truth table.

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Device types 01 and 03

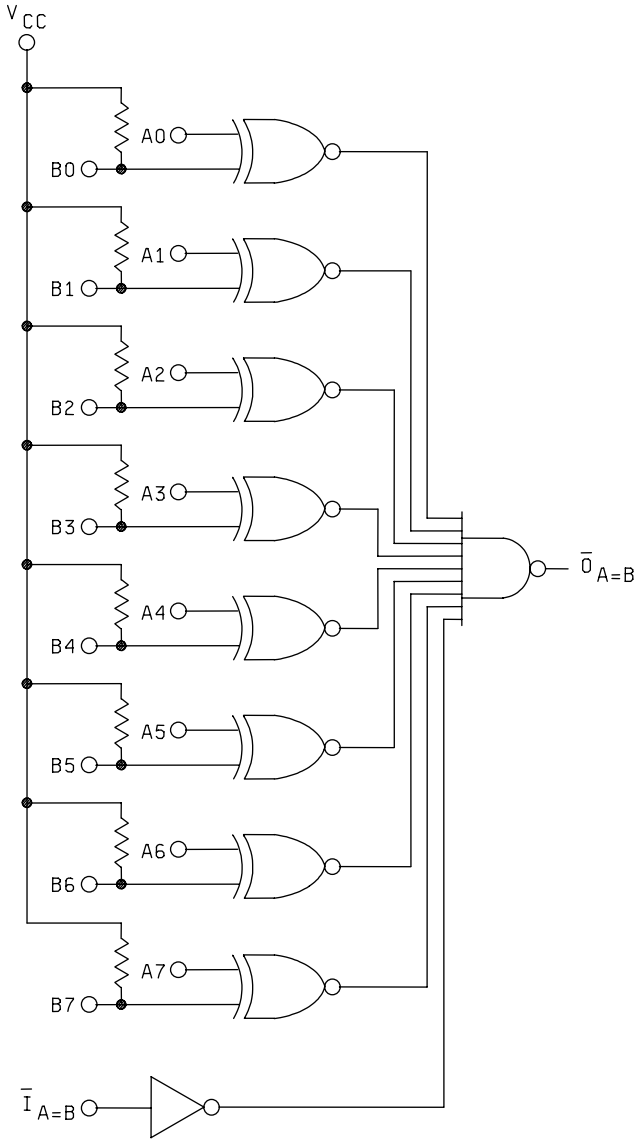

FIGURE 3. Logic diagram.

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Device types 02 and 04

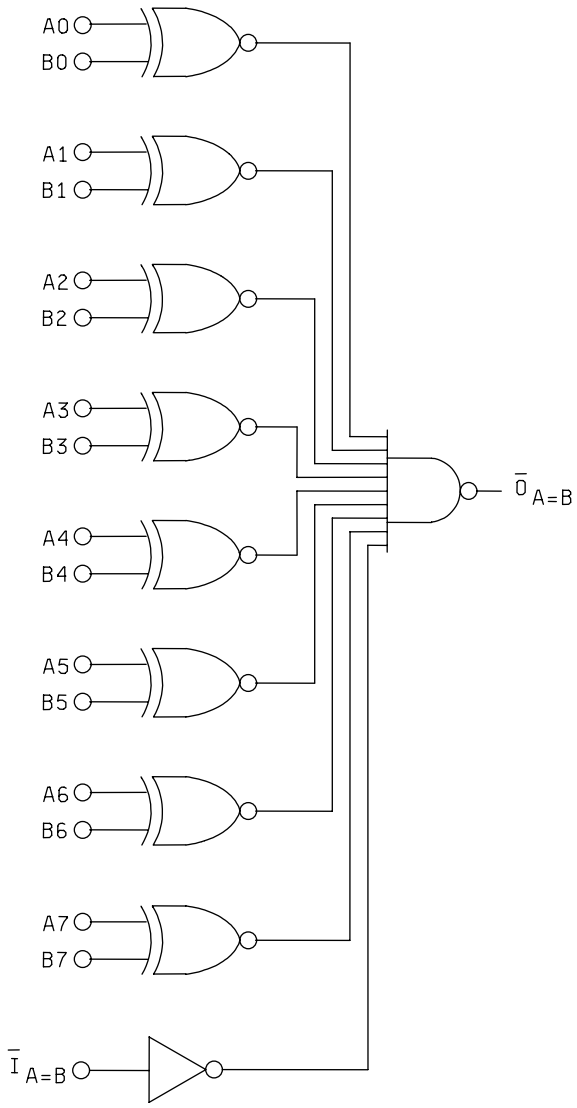

FIGURE 3. Logic diagram – Continued.

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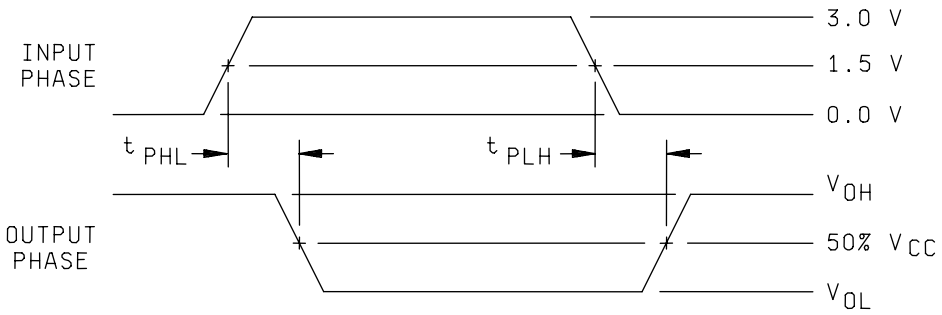

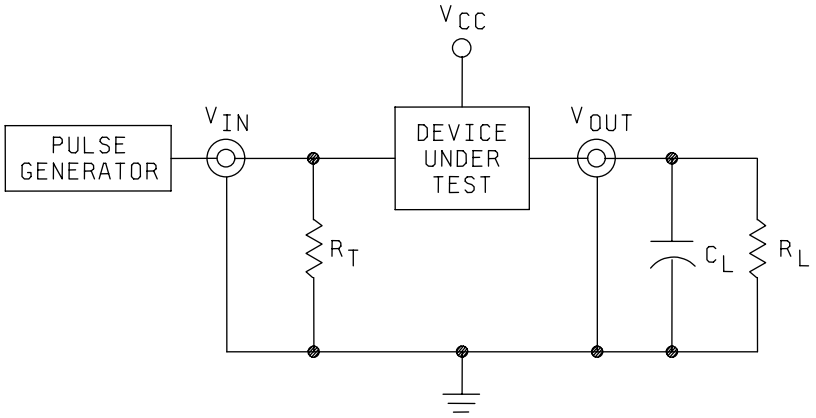

NOTES:
1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_L = 500Ω or equivalent; R_T = 50Ω or equivalent.
3. $t_r = t_f$ = 3.0 ns (10 percent to 90 percent), unless otherwise specified.

FIGURE 4. Switching waveforms and test circuit.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and V_{SS} or GND at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, and D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-12-20

Approved sources of supply for SMD 5962-89793 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8979301RA	0C7V7	54ACT520DMQB
5962-8979301SA	0C7V7	54ACT520FMQB
5962-89793012A	0C7V7	54ACT520LMQB
5962-8979302RA	0C7V7	54ACT521DMQB
5962-8979302SA	0C7V7	54ACT521FMQB
5962-89793022A	0C7V7	54ACT521LMQB
5962-8979303RA	3/	54ACT11520
5962-89793032A	3/	54ACT11520
5962-8979304RA	3V146	54ACT11521/BRA
5962-89793042A	3V146	54ACT11521/B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
3V146	Rochester Electronics 16 Malcolm Hoyt Drive Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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