| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add vendor CAGE 92527. Page 5: Changes to electrical in table I. Editorial changes throughout. | 88-03-28 | Michael A. Frye |
| B | Add vendor CAGE 75569 for device type 01. Add device type 02. Delete vendor CAGE 92527. Add case outline S for device types 01 and 02. Editorial changes throughout. Technical changes in figure 2. | 89-01-03 | Michael A. Frye |
| C | Technical changes in table I. Add vendor CAGE 27014 and 9Z527 for device type 01. Add vendor CAGE 75569 for device type 02 and 01SX. Editorial changes throughout. - mbk | 89-11-29 | Michael A. Frye |
| D | Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. – jak | 06-07-11 | Thomas M. Hess |
| E | Correct test condition for total supply current ($I_{CCT}$) and add footnote 5/ in table I. Update boilerplate paragraphs as specified in current requirements of MIL-PRF-38535. – MAA. | 09-12-24 | Thomas M. Hess |

| | | | | | | | | | | | | | | | | | | | |
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| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | |

PMIC N/A

PREPARED BY
Marcia B. Kelleher

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

CHECKED BY
Raymond Monnin

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

APPROVED BY
Michael A. Frye

MICROCIRCUIT, DIGITAL, FAST CMOS, OCTAL NONINVERTING D-TYPE FLIP-FLOP WITH THREE-STATE OUTPUTS AND TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

DRAWING APPROVAL DATE
87-11-30

AMSC N/A

REVISION LEVEL
E

| SIZE | CAGE CODE | |
|---|---|---|
| **A** | **67268** | **5962-87628** |

SHEET 1 OF 11

DSCC FORM 2233
APR 97

5962-E128-10

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

| 5962-87628 | 01 | R | A |
|---|---|---|---|
| Drawing number | Device type (see 1.2.1) | Case outline (see 1.2.2) | Lead finish (see 1.2.3) |

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54FCT374 | Octal non-inverting D-type flip-flop with three-state outputs, TTL compatible inputs |
| 02 | 54FCT374A | Octal non-inverting D-type flip-flop with three-state outputs, TTL compatible inputs |

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| R | GDIP1-T20 or CDIP2-T20 | 20 | Dual-in-line |
| S | GDFP2-F20 or CDFP3-F20 | 20 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | -0.5 V dc to +6.0 V dc |
| DC input voltage range ($V_{IN}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC output voltage range ($V_{OUT}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC input diode current ($I_{IK}$) | -20 mA |
| DC output diode current ($I_{OK}$) | -50 mA |
| DC output current ($I_{OUT}$) | ±100 mA |
| Maximum power dissipation ($P_D$) 2/ | 500 mW |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | See MIL-STD-1835 |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Junction temperature ($T_J$) | +175°C |
| Lead temperature (soldering, 10 seconds) | +300°C |

1.4 Recommended operating conditions. 1/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Maximum low level input voltage ($V_{IL}$) | 0.8 V |
| Minimum high level input voltage ($V_{IH}$) | 2.0 V |
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Minimum setup time, Dn to CP ($t_s$) | 2.5 ns |
| Minimum hold time, Dn to CP ($t_h$) | 2.5 ns |
| Minimum clock pulse width ($t_w$) | 7.0 ns |

1/ Unless other wise specified, all voltages are referenced to ground.

2/ Must withstand the added $P_D$ due to short circuit test; e.g., $I_{OS}$.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{CC}$ = 5.0 V dc ± 10%<br>unless otherwise specified | | $V_{CC}$ | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| High level output voltage | $V_{OH}$ | $V_{IL}$ = 0.8 V<br>$V_{IH}$ = 2.0 V | $I_{OH}$ = -300 µA | 4.5 V | All | 1, 2, 3 | 4.3 | | V |
| | | | $I_{OH}$ = -12 mA | | | | 2.4 | | |
| Low level output voltage | $V_{OL}$ | $V_{IL}$ = 0.8 V<br>$V_{IH}$ = 2.0 V | $I_{OL}$ = +300 µA | 4.5 V | All | 1, 2, 3 | | 0.2 | V |
| | | | $I_{OL}$ = +32 mA | | | | | 0.5 | |
| Input clamp voltage | $V_{IK}$ | $I_{IN}$ = -18 mA | | 4.5 V | All | 1, 2, 3 | | -1.2 | V |
| High level input current | $I_{IH}$ | $V_{IN}$ = 5.5 V | | 5.5 V | All | 1, 2, 3 | | 5.0 | µA |
| Low level input current | $I_{IL}$ | $V_{IN}$ = GND | | 5.5 V | All | 1, 2, 3 | | -5.0 | µA |
| High impedance output current | $I_{OZH}$ | $V_{IN}$ = 5.5 V | | 5.5 V | All | 1, 2, 3 | | 10.0 | µA |
| | $I_{OZL}$ | $V_{IN}$ = GND | | 5.5 V | All | 1, 2, 3 | | -10.0 | µA |
| Short circuit output current | $I_{OS}$<br>1/ | $V_{OUT}$ = GND | | 5.5 V | All | 1, 2, 3 | -60 | | mA |
| Quiescent power supply current (CMOS inputs) | $I_{CCQ}$ | $V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V<br>$f_i$ = 0 MHz | | 5.5 V | All | 1, 2, 3 | | 1.5 | mA |
| Quiescent power supply current (TTL inputs) | $\Delta I_{CC}$<br>2/ | $V_{IN}$ = 3.4 V | | 5.5 V | All | 1, 2, 3 | | 2.0 | mA |
| Dynamic power supply current | $I_{CCD}$ | Outputs open, $\overline{OE}$ = GND<br>One bit toggling,<br>50% duty cycle<br>$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V | | 5.5 V | All | 3/ | | 0.4 | mA/ MHz |
| Total power supply current | $I_{CC}$<br>4/ 5/ | $V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V<br>$f_{CP}$ = 10 MHz<br>Outputs open, $\overline{OE}$ = GND<br>One bit toggling at $f_i$ = 5 MHz<br>50% duty cycle | | 5.5 V | All | 1, 2, 3 | | 5.5 | mA |
| | | $V_{IN}$ = 3.4 V or $V_{IN}$ = GND<br>$f_{CP}$ = 10 MHz<br>Outputs open, $\overline{OE}$ = GND<br>Eight bits toggling at<br>$f_i$ = 2.5 MHz<br>50% duty cycle | | 5.5 V | All | 1, 2, 3 | | 6.0 | mA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{CC}$ = 5.0 V dc ± 10%<br>unless otherwise specified | $V_{CC}$ | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Input capacitance | $C_{IN}$ | See 4.3.1c | | All | 4 | | 10 | pF |
| Input capacitance | $C_{OUT}$ | See 4.3.1c | | All | 4 | | 12 | pF |
| Functional tests | | See 4.3.1d | 4.5 V | All | 7, 8 | | | |
| Propagation delay time, CP to Qn | $t_{PHL}$, $t_{PLH}$ 6/ | $C_L$ = 50 pF<br>$R_L$ = 500Ω<br>See figure 4 | 4.5 V | 01 | 9, 10, 11 | 2.0 | 11.0 | ns |
| | | | | 02 | 9, 10, 11 | 2.0 | 7.2 | |
| Propagation delay time, output enable, $\overline{OE}$ to Qn | $t_{PZH}$, $t_{PZL}$ 6/ | | 4.5 V | 01 | 9, 10, 11 | 1.5 | 14.0 | ns |
| | | | | 02 | 9, 10, 11 | 1.5 | 7.5 | |
| Propagation delay time, output disable, $\overline{OE}$ to Qn | $t_{PHZ}$, $t_{PLZ}$ 6/ | | 4.5 V | 01 | 9, 10, 11 | 1.5 | 8.0 | ns |
| | | | | 02 | 9, 10, 11 | 1.5 | 6.5 | |

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed 1 second.

2/ For TTL driven inputs, $V_{IN}$ = 3.4 V; all other inputs are equal to $V_{CC}$ or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} D_H N_T) + I_{CCD}(f_{CP}/2 + f_i N_i)$, where: $D_H$ = duty cycle for TTL input high; $N_T$ = number of TTL inputs at $D_H$; $f_i$ = input frequency in MHz; $N_i$ = number of inputs at $f_i$; $f_{CP}$ = clock frequency in MHz.

5/ For total current supply ($I_{CCT}$) test in an ATE environment, the effect of parasitic output capacitive loading from the test environment must be taken into account, as its effect is not intended to be included in the test results. The impact must be characterized and appropriate offset factors must be applied to the test result.

6/ The minimum limits are guaranteed; if not tested, to the specified limits in table I

.

| Device types | 01 and 02 |
|---|---|
| Case outlines | R, S, and 2 |
| Terminal number | Terminal symbol |
| 1 | $\overline{OE}$ |
| 2 | $Q_0$ |
| 3 | $D_0$ |
| 4 | $D_1$ |
| 5 | $Q_1$ |
| 6 | $Q_2$ |
| 7 | $D_2$ |
| 8 | $D_3$ |
| 9 | $Q_3$ |
| 10 | GND |
| 11 | CP |
| 12 | $Q_4$ |
| 13 | $D_4$ |
| 14 | $D_5$ |
| 15 | $Q_5$ |
| 16 | $Q_6$ |
| 17 | $D_6$ |
| 18 | $D_7$ |
| 19 | $Q_7$ |
| 20 | $V_{CC}$ |

FIGURE 1. Terminal connections.

| Function | Inputs | | | Outputs |
|---|---|---|---|---|
| High-Z | $\overline{OE}$ | CP | Dn | Qn |
| | H | L | X | Z |
| | H | H | X | Z |
| Load register | L | ↑ | L | L |
| | L | ↑ | H | H |
| | H | ↑ | L | Z |
| | H | ↑ | H | Z |

L = Low voltage level
H = High voltage level
Z = High impedance
X = Don't care
↑ = Low-to-high transition of the clock

FIGURE 2. Truth table.

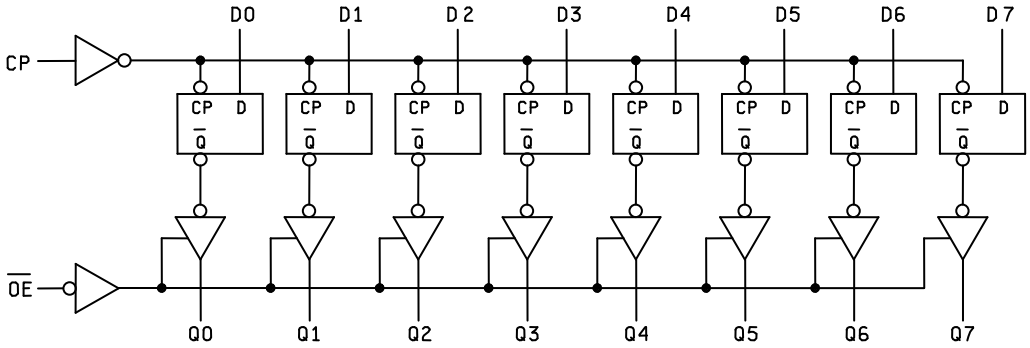



FIGURE 3. Logic diagram.

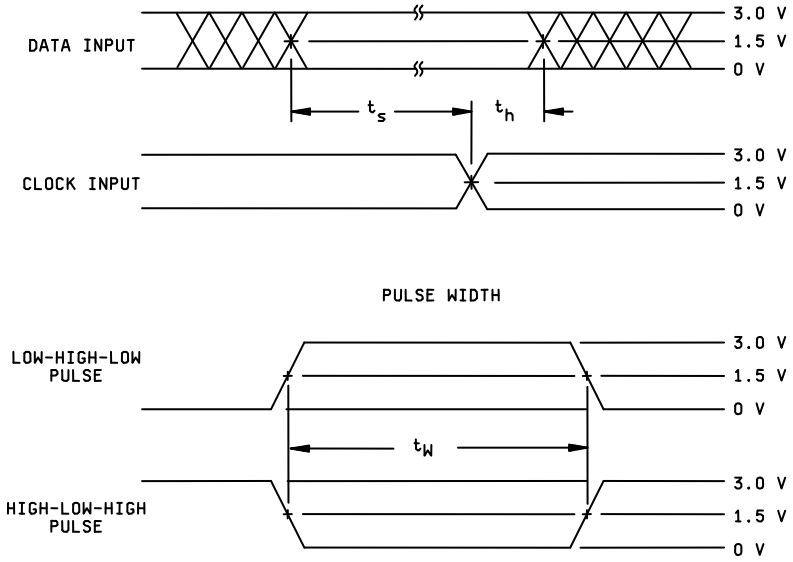
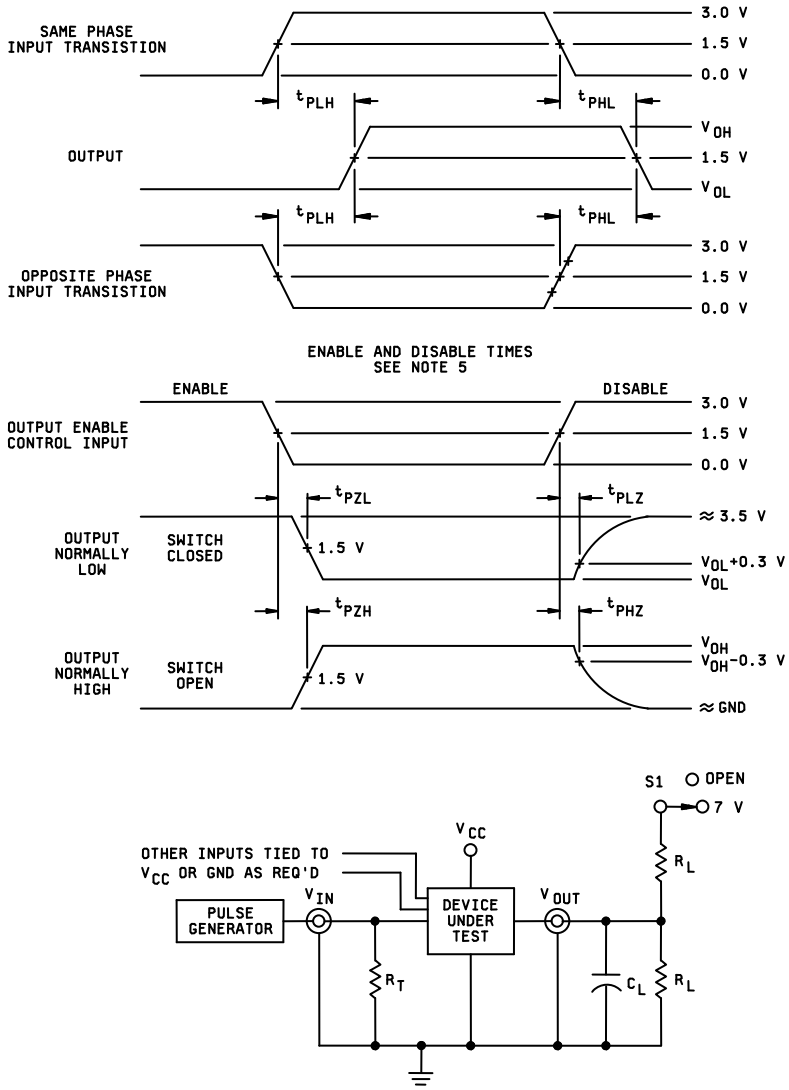



FIGURE 4. Switching waveforms and test circuit.




NOTES:

1. When measuring $t_{PLH}$, $t_{PHL}$, $t_{PZH}$, and $t_{PHZ}$: S1 = Open.
   When measuring $t_{PLZ}$ and $t_{PZL}$: S1 = Closed.
2. $R_L$ = 500Ω or equivalent.
3. $R_T$ = 50Ω or equivalent, terminal resistance which should be equal to $Z_{OUT}$ of the pulse generator.
4. $C_L$ = 50 pF or equivalent (includes test jig and probe capacitance).
5. Diagram shown for input control enable-low and input control disable-high.
6. Pulse generator for all pulses: $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns.

FIGURE 4. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | - - - |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroup 7 and 8 tests shall include verification of the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-12-24

Approved sources of supply for SMD 5962-87628 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8762801RA | 0C7V7 | 54FCT374DMQB |
| | | IDT54FCT374DB |
| 5962-8762801SA | 0C7V7 | 54FCT374FMQB |
| | | IDT54FCT374EB |
| 5962-87628012A | 0C7V7 | 54FCT374LMQB |
| | | IDT54FCT374LB |
| 5962-8762802RA | 0C7V7 | IDT54FCT374ADB |
| 5962-8762802SA | 0C7V7 | IDT54FCT374AEB |
| 5962-87628022A | 0C7V7 | IDT54FCT374ALB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 0C7V7 | QP Semiconductor<br>2945 Oakmead Village Court<br>Santa Clara, CA 95051 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.