REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Terminal connections changed to table form. Change drawing CAGE code to 67268. Add figure 4. Technical change to 1.4. Technical changes to tables I and II. Editorial changes throughout document.	89-03-20	M. A. Frye
B	Changes in accordance with NOR 5962-R047-92	91-12-02	M. A. Frye
C	Revise for “QD” certification. New boilerplate. Editorial changes throughout. - ljs	00-02-16	Raymond Monnin
D	Update to current requirements. Editorial changes throughout. gap	06-04-06	Raymond Monnin

The original first page of this drawing has been replaced.

REV																				
SHEET																				
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REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D			
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A	PREPARED BY Larry T. Gauder	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Wm. J. Johnson	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, DIGITAL,ECL, QUAD EXCLUSIVE-OR GATE, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 87-04-10	
	REVISION LEVEL D	SIZE A CAGE CODE **67268** **5962-87558**
		SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87558	01	E	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	10H513	Quad EXCLUSIVE-OR gate

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1T-16 or CDIP2-T16	16	dual-in-line
F	GDFP2-F16 or GDFP3-F16	16	flat package
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{EE})	-8.0 V dc minimum to 0.0 V dc
Input voltage range	-5.2 V to 0.0 V dc
Storage temperature range	-65°C to +165°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+165°C
Maximum power dissipation (P_D)	275 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{EE})	-5.46 V minimum to -4.94 V maximum
Supply voltge range (V_{CC})	-0.02 V to 0.02 V or 1.98 V to 2.02 V
Ambient operating temperature range (T_A)	-55°C to +125°C
Minimum high level input voltage (V_{IH}):	
T_A = +25°C	-0.780 V dc
T_A = +125°C	-0.650 V dc
T_A = -55°C	-0.840 V dc
Maximum low level input voltage (V_{IL})	-1.950 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil;quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A. For class Q product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer's Quality Management (QM) Plan, the "QD" certification mark shall be used in place of the "QML" or "Q" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{IH}	V_{IL}	Group A subgroups	Limits Min	Limits Max	Unit
Quiescent conditions 1/								
High level output voltage	V_{OH}	Outputs terminated through 100Ω to -2.0 V V_{EE} = -5.2 V V_{CC} = 0.0 V	-0.780	-1.950	1	-1.010	-0.780	V
			-0.650	-1.950	2	-0.860	-0.650	
			-0.840	-1.950	3	-1.060	-0.840	
Low level output voltage	V_{OL}		-0.780	-1.950	1	-1.950	-1.580	V
			-0.650	-1.950	2	-1.950	-1.565	
			-0.840	-1.950	3	-1.950	-1.610	
High level threshold output voltage	V_{OHA}	2/	-1.110	-1.480	1	-1.010	-0.780	V
			-0.960	-1.465	2	-0.860	-0.650	
			-1.160	-1.510	3	-1.060	-0.840	
Low level threshold output voltage	V_{OLA}		-1.110	-1.480	1	-1.950	-1.580	V
			-0.960	-1.465	2	-1.950	-1.565	
			-1.160	-1.510	3	-1.950	-1.610	
Power supply drain current 3/	I_{EE}	V_{EE} = -5.46 V, V_{CC} = 0.0 V,			1	-42		mA
					2, 3	-46		
High level input current	I_{IH1}	V_{IH} = -0.780 V at +25°C = -0.650 V at +125°C = -0.840 V at -55°C	B inputs		1		270	µA
					2, 3		430	
	I_{IH2}		A inputs		1		320	µA
					2, 3		510	
	I_{IH3}		$\overline{E}$		1		740	µA
					2, 3		1100	
Low level input current	I_{IL}	V_{EE} = -4.94 V, V_{CC} = 0.0 V V_{IL} = -1.950 V 3/			1, 3	0.5		µA
					2	0.3		
Functional tests		See 4.3.1c			7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Cases E and F		DC rapid test conditions 4/						
High level output voltage	V_{OH}	Outputs terminated through 100 Ω to -2.0 V	V_{IH} -0.792	V_{IL} -1.950	1	-1.021	-0.792	V
			-0.663	-1.950	2	-0.872	-0.663	
			-0.853	-1.950	3	-1.072	-0.853	
Low level output voltage	V_{OL}	V_{EE} = -5.2 V V_{CC} = 0.0 V	-0.792	-1.950	1	-1.950	-1.584	V
			-0.663	-1.950	2	-1.950	-1.569	
			-0.853	-1.950	3	-1.950	-1.614	
High level threshold output voltage	V_{OHA}	2/	-1.121	-1.484	1	-1.021	-0.792	V
			-0.972	-1.469	2	-0.872	-0.633	
			-1.172	-1.514	3	-1.072	-0.853	
Low level threshold output voltage	V_{OLA}		-1.121	-1.484	1	-1.950	-1.584	V
			-0.972	-1.469	2	-1.950	-1.569	
			-1.172	-1.514	3	-1.950	-1.614	
Power supply drain current 3/	I_{EE}	V_{EE} = -5.46 V, V_{CC} = 0.0 V,			1	-41		mA
					2, 3	-45		
High level input current	I_{IH1}	V_{IH} = -0.792 V at +25°C = -0.663 V at +125°C = -0.853 V at -55°C	B inputs		1		255	µA
					2, 3		415	
	I_{IH2}		A inputs		1		305	µA
					2, 3		495	
	I_{IH3}		$\overline{E}$		1		725	µA
					2, 3		1085	
Low level input current	I_{IL}	V_{EE} = -4.94 V, V_{CC} = 0.0 V V_{IL} = -1.950 V 3/			1, 3	0.5		µA
					2	0.3		
Functional tests		See 4.3.1c			7, 8			
Case 2		DC rapid test conditions 4/						
High level output voltage	V_{OH}	Outputs terminated through 100 Ω to -2.0 V	-0.797	-1.950	1	-1.026	-0.797	V
			-0.669	-1.950	2	-0.877	-0.669	
			-0.859	-1.950	3	-1.077	-0.859	
Low level output voltage	V_{OL}	V_{EE} = -5.2 V V_{CC} = 0.0 V	-0.797	-1.950	1	-1.950	-1.585	V
			-0.669	-1.950	2	-1.950	-1.571	
			-0.859	-1.950	3	-1.950	-1.616	
High level threshold output voltage	V_{OHA}	2/	-1.126	-1.485	1	-1.026	-0.797	V
			-0.977	-1.471	2	-0.877	-0.669	
			-1.177	-1.516	3	-1.077	-0.859	
Low level threshold output voltage	V_{OLA}		-1.126	-1.485	1	-1.950	-1.585	V
			-0.977	-1.471	2	-1.950	-1.571	
			-1.177	-1.516	3	-1.950	-1.616	

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Power supply drain current 3/	I_{EE}	V_{EE} = -5.46 V V_{CC} = 0.0 V		1	-41		mA
				2, 3	-45		
High level input current	I_{IH1}	V_{IH} = -0.797 V at +25°C = -0.669 V at +125°C = -0.859 V at -55°C	B inputs	1		255	µA
				2, 3		415	
	I_{IH2}		A inputs	1		305	µA
				2, 3		495	
	I_{IH3}		$\overline{E}$	1		725	µA
				2, 3		1085	
Low level input current	I_{IL}	V_{EE} = -4.94 V, V_{CC} = 0.0 V V_{IL} = -1.950 V 3/		1, 3	0.5		µA
				2	0.3		
Functional tests		See 4.3.1c		7, 8			
Cases E, F, and 2		AC test conditions					
Transition time	t_{TLH} t_{THL}	V_{EE} = -2.94 V V_{CC} = 2.0 V $C_L \le 5$ pF		9	0.60	1.90	ns
				10	0.60	2.00	ns
				11	0.50	1.80	ns
Propagation delay time, Any input to Y	t_{PHH}, t_{PLL}	Load all outputs through 100 Ω to GND		9	0.40	2.40	ns
	t_{PHL}, t_{PLH}			10	0.50	2.50	ns
		See figure 4		11	0.40	2.30	ns

1/ The quiescent limits are determined after a device has reached thermal equilibrium. This is defined as the reading taken with the device in a socket with ≥ 500 LFPM of +25°C, +125°C or -55°C (as applicable) air blowing on the unit in a transverse direction with power applied for at least 4 minutes before the reading is taken. This method was used for theoretical limit establishment only. All devices shall be tested to the delta V (rapid test) conditions specified herein. The rapid test method is an equivalent method of testing quiescent conditions.

2/ The high and low level output current varies with temperature, and shall be calculated using the following formulas:

$I_{OH} = (-2.0\ V - V_{OH})/100\Omega$
$I_{OL} = (-2.0\ V - V_{OL})/100\Omega$

3/ The I_{EE} and I_{IL} limits, although specified in the minimum column, shall not be exceeded, in magnitude, as a maximum value.

4/ The dc rapid test forcing functions and limits are used for all dc testing. These limits are determined for each device type based on the power dissipation and package type. The rapid test (delta V) limits and forcing functions are skewed allowing rapid testing to be performed at standard temperatures without the addition of delta T's.

Device type	01		
Case outlines	E	F	2
Terminal number	Terminal symbol		
1	V_{CC1}	B4	NC
2	Y1	Y3	V_{CC1}
3	Y2	Y4	Y1
4	A1	V_{CC2}	Y2
5	B1	V_{CC1}	A1
6	A2	Y1	NC
7	B2	Y2	B1
8	V_{EE}	A1	A2
9	$\overline{E}$	B1	B2
10	A3	A2	V_{EE}
11	B3	B2	NC
12	A4	V_{EE}	$\overline{E}$
13	B4	$\overline{E}$	A3
14	Y3	A3	B3
15	Y4	B3	A4
16	V_{CC2}	A4	NC
17	---	---	B4
18	---	---	Y3
19	---	---	Y4
20	---	---	V_{CC2}

NC = No connection

FIGURE 1. Terminal connections.

Inputs		Enable	Output
A	B	$\overline{E}$	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
X	X	H	L

L = Low level voltage
H = High level voltage
X = Irrelevant

FIGURE 2. Truth table.

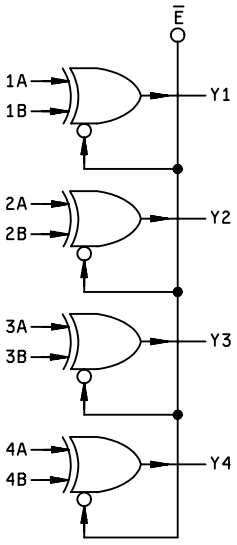
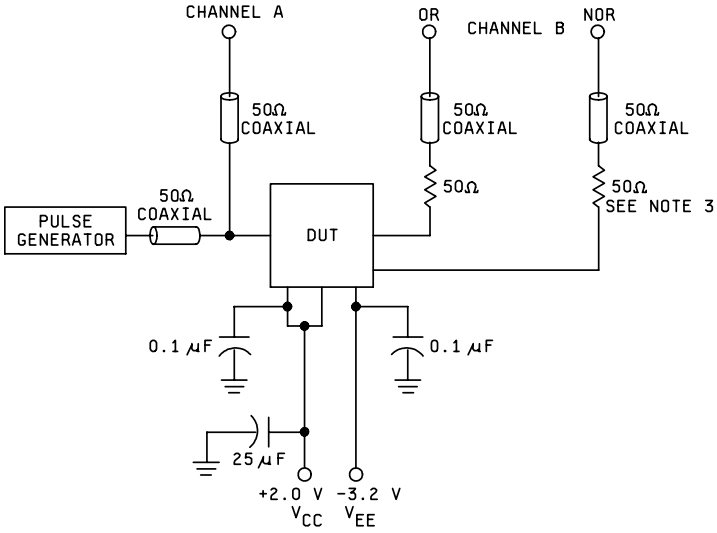


FIGURE 3. Logic diagram.

NOTES:
1. Pulse generator characteristics: PRR = 1 MHz, $t_{THL} = t_{TLH} = 1.0 \pm 2.0$ ns (20% to 80%), duty cycle = 50%.
2. All other outputs are loaded through 100 Ω to GND.
3. The 50 Ω resistor in series with the 50 Ω coaxial constitutes the 100 Ω load.



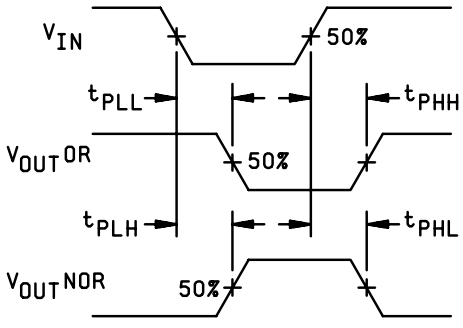


FIGURE 4. Test circuit and switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall verify the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-04-06

Approved sources of supply for SMD 5962-87558 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8755801EA	0C7V7	10H513/EA
	3/	10H513/BEAJC
5962-8755801FA	0C7V7	10H513/FA
	3/	10H513/BFAJC
5962-87558012A	0C7V7	10H513/2A
	3/	10H513M/B2AJC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.