REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add packages J and 3 for device type 02. Editorial changes throughout.	93-02-16	Monica L. Poelking
B	Update to current requirements. Editorial changes throughout. - gap	06-01-05	Raymond Monnin

CURRENT CAGE CODE 67268

The original first page of this drawing has been replaced.

REV																				
SHEET																				
REV	B																			
SHEET	15																			

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
Nelson A. Hauck

DRAWING APPROVAL DATE
86-10-06

MICROCIRCUIT, DIGITAL,ADVANCED, SCHOTTKY TTL, ARITHMETIC LOGIC UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-86710**

REVISION LEVEL
B

SHEET 1 OF 15

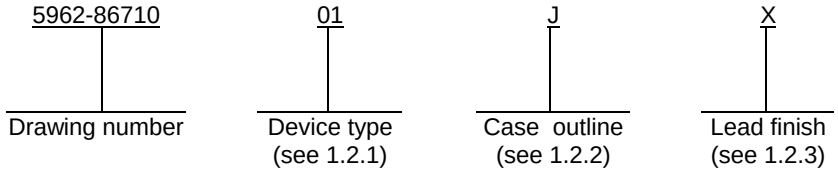
DSCC FORM 2233
APR 97

5962-E084-06

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F381	4-bit arithmetic logic unit
02	54F181	4-bit arithmetic logic unit

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line package
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20	Flat package
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +7.0 V dc
Input voltage range ..... -1.5 V dc at -18 mA to +7.0 V dc
Storage temperature ..... -65°C to +150°C
Maximum power dissipation (P_D) per device 1/ ..... 490 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH}) ..... +2.0 V dc
Maximum low level input voltage (V_{IL}) ..... +0.8 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil;quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1.0 mA, V_{IN} = 0.8 V or 2.0 V		1,2,3	All	2.5		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IN} = 0.8 V or 2.0 V		1,2,3	All		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA, T_C = +25°C		1	All		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1,2,3	All		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V		1,2,3	All		100	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.5 V	S_0-S_2 inputs	1,2,3	01		-0.6	mA
			Other inputs				-2.4	
			M input	1,2,3	02		-0.6	
			An, Bn inputs				-1.8	
			Sn inputs				-2.4	
			Cn inputs				-3.0	
Short circuit output current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.0 V 1/		1,2,3	All	-60	-150	mA
Supply current	I_{CC}	V_{CC} = 5.5 V, S_0-S_3 = GND, Other inputs high		1,2,3	01		89	mA
					02		65	
Functional tests		See 4.3.1c		7	All			
Propagation delay time, Cn to F_1	t_{PLH1}	V_{CC} = 5.0 V, R_L = 500Ω, C_L = 50 pF minimum, See figure 4.		9	01		12	ns
				10, 11			15	
	t_{PHL1}			9	01		8	ns
				10, 11			12	
Propagation delay time, Cn to $\overline{F}n$	t_{PLH2}			9	02	3.0	8.5	ns
				10, 11		2.5	16.0	
	t_{PHL2}			9	02	3.0	8.5	ns
				10, 11		2.5	12.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, any A or B to any F	t_{PLH3}	V_{CC} = 5.0 V R_L = 500Ω C_L = 50 pF minimum See figure 4.	9	01		15	ns
			10, 11			19	
	t_{PHL3}		9	01		13	ns
			10, 11			16	
Propagation delay time, any $\overline{A}$ or $\overline{B}$ to any $\overline{F}$ (mode = sum)	t_{PLH4}		9	02	4.0	10.5	ns
			10, 11		3.5	16.5	
	t_{PHL4}		9	02	4.0	10.0	ns
			10, 11		4.0	13.5	
Propagation delay time, any $\overline{A}$ or $\overline{B}$ to any $\overline{F}$ (mode = dif)	t_{PLH5}		9	02	4.0	12.0	ns
			10, 11		3.5	17.5	
	t_{PHL5}		9	02	3.0	12.0	ns
			10, 11		3.0	14.0	
Propagation delay time, S_1 to F_1	t_{PLH6}		9	01		20	ns
			10, 11			24	
	t_{PHL6}		9	01		14	ns
			10, 11			17	
Propagation delay time, A_1 or B_1 to $\overline{G}$	t_{PLH7}		9	01		12	ns
			10, 11			14	
	t_{PHL7}		9	01		10	ns
			10, 11			14	
Propagation delay time, $\overline{A}$ or $\overline{B}$ to $\overline{G}$ (mode = sum)	t_{PLH8}		9	02	2.5	7.5	ns
			10, 11		2.5	9.0	
	t_{PHL8}		9	02	2.5	7.5	ns
			10, 11		2.5	9.5	
Propagation delay time, $\overline{A}$ or $\overline{B}$ to $\overline{G}$ (mode = dif)	t_{PLH9}		9	02	3.0	9.0	ns
			10, 11		2.5	11.5	
	t_{PHL9}		9	02	2.5	9.5	ns
			10, 11		2.5	11.0	
Propagation delay time, A_1 or B_1 to $\overline{P}$	t_{PLH10}		9	01		11	ns
			10, 11			15	
	t_{PHL10}		9	01		10	ns
			10, 11			13	
Propagation delay time, $\overline{A}$ or $\overline{B}$ to $\overline{P}$ (mode = sum)	t_{PLH11}		9	02	2.5	7.0	ns
			10, 11		2.5	8.5	
	t_{PHL11}		9	02	3.0	7.5	ns
			10, 11		3.0	9.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, $\overline{A}$ or $\overline{B}$ to $\overline{P}$ (mode = dif)	t_{PLH12}	V_{CC} = 5.0 V R_L = 500Ω C_L = 50 pF minimum See figure 4.	9	02	2.5	8.0	ns
			10, 11		2.5	11.0	
	t_{PHL12}		9	02	3.0	8.5	ns
			10, 11		3.0	11.0	
Propagation delay time, S_1 to $\overline{G}$ or $\overline{P}$	t_{PLH13}		9	01		14	ns
			10, 11			19	
	t_{PHL13}		9	01		14	ns
			10, 11			19	
Propagation delay time, $\overline{A}$ or $\overline{B}$ to A = B (mode = dif)	t_{PLH14}		9	02	11	27	ns
			10, 11		8	35	
	t_{PHL14}		9	02	5.5	13.5	ns
			10, 11		5.5	21.0	
Propagation delay time, $\overline{Ai}$ or $\overline{Bi}$ to $\overline{Fi}$ (mode = sum)	t_{PLH15}		9	02	3.0	9.0	ns
			10, 11		3.0	14.5	
	t_{PHL15}		9	02	3.0	10.0	ns
			10, 11		3.0	14.5	
Propagation delay time, $\overline{Ai}$ or $\overline{Bi}$ to $\overline{Fi}$ (mode = dif)	t_{PLH16}		9	02	3.0	11.0	ns
			10, 11		3.0	17.5	
	t_{PHL16}		9	02	3.0	11.0	ns
			10, 11		3.0	14.5	
Propagation delay time, $\overline{A}$ or $\overline{B}$ to Cn+4 (mode = sum)	t_{PLH17}		9	02	5.0	13.0	ns
			10, 11		5.0	15.5	
	t_{PHL17}		9	02	3.5	12.0	ns
			10, 11		3.5	16.5	
Propagation delay time, $\overline{A}$ or $\overline{B}$ to Cn+4 (mode = dif)	t_{PLH18}		9	02	5.0	14.0	ns
			10, 11		5.0	17.0	
	t_{PHL18}		9	02	5.0	13.0	ns
			10, 11		4.0	15.0	
Propagation delay time, Cn to Cn+4	t_{PLH19}		9	02	3.0	8.5	ns
			10, 11		3.0	10.0	
	t_{PHL19}		9	02	3.0	8.0	ns
			10, 11		3.0	9.5	
Propagation delay time, $\overline{A}$ or $\overline{B}$ to $\overline{F}$ (mode = logic)	t_{PLH20}		9	02	3.5	9.5	ns
			10, 11		3.5	14.5	
	t_{PHL20}		9	02	3.0	10.0	ns
			10, 11		3.0	15.5	

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed 1 second.

Device type	01	02	02
Case outline	R, S, 2	J	3
Terminal number	Terminal symbol		
1	A_1	$\overline{B}_0$	NC
2	B_1	$\overline{A}_0$	$\overline{B}_0$
3	A_0	S_3	$\overline{A}_0$
4	B_0	S_2	S_3
5	S_0	S_1	S_2
6	S_1	S_0	S_1
7	S_2	Cn	S_0
8	F_0	M	NC
9	F_1	$\overline{F}_0$	Cn
10	GND	$\overline{F}_1$	M
11	F_2	$\overline{F}_2$	$\overline{F}_0$
12	F_3	GND	$\overline{F}_1$
13	$\overline{G}$	$\overline{F}_3$	$\overline{F}_2$
14	$\overline{P}$	A = B	GND
15	Cn	$\overline{P}$	NC
16	B_3	Cn+4	$\overline{F}_3$
17	A_3	$\overline{G}$	A = B
18	B_2	$\overline{B}_3$	$\overline{P}$
19	A_2	$\overline{A}_3$	Cn+4
20	V_{CC}	$\overline{B}_2$	$\overline{G}$
21	---	$\overline{A}_2$	$\overline{B}_3$
22	---	$\overline{B}_1$	NC
23	---	$\overline{A}_1$	$\overline{A}_3$
24	---	V_{CC}	$\overline{B}_2$
25	---	---	$\overline{A}_2$
26	---	---	$\overline{B}_1$
27	---	---	$\overline{A}_1$
28	---	---	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

Device type 01

	Inputs						Outputs					
Function	S_0	S_1	S_2	Cn	An	Bn	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
Clear	0	0	0	X	X	X	0	0	0	0	0	0
B minus A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	1	0	0
				1	0	1	1	1	1	0	0	1
				1	1	0	1	0	0	0	1	0
				1	1	1	0	0	0	0	1	0
A minus B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A plus B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A ⊕ B	0	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
Preset	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

1 = High voltage level
0 = Low voltage level
X = Immaterial

FIGURE 2. Truth tables.

Device type 02

Selection				Active low data and Fn outputs		
				Logic function (M = H)	Arithmetic operations (M = H)	
S3	S2	S1	S0		Cn = inactive (no carry)	Cn = active (carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A+B}$	F = A PLUS ($\overline{A+B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS(A + B)	F = A PLUS(A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

Selection				Active high data and Fn outputs		
				Logic function (M = H)	Arithmetic operations (M = H)	
S3	S2	S1	S0		Cn = inactive (no carry)	Cn = active (carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS $\overline{A}$B	F = (A + B) PLUS $\overline{A}$B PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

H = High voltage level
L = Low voltage level

FIGURE 2. Truth tables - Continued.

Device type 01

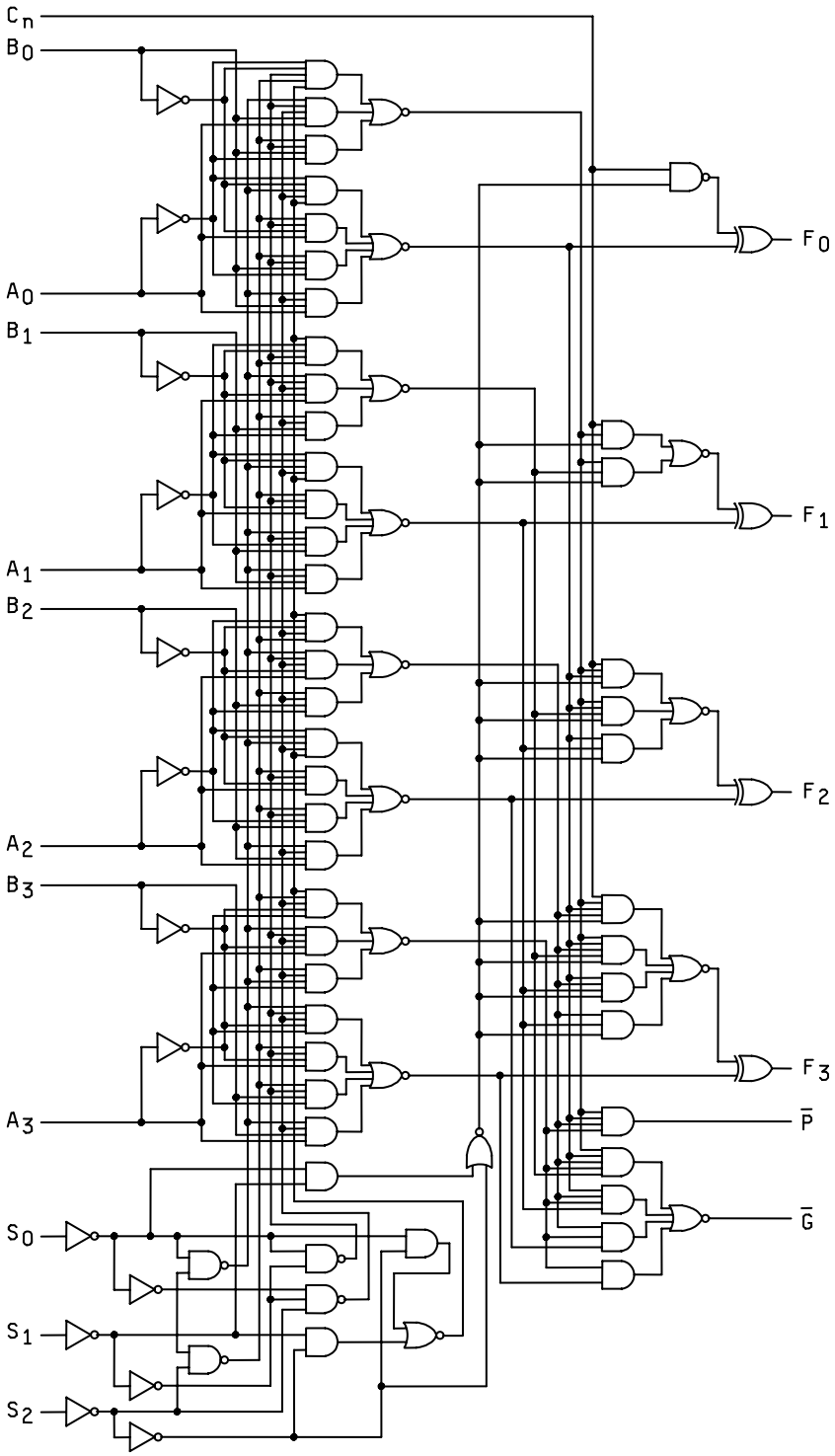


FIGURE 3. Logic diagram.

Device type 02

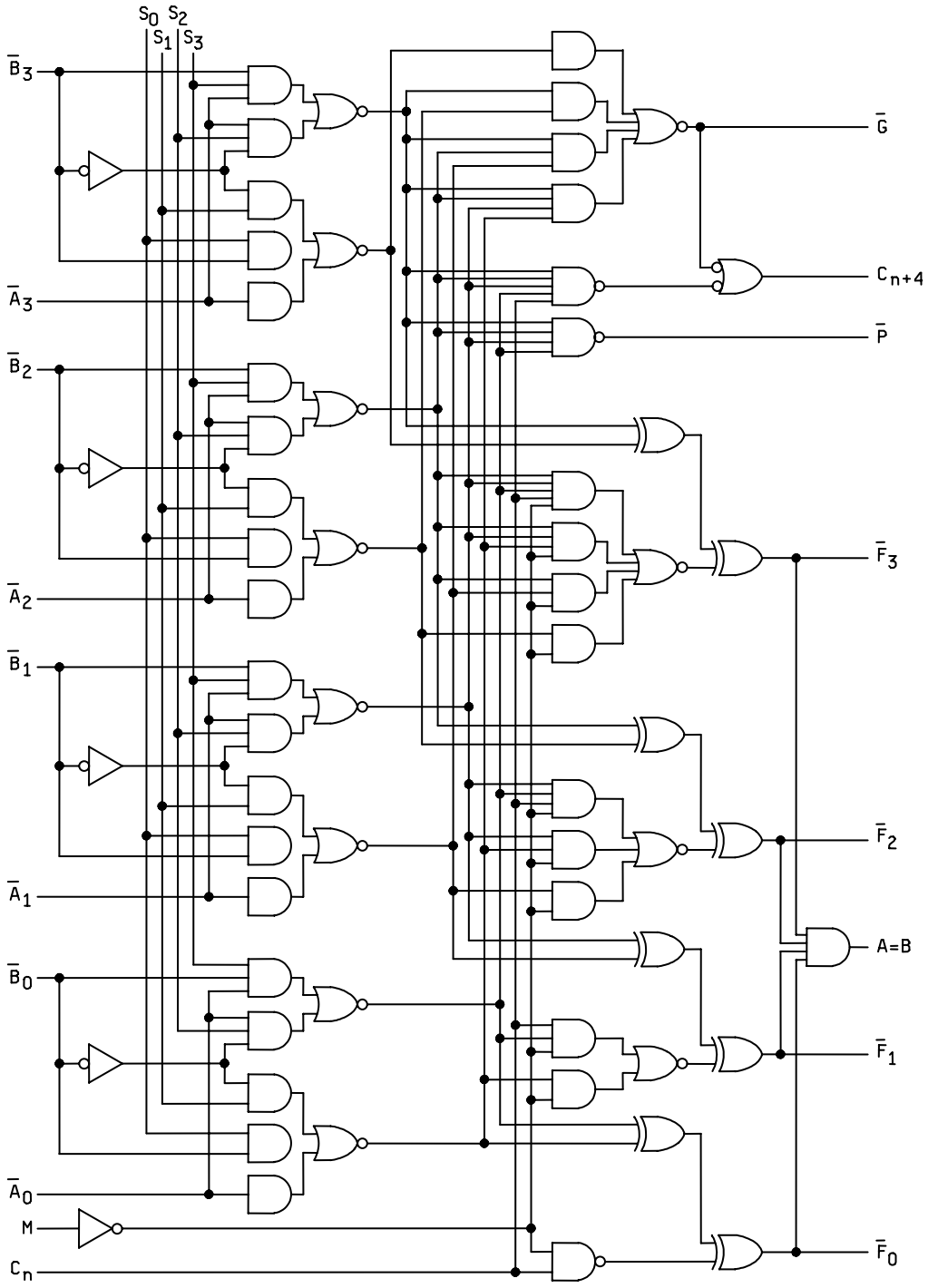
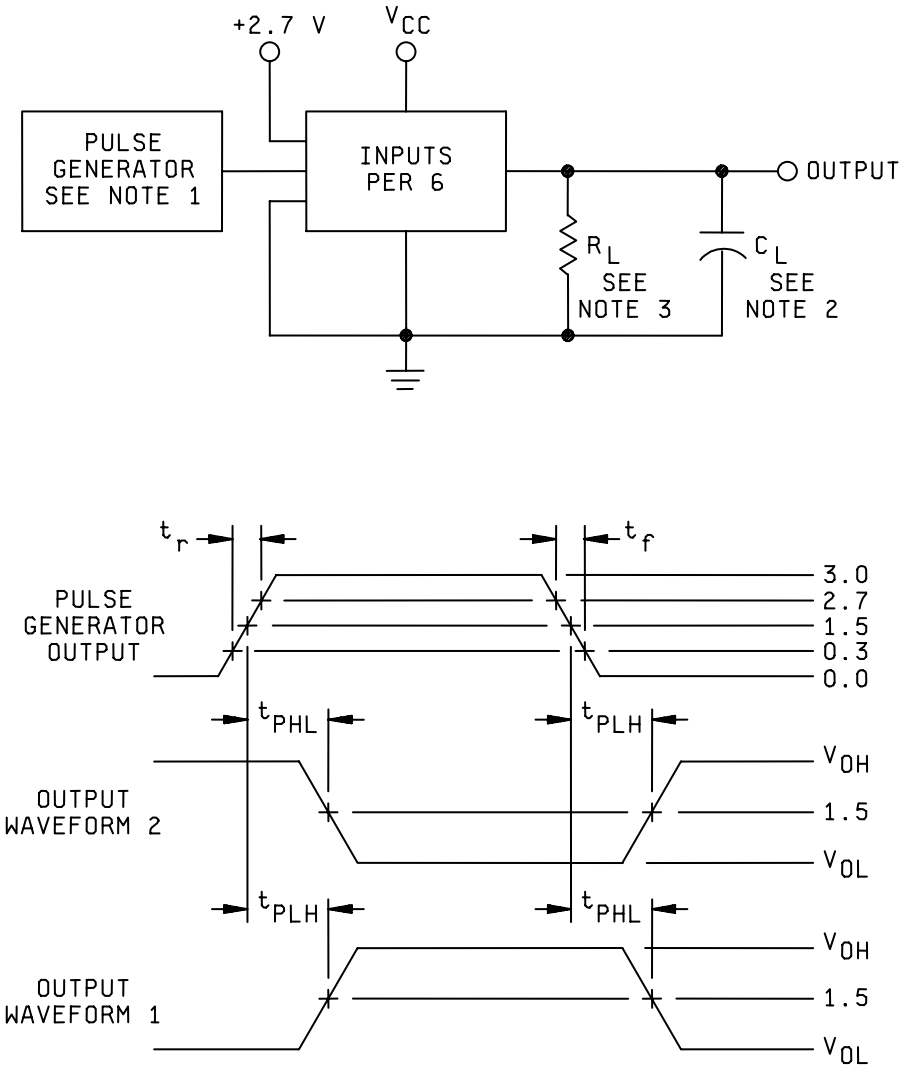


FIGURE 3. Logic diagrams - Continued.

Device type 01 and 02



NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f \leq 1$ MHz, $Z_{OUT} = 50\ \Omega$.
2. C_L includes jig and probe capacitance. $C_L = 50$ pF.
3. $R_L = 500\Omega$.

FIGURE 4. Test circuit and switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-01-05

Approved sources of supply for SMD 5962-86710 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
5962-8671001RA	3/	54F381/BRAJC	M38510/33803BRA
5962-8671001SA	3/	54F381/BSAJC	M38510/33803BSA
5962-86710012A	3/	54F381/B2AJC	M38510/33803B2A
5962-8671002JA	27014	54F181DMQB	---
	0C7V7	54F181DMQB	
5962-86710023A	27014	54F181LMQB	---
	0C7V7	54F181LMQB	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Dr PO Box 58090 Santa Clara, CA 95052-8090
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.