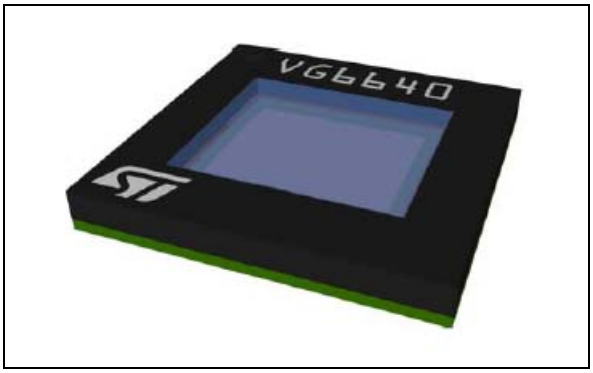
VG6640, VD6640

Automotive 1.3 megapixel high-dynamic range image sensor

Datasheet - production data



Features

- AEC-Q100 qualified
- 1.3 megapixel resolution sensor (1304 x 980) in 1/2.7 inch optical format
- High dynamic range (HDR) pixel architecture, up to 132 dB dynamic range
- Best in class FSI high pixel sensitivity with 3.75 µm pixel size
- 45 frames per second at full resolution, 60 frames per second at 720p resolution
- Small physical size: 9.0 mm x 9.3 mm Im2BGA
- Synchronization for multiple cameras
- Highly configurable HDR image pre-processing
- Motion and Flicker tolerant HDR options including flicker flag to denote affected pixels
- Comprehensive inline pixel defect correction
- Fast+ I^2C control interface
- MIPI CSI-2 (copyright© 2005-2010 MIPI Alliance, Inc. Standard for Camera Serial Interface 2 (CSI-2) version 1.01, limited to 1 Gbps per lane) version 1.01 serial and/or 12-bit parallel video data interface
- Automotive Safety Integrity Level (ASIL) data included as part of each frame
- Operating junction temperature: -40°C to +125°C

Description

This is a high performance, high dynamic range 1.3 megapixel image sensor. Designed for automotive, security and other demanding outdoor applications, the device offers supreme low light performance and numerous safety integrity features.

An embedded Bayer and monochrome data pre-processor integrates a wide range of image enhancement functions, designed to ensure high image quality.

An advanced synchronization facility allows stereo and multi-camera systems to work synchronously, minimizing system latency and motion temporal mismatch artifacts.

Table 1. Device summary

Device	Color filter	Package
VG6640	RGB Bayer	Im2BGA
VD6640	RGB Bayer	None (bare die

This is information on a product in full production. www.st.com

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1 Overview

The VG6640, VD6640 are generically referred to in this document as “the image sensor”.

Table 2. Technical specifications

Feature	Detail
Pixel resolution	1304 x 980 (to allow 1280 x 960 + 8 border surrounding pixels for ISP processing)
Sensor technology	65 nm, CMOS imager process
Pixel size	3.75 µm x 3.75 µm
HDR characteristics	3 integration times with real-time data merging
Shutter	Electrical rolling
Frame rate at full resolution	45 fps
Frame rate at HD video (720p) resolution	60 fps
Parallel interface data rate	66 Mpixel/s (12 bits per pixel)
CSI-2 serial interface data rate	2 x 550 Mbit/s
Frame synchronization	±1 line through an I^2C command or through dedicated signal
Package	Exposed glass BGA 9.0 mm x 9.3 mm
Maximum recommended CRA(1)	25°
Pixel gain	+13 dB (x5)
Analog gain	+12 dB (maximum)
Supply voltages	2.8V analog supply 1.8V digital I/O supply 1.2V digital core supply (may optionally be generated internally from 1.8V)
Power consumption (typical)	400mW @ 30 fps
External clock frequency range	12-50 MHz, AC or DC coupled
Oscillator frequency range	12-27 MHz, quartz crystal
Junction Temperature range (Tj)	-40°C to +125°C functional (-40°C to +105°C for acceptable images)
Temperature sensors	Two factory calibrated temperature sensors provide ±3°C accuracy over the operating temperature range

1. Due to the excellent angular response of the VG6640 pixels the microlens array does not require to be optimised for a specific lens CRA. At the quoted maximum CRA of 25 degrees the relative efficiency of the pixels is still greater than 80%.

Note: Further specifications can be found in Chapter 10: Electro-optical characteristics

1.1 Interfaces

The image sensor is ready to connect to the camera enabled companion device. Image data is output from the image sensor over a 12-bit parallel interface or a dual lane MIPI CSI-2 serial interface. Before transmission, the image data is compressed from 22-bit to 12-bit using a compression algorithm that causes no perceptible losses.

The 12-bit parallel interface is capable of 66 Mpixel/s.

The dual lane MIPI CSI-2 serial data interface is capable of 2 x 550 Mbit/s and is the industry standard for low EMI and excellent EMC.

The control interface is I2C in either Fast (up to 400KHz) or Fast+ (up to 1MHz) modes.

1.2 Power supplies

Power supplies required:

- 2.8 V for the analog blocks
- 1.8 V for the digital I/Os
- 1.2 V for the digital core

The internal digital core operates from 1.2V. This may optionally be supplied from an external regulator or generated internally from the 1.8V supply by a low drop out regulator included in the image sensor.

1.3 Clock and PLL

An input clock is required which can be supplied as an external clock in the range of 12 MHz to 50 MHz or as an external quartz crystal of 12 MHz to 27 MHz.

The image sensor has an embedded phased locked loop (PLL) block to generate all necessary internal clocks. The PLL can be configured to run at a fixed frequency or with a spread spectrum of up to 30 kHz modulation.

1.4 Image enhancement, status and test features

The video processor integrates a wide range of image enhancement functions, designed to ensure high image quality. These include:

- real-time exposure merging for High Dynamic Range (HDR) imaging
- comprehensive set of motion and flicker minimising HDR options
- flicker flag to indicate where flickering has been detected within a frame
- digital per-channel gain stage for white balancing
- external synchronization
- windowing/image cropping
- subsampling
- analog, pixel and digital gain
- dark calibration
- frame crop
- defective pixel correction
- test pattern generation
- statistics generation
- embedded sensor status data (trailer, and header)

1.5 External frame synchronization

The external frame synchronization features two modes which can be exploited to synchronize the frame start in multiple-camera systems.

- Where an external frame synchronization signal is available, it can be applied to a dedicated synchronization ball. The sensor will synchronize its frame start to the edge of the synchronization signal. Further improvement to the synchronization accuracy can be achieved by applying a common clock to all cameras.
- Where a frame synchronization signal is not available (remote cameras), an I^2C register may be set to synchronize the frame start. The sensor will synchronize its frame start to the end of the I^2C transmission of when the sync register is set.

1.6 Safety integrity

A set of self diagnosis features allows the device to support the automotive safety integrity level (ASIL) system requirements:

- ECC (error correction codes) for critical memories
- analog in-line test modes
- digital in-line test readout modes
- dual temperature sensor
- all diagnosis states can be read back from the internal registers and are also embedded in the image status data

1.7 Reference documents

Table 3. Reference documents

Title	Date
MIPI Alliance Specification for D-PHY v1.10.00	7th November 2011
MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) v1.01	9th November 2010
SMIA 1.0 Functional Specification	06/2004
SMIA 1.0 Characterization Specification Rev A	03/2005
SMIA 1.0 Functional Specification ECR0001 ver 1	02/2005
ITU-R BT.601-7	03/2011

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2 Signal, ball assignment, pad, and wafer description

2.1 Signal description

Table 4. Signal description with Im2BGA 100 balls

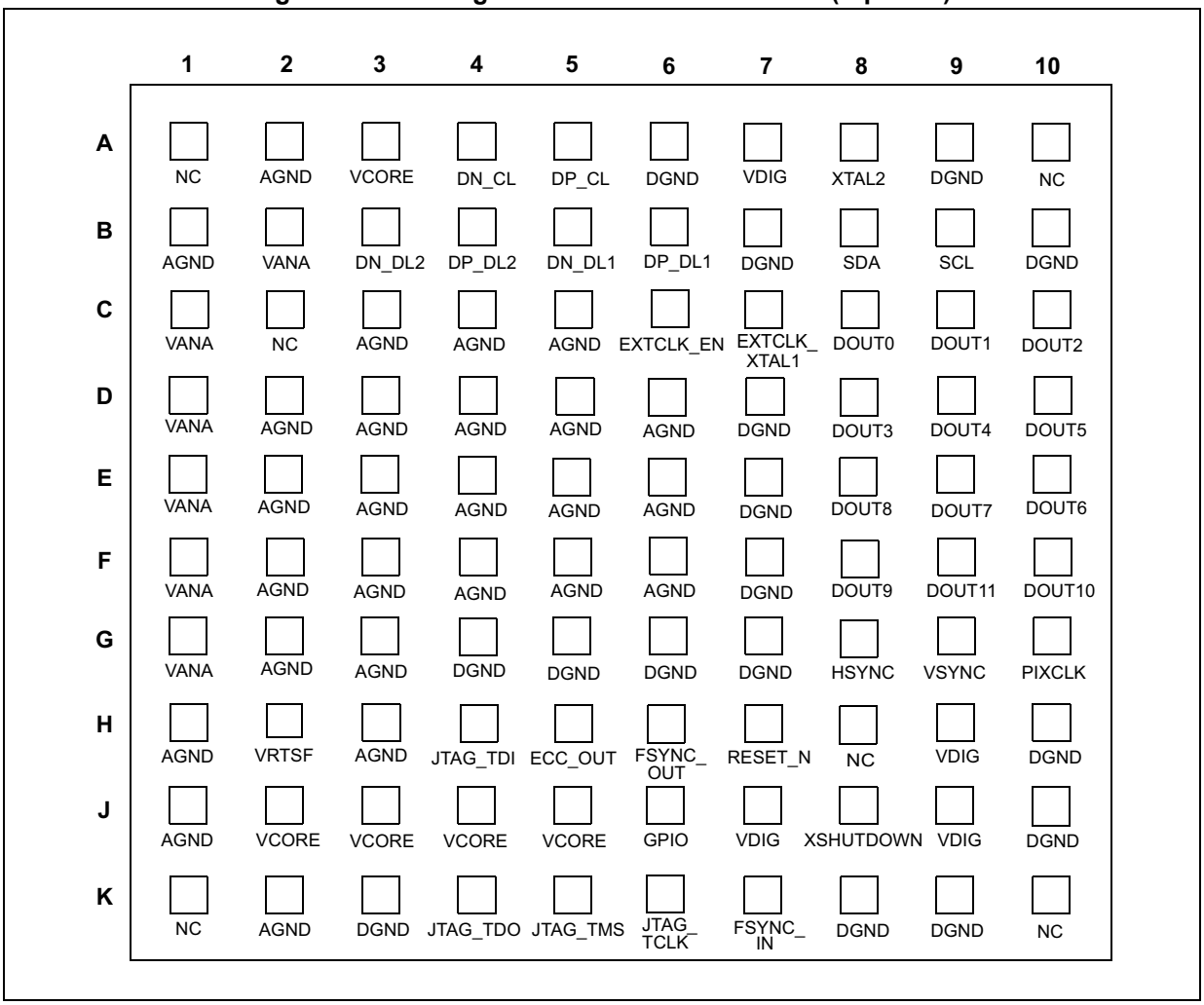
Pin name	Type(1)	Description	Reset state(2)	Reference supply
Power supplies				
VCORE	PWR	1V2 power supply for the digital core (optional, 1V2 may be generated internally using the LDO regulator)		1.2 V
VDIG	PWR	1V8 power supply for the I/O ring (and internal LDO regulator)		1.8 V
VANA	PWR	2V8 power supply for analog blocks		2.8 V
DGND	PWR	Digital ground		1.8 V
AGND	PWR	Analog ground		VANA
Reference				
VRTSF	REF	Internal reference. Must be connected by 220nF capacitor to AGND		N/A
Clocks				
EXTCLK_XTAL1	I-SCH	External clock input, or, crystal oscillator input (dependent on state of EXTCLK_EN pin)		N/A
XTAL2	O	Crystal oscillator output		N/A
CSI2 interface				
DP_DL1, DN_DL1	O	CSI2 data lane 1, positive and negative	HI_Z	VCORE
DP_DL2, DN_DL2	O	CSI2 data lane 2, positive and negative	HI_Z	VCORE
DP_CL, DN_CL	O	CSI2 clock, positive and negative	HI_Z	VCORE
Parallel (ITU) interface				
DOUT[11:0]	O	ITU Data lines	LO	VDIG
PIXCLK	O	ITU Pixel Clock	LO	VDIG
HSYNC	O	ITU Horizontal Sync	LO	VDIG
VSYNC	O	ITU Vertical Sync	LO	VDIG
Control interface				
XSHUTDOWN	I-SCH	Internal 1V2 LDO enable (HI enables the regulator)		VDIG
RESET_N	I-SCH-PU20	Master reset for digital core		VDIG
EXTCLK_EN	I-PD5	External clock enable input	LO	VDIG
SDA	I/O	I2C-style data		VDIG

Table 4. Signal description with Im2BGA 100 balls (continued)

Pin name	Type[1]	Description	Reset state[2]	Reference supply
SCL	I	I2C-style clock		VDIG
FSYNC_IN	I-PD5	Frame synchronization input (rising edge)	LO	VDIG
FSYNC_OUT	O	Frame synchronization output (start of integration on rising edge)	LO	VDIG
ECC_OUT	O	Flags uncorrectable (double bit) ECC occurrences	LO	VDIG
GPIO	I/O	General purpose input or output / Flicker Indication	LO	VDIG
Test interface				
JTAG_TMS	I-PD5	Test mode (connect to GND when not in use)	LO	VDIG
JTAG_TCK	I-PD5	Test clock (connect to VDIG when not in use)	LO	VDIG
JTAG_TDI	I-PD5	Test data in (connect to GND when not in use)	LO	VDIG
JTAG_TDO	O	Test data out	LO	VDIG
Other pins				
NC		Leave unconnected		N/A

1. I = Input, O = Output, I/O = Input or output, I-PD5 -= Input with 5K pull-down, I-SCH = Input with Schmitt trigger, I-Sh-PU20 = Input Schmitt with 20k pull-up, REF = Reference, PWR = Power supply or ground
2. LO = Digital low level, HI = Digital high level, HI_Z = High impedance state

Figure 1. Ball assignment in Im2BGA 100 balls (top view)



1. DNC = do not connect, the ball must be left unconnected
   NC = not connected, the ball is not connected to anything inside the device

Figure 2. IO ring pad layout

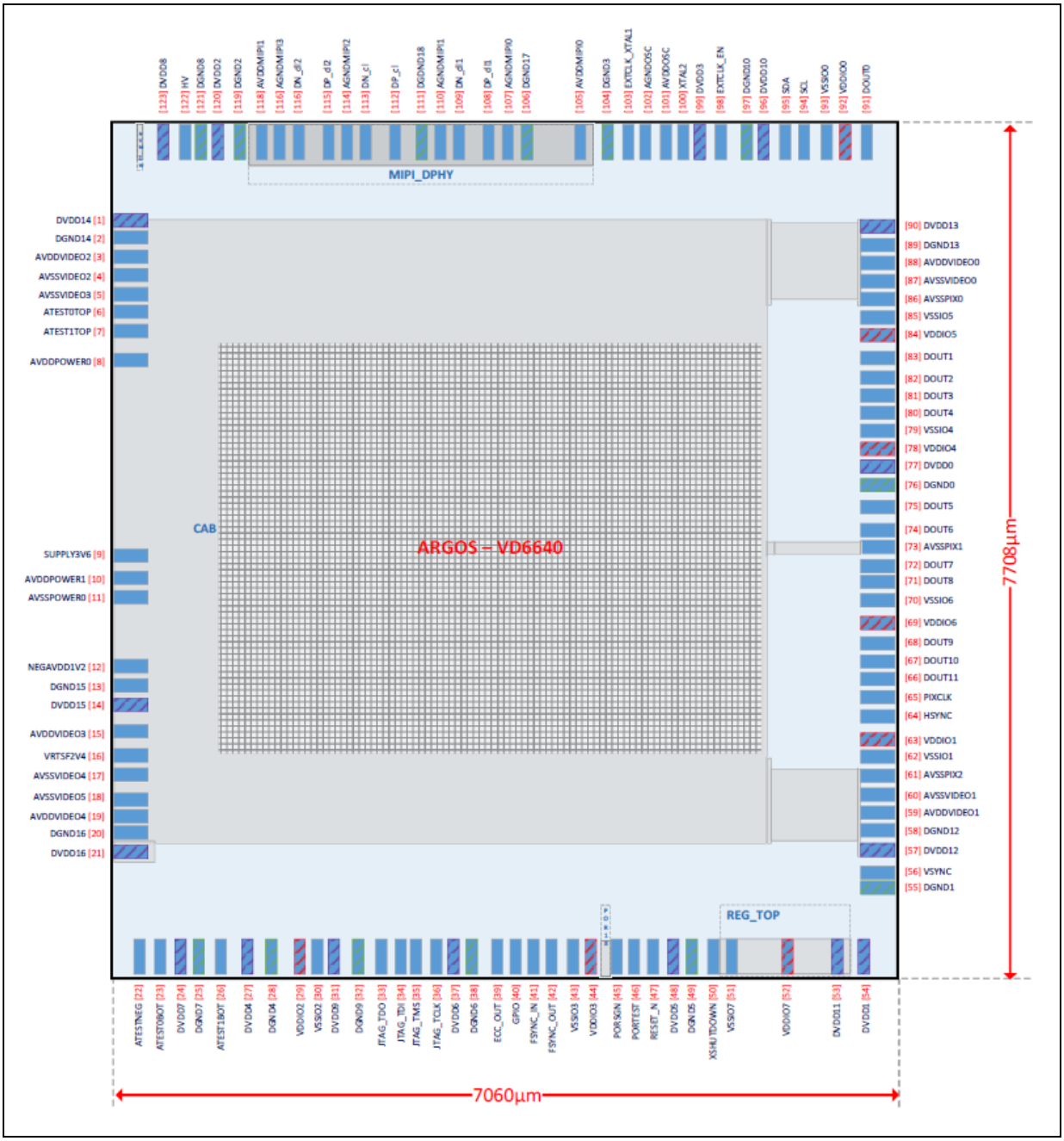
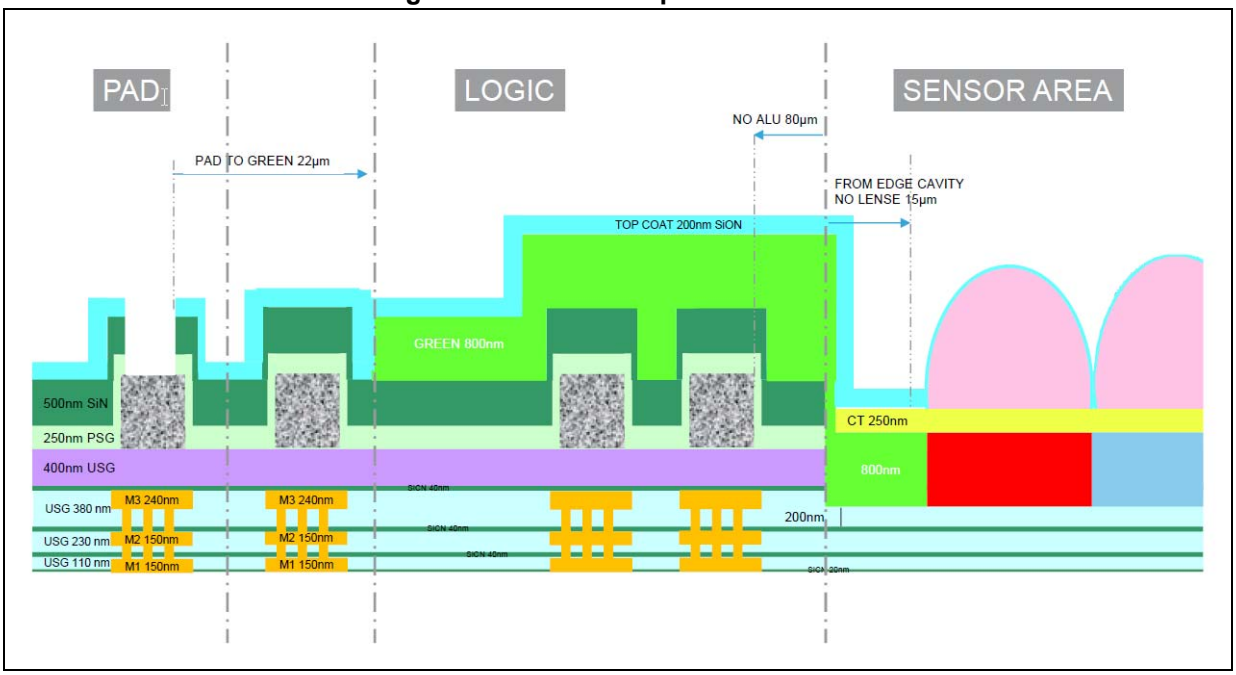
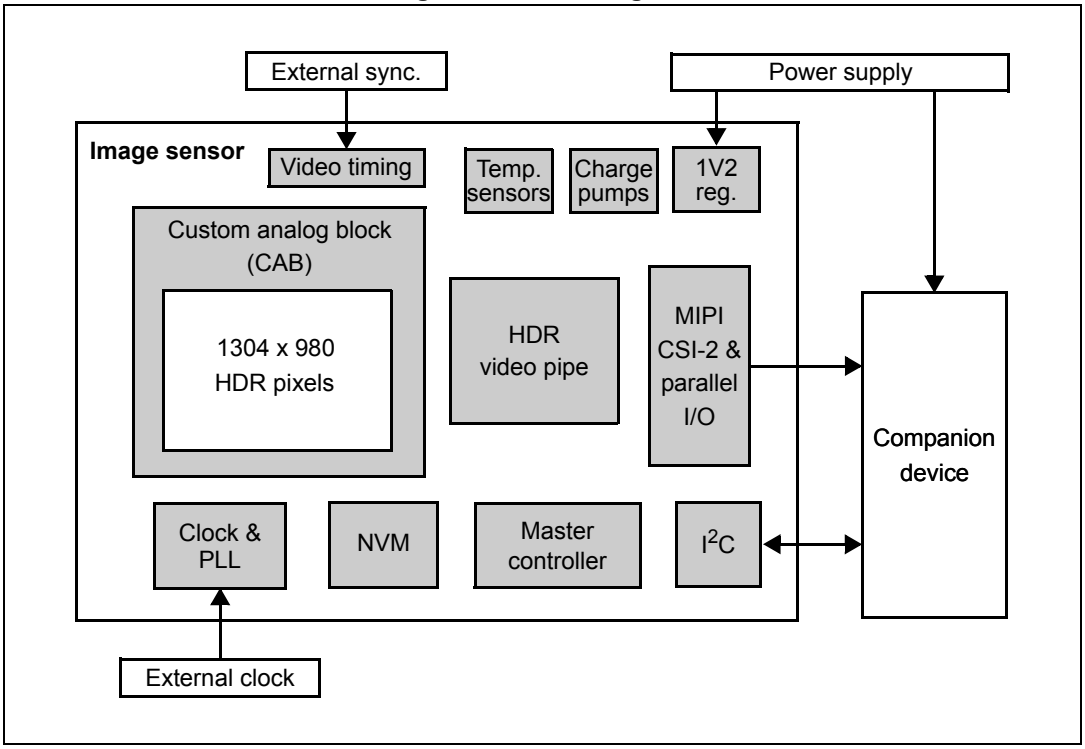


Figure 3. Wafer description and stack



3 Functional description

Figure 4. Block diagram



The image sensor includes the following main functional blocks:

- Master controller

  Responsible for system operation and sequencing with the following features:
  - microcontroller core
  - clock and reset management
  - I^2C control interface and control transaction routing
  - safe system startup from reset to standby
  - system transition from standby to streaming mode
  - system streaming soft stop
  - device re-initialization to default mode (software reset)
  - high dynamic mode setting (management of the integration time settings).
  - non-volatile memory (NVM) management
- Custom analog block (CAB)
  - Contains the pixel array and the analog components to drive it.
- Video timing block
  - Generates digital video timing signals for the CAB with synchronization to an optional external sync signal.

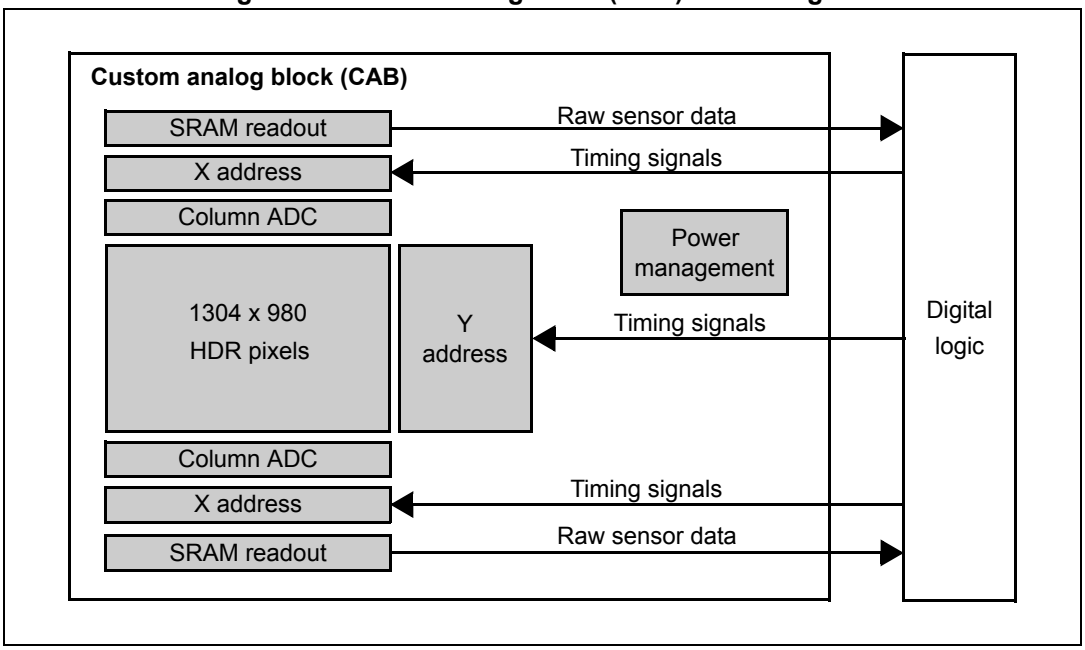
- HDR video pipe
  - Responsible for real-time image data processing at pixel clock rate. Processes the raw pixel data from the ADCs in the CAB. The HDR video pipe contains a set of correction algorithm blocks and dedicated blocks for data coding.
  - Manages the 22bit to12bit compression using a programmable 32 element PWL table.
- Image data transmitters
  - Video data coders and transmitters, including serial (MIPI) and parallel interfaces.
- On chip regulators
  - Supplies the analog block and the digital core.
- Clock and PLL
  - Provides all the clocks required for the video timing.
- Non-volatile memory (NVM)
  - Stores production test data and part-to-part variation data for image quality enhancement.
- Temperature sensors
  - Allows the application to take decisions based on the sensor temperature.

3.1 Analog video block

The custom analog block (CAB) includes the following main functional blocks:

- pixel array, see *Section 3.1.1*
- X, Y address, see *Section 3.1.2*
- dual column ADCs, see *Section 3.1.3*
- dual SRAM, see *Section 3.1.4*
- power management, see *Section 3.1.5*
- multiple exposure HDR pixel, see *Section 3.1.6*

Figure 5. Custom analog block (CAB) block diagram



3.1.1 Pixel array

The pixel array consists of:

- 1304 x 980 visible pixels, each of 3.75 µm x 3.75 µm pixel size
- pixels offer 2 global conversion gain settings with a nominal ratio of
- dark pixels - used to calibrate the dark current
- border pixels - required by the algorithms in the HDR video pipe
- automotive safety integrity level (ASIL) pixels - a synthetic signal source used to generate stimuli for the analog signal chain which can then be verified by the receiver of the image

3.1.2 X, Y address

The X and Y addressing blocks address each pixel in the array in turn, to generate video data. Each pixel integrates the incoming light up to three times, in order to increase the dynamic range.

3.1.3 Dual column ADCs

The dual column ADCs digitize the analog pixel signal from the pixel array. Analog gain may be applied to the analog pixel signal before digitization.

3.1.4 Dual SRAM

The dual SRAM stores the pixel values for two integration times until the pixel values for the third integration time becomes available.

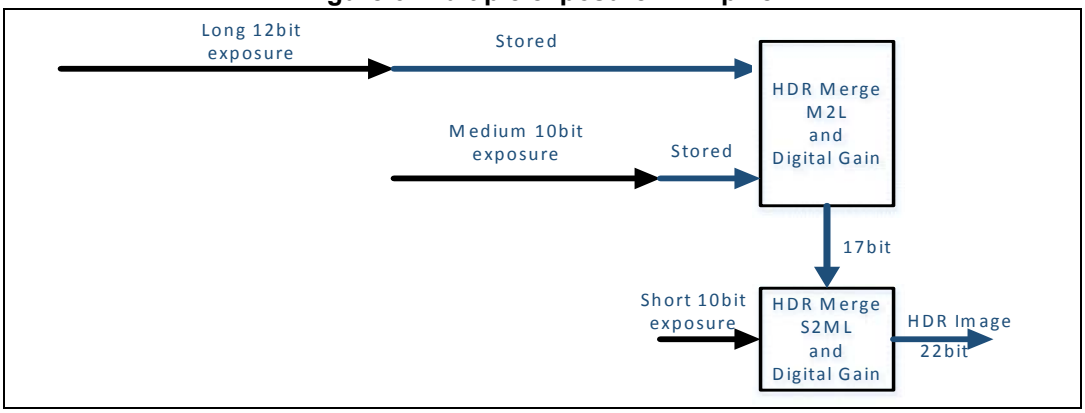
3.1.5 Power management

The power management block provides the necessary supplies to the CAB and improves the power supply rejection ratio (PSRR).

3.1.6 Multiple exposure HDR pixel

The high dynamic range (HDR) image data is constructed by combination of three exposures (integration time) for each pixel. A long exposure captures details in the dark parts of the scene, whilst a short exposure captures details in the bright parts. A mid-length exposure captures all mid-range details.

Figure 6. Multiple exposure HDR pixel



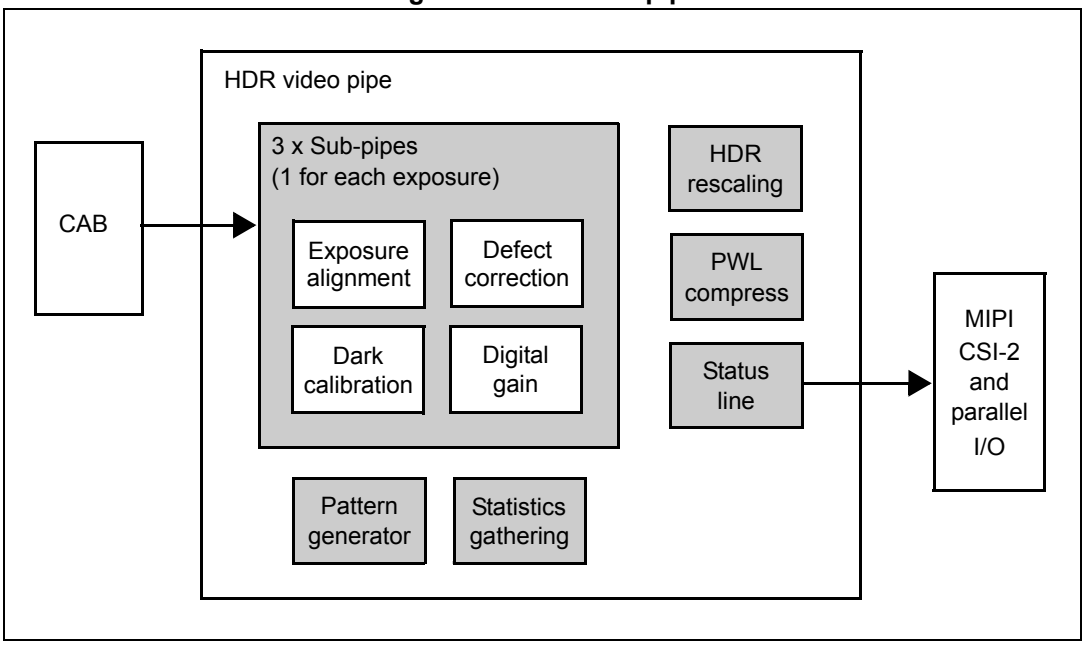
During pixel data collection, the long exposure is made first and stored in SRAM. Then the medium exposure is made Finally, the short exposure is made and once all the data is collected, the three exposures are intelligently merged to create one high dynamic range pixel value.

3.2 Digital video block

The HDR video pipe includes the following main functional blocks:

- three sub-pipes, one for each pixel exposure, see *Section 3.2.1*
- statistics gathering, see *Section 3.2.2*
- pattern generator, see *Section 3.2.3*
- HDR rescaling, see *Section 3.2.4*
- piece-wise linear (PWL) compression, see *Section 3.2.5*
- status line and trailer, see *Section 3.2.6*
- defect correction supporting RAW Bayer and Monochrome color masks.

Figure 7. HDR video pipe



3.2.1 Three sub-pipes for each pixel

Each sub-pipe contains the following blocks, operating on each exposure of the image:

- Dark calibration

  An algorithm that estimates the dark current for each pixel and each pixel exposure. The estimated dark current value is then subtracted from each pixel exposure value in order to accurately render the image.

- Exposure alignment

  Line memories that store the intermediate long and medium exposure time values until the short integration time value of the same pixel is available.

- Defect correction

  An algorithm to correct defective pixels. This can be configured to manage RAW Bayer or monochrome color masks. Single or couplet defective pixels may be removed dynamically. Couplet defective pixels may be mapped out and removed using data from the non-volatile memory (NVM). Up to 32 pixels may be mapped out.

- Digital gain

  In combination with the analog gain, a higher system gain can be achieved. The digital gain can also be used to compensate for the coarse step size of the analog gain, as the digital gain has a much finer step size. This allows further white balance and exposure corrections to be made by the companion device.

3.2.2 Statistics gathering

The statistics gathering block collects and collates pixel values for use by exposure and white balance algorithms. The average pixel value and variance are generated for up to 48 zones (across the full field of view).

Histogram data can be collected over a maximum of four regions of interest (ROIs), and over any or all of the color planes. Each histogram has a resolution of 64 bins, each bin is 16-bits.

3.2.3 Pattern generator

The pattern generator block generates a test pattern that can be used to test the entire HDR video pipe. The following patterns are available:

- color bars (plain and fade to 50%)
- grayscale (horizontal, vertical and diagonal)
- solid colors
- test cursors with programmable positions
- pseudo-random data
- HDR ramp

3.2.4 HDR rescaling

The HDR rescaling algorithm merges the three exposures for each pixel. Exposure correction factors are calculated and applied to compensate for non-linearities. The merge algorithm options ensure that true colors are preserved and flicker and ghost artifacts are minimized.

3.2.5 Piecewise linear (PWL) compression

The PWL block contains a logarithmic type compression algorithm to reduce the data bit-depth transmitted and avoid excessive bandwidth requirements. The PWL compression algorithm is loss-less in the sense that any losses in image quality are below the noise floor of the image. This is implemented using a 32 point curve resulting in an improved SNR performance, reduced quantization noise and a more natural image.

3.2.6 Status and trailer lines

The status and trailer lines include frame-by-frame metadata such as:

- product identification
- configuration status
- image statistics including histograms
- frame counter

The data in the status and data lines is encoded using the SMIA embedded line tagging mechanism. This mechanism allows the data to be decoded in a generic way. For example, data tags allow both the I^2C index and the value of each register included in the status and trailer lines to be decoded.

Refer to *SMIA 1.0 Part 1: Functional Specification, section 4.9 Embedded Data Line Formats* for further details.

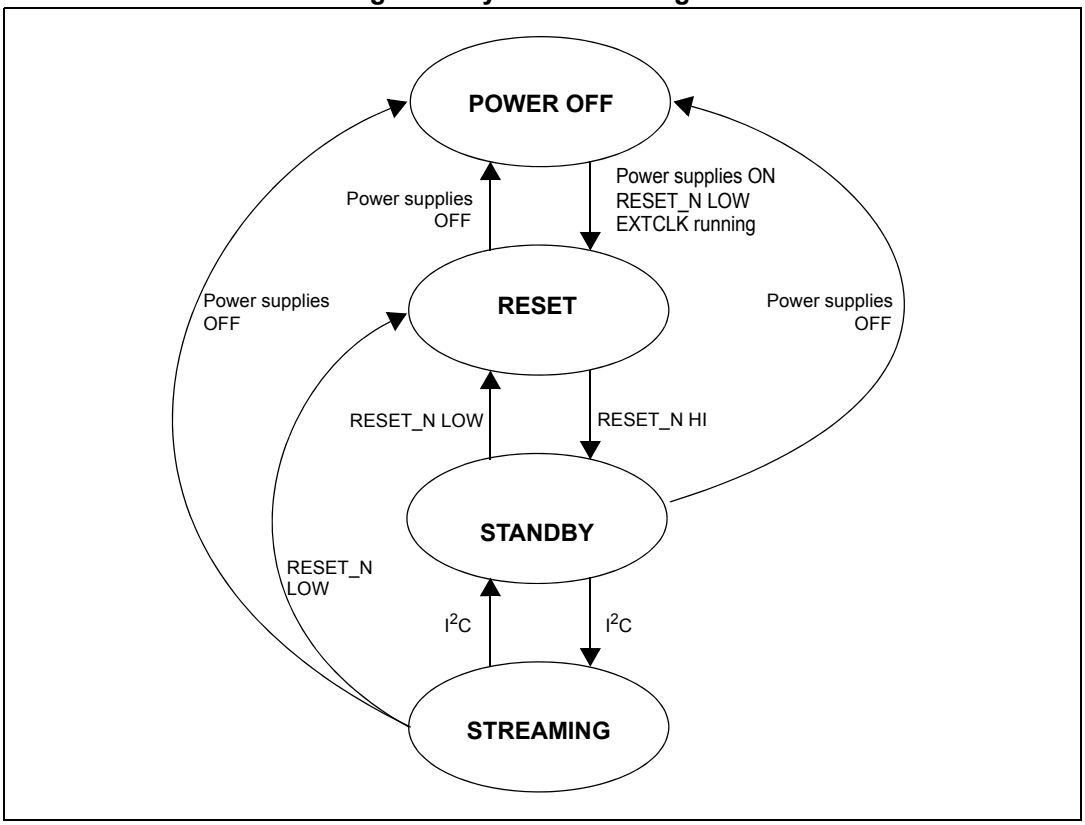
3.2.7 ASIL lines

ASIL data lines follow the trailer data lines in the frame format. They including analog and digital test data that allows comprehensive system monitoring and fault detection.

3.3 Device operating modes

The mode changes in the image sensor are shown in *Figure 8*.

Figure 8. System state diagram



3.3.1 Power off state

Power supplies are off.

3.3.2 Reset state

All blocks are powered and in a state of reset. I^2C communications are not supported in this mode. All registers are returned to their default values. EXTCLK should be provided to the sensor in this mode.

3.3.3 Standby state

Standby state preserves the contents of the register settings. I^2C communications are supported in this mode. The internal video timing is reset to the start of a video frame in preparation for the enabling of active video. The previous settings of exposure and gain are preserved. The system clock must remain active when communicating with the image sensor.

If the MIPI CSI-2 interface is in use then the state of the bus in Standby depends on whether the previous state was Reset or Streaming. If the previous state was Reset then all MIPI CSI2 data lines remain at high impedance. If the previous state was Streaming then the MIPI CSI2 data lines go to LP11 state while in Standby state.

Standby state is entered from reset by setting RESET_N high, or from streaming by writing to the mode_select register; or by commanding a software reset by writing to the software_reset register.

Note: After a software reset or the transition of RESET_N to high, all registers are returned to their default values.

3.3.4 Streaming state

Streaming state allows live video data to be streamed to the output. Streaming mode is entered by writing to the mode_select register.

4 Control interface

Control and status data is transferred to and from the image sensor using the control interface. The internal registers in the image sensor can be configured or read back by a companion device containing an I^2C master (SDA, SCL). Commands are in the format specified by the control interface in the MIPI CSI-2 specification (16-bit index followed by 8-bit data).

The control interface is an I^2C-type interface with two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus uses a unique address and a simple master/slave relationships exists.

Note: Technically, the control interface serial bus is a protocol and subset of the I^2C standard. For brevity, this datasheet will refer to the control interface as I^2C.

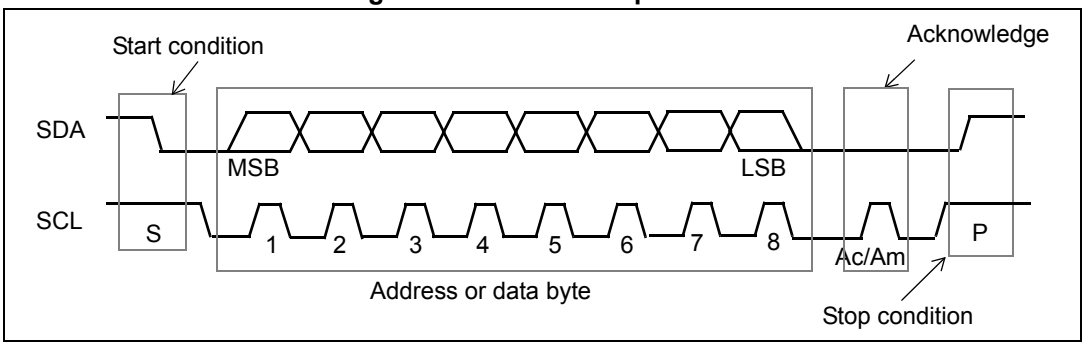
By default the image sensor operates in I^2C Fast mode (up to 400kHz). For operation in Fast+ mode (up to 1MHz), this must be enabled by setting the relevant register.

Note: Operation in Fast+ mode requires a change in value of pull-up resistor to ensure fast enough rise time of the signals (see Section 11.5: I2C pull-up resistors).

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located externally or on the companion device. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high. See*Chapter 9: Electrical characteristics on page 87* for electrical and timing information.

Clock signal (SCL) generation is performed by the master device. The master device initiates data transfer. The I^2C bus on the image sensor uses a default device address of 0x20. This slave address is held in register 0x41A8 as detailed in the register map.

Figure 9. Data transfer protocol

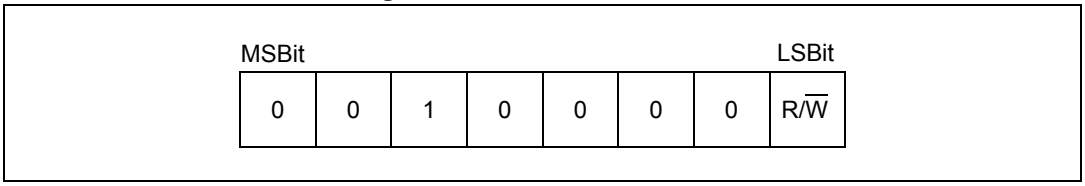


Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for camera acknowledge and Am for master acknowledge. The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x20 by default) and also specifies the data direction. If the least significant bit (lsb) is low (that is, 0x20) the

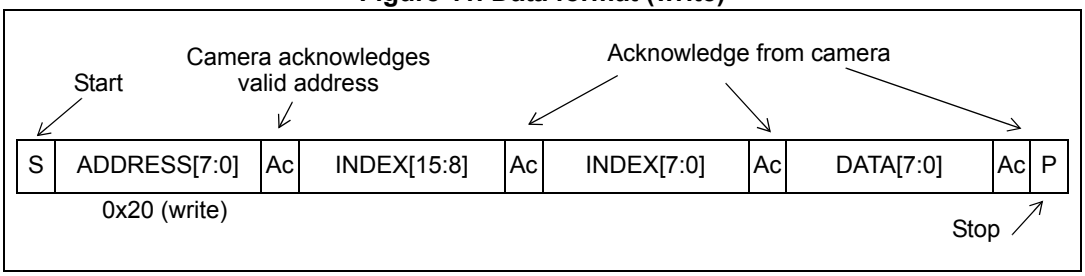
message is a master write to the slave. If the lsb is set (that is, 0x21) then the message is a master read from the slave.

Figure 10. I²C device address



All serial interface communications with the sensor must begin with a start condition. The sensor acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (lsb of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence the second and third bytes received provide a 16-bit index which points to one of the internal 8-bit registers.

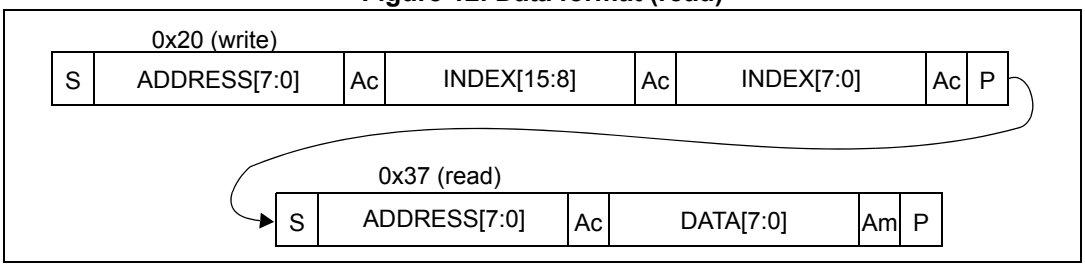
Figure 11. Data format (write)



As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 12. Data format (read)



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the image sensor for a write and the baseband for a read).

A message can only be terminated by the bus master, either by issuing a stop condition or by a negative acknowledge (that is, **not** pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a stop condition. If the auto-increment feature is used the master does **not** have to send address indexes to accompany the data bytes.

Figure 13. Data format (sequential write)

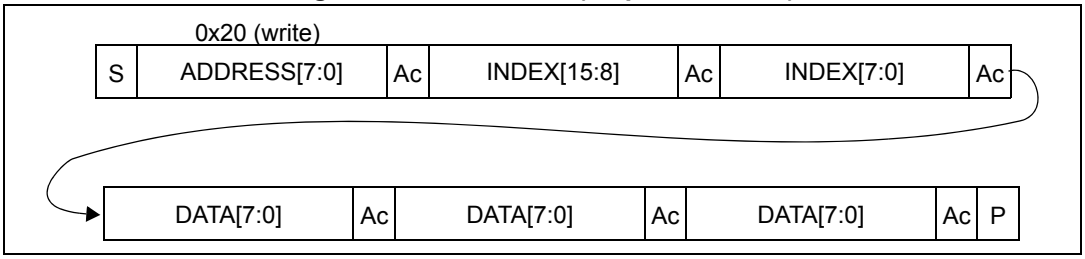
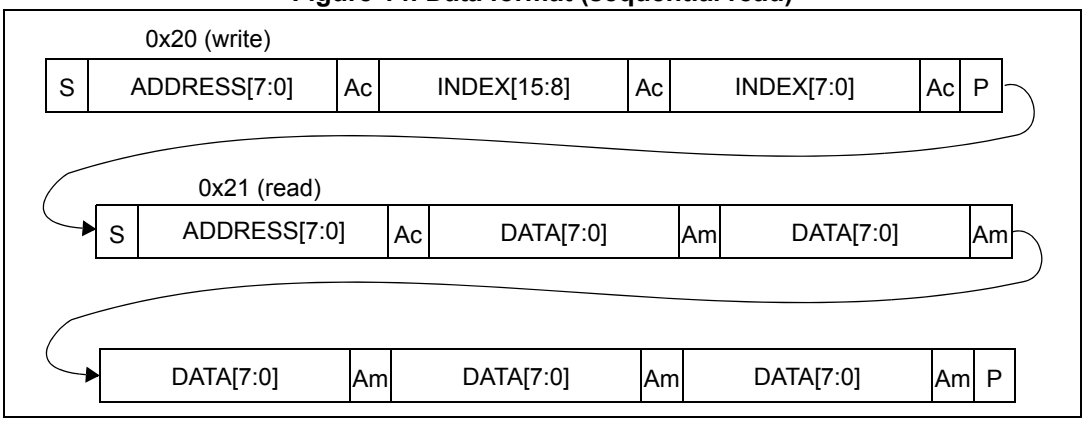


Figure 14. Data format (sequential read)



Further details of the control interface protocol can be found in the *MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2)*.

4.1 Register formats

Any internal register that can be written to, can also be read from. There are also read only registers that contain device status information, for example, design revision details.

A read instruction from an unused register location returns the value 0x00. A read instruction from a reserved address may return any value.

A write instruction to a reserved or unused register location is illegal and the effect of such a write is undefined.

A read or write to an unused register location must not cause the I^2C read or write message to be aborted. Therefore an I^2C read or write message to an unused register location must complete in the same way as if the read or write message had addressed a used register location.

It is the responsibility of the companion device to only write to register locations which have been defined.

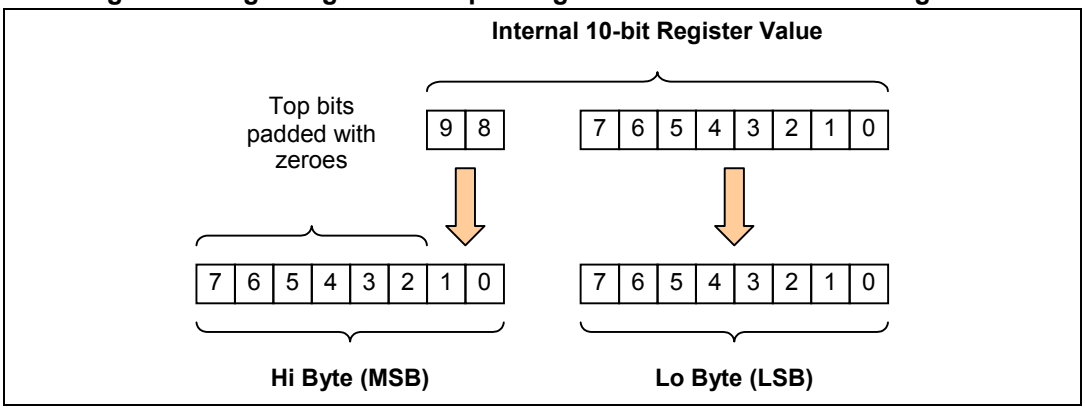
Note that some registers marked as Read Only (RO) or Do Not Write (DNW) can be written to and may read back with the data written but may also have unpredictable effects on the operation of the sensor.

4.1.1 Data alignment within registers

Registers that are larger than 8 bits long are stored most significant byte first, i.e the MSB is placed in the location with the lowest index.

If the width of an internal register is narrower than the 8-bit, 16-bit or 32-bit register which reports it's value, then the register value is right aligned within the register and the unused MS bits are padded with zeroes.

Figure 15. Right alignment for packing 10-bit data into two 8-bit registers



4.1.2 Valid register data types

The contents of the registers can represent a number of different data types (see *Table 5*). The register map uses this coding to help with the interpretation of the contents of each register.

Table 5. Valid register data types

Data type	Name	Range	Description
8UI	8-bit unsigned integer	0 to 255	-
8SI	8-bit signed integer	-128 to 127	Two's complement notation
16UI	16-bit unsigned integer	0 to 65535	-
16SI	16-bit signed integer	-32768 to 32767	Two's complement notation
16UR	16-bit unsigned iReal	0 to 255.99609375	08.08 fixed point number. 8 integer bits (MS Byte), 8 fractional bits (LS Byte)
16SR	16-bit signed iReal	-128 to 127.9960375	Two's complement notation, 8 fractional bits
32UR	32-bit unsigned iReal	0 to 65535.99998474	16.16 fixed point number. 16 integer bits (MS 2 Bytes), 16 fractional bits (LS 2 Bytes)
32SR	32-bit signed iReal	-32768 to 32767.99998474	Two's complement notation,16 fractional bits
32SF	32-bit IEEE floating-point number	As per IEEE 754	As per IEEE 754. 1 sign bit, 8 exponent bits, 23 fractional bits
8C or 16C	8-bit or 16-bit Coded	-	This indicates that the value is decoded to select one of several functions or modes.
8B or 16B	8 or 16 bits	-	Each bit represents a specific function or mode.

4.2 Register map

User should write only to the register addresses defined in this document. Writes to other addresses may cause the VG6640 to operate incorrectly.

4.2.1 Status registers [0x0000 to 0x0013]

Table 6. Status registers [0x0000 to 0x0013]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0000	HI	Sensor_Model_ID	16UI	0x02	DNW	Sensor model identification number.
0x0001	LO			0x80		
0x0002		Revision_Number_Major	8UR	0x20	DNW	Revision identifier of the camera. Default value depends on NVM content. 4.4
0x0006		Pixel_Order	8UI	0x00	DNW	Color pixel readout order. Changes according to mirror and flip (register 0x0101). 0x00 - GR/BG normal. 0x01 - RG/GB horizontal mirror. 0x02 - BG/GR vertical flip. 0x03 - GB/RG vertical flip and horizontal mirror.
0x0008	HI	Data_Pedestal	16UI	0x00	DNW	Data pedestal being applied to the LongX4 data.
0x0009	LO			0x00		
0x0010	HI	Frame_Count	32UI	0xFF	DNW	Increments by 1 every time a frame is streamed. Reports 0xFFFFFFFF when sensor is idle or after a soft reset. Rolls over at 0xFFFFFFFE to 0x00000001.
0x0011				0xFF		
0x0012				0xFF		
0x0013	LO			0xFF		

4.2.2 Frame format description registers [0x0040 to 0x0055]

Table 7. Frame format description registers [0x0040 to 0x0055]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0040		Frame_Format_Model_Type	8UI	0x01	DNW	Generic frame format 0x01 = 2 byte data format 0x02 = 4 byte data format
0x0041		Frame_Format_Model_Subtype	8UI	0x15	DNW	Contains the number of 2-byte data format descriptors used The upper nibble defines the number of column descriptors The lower nibble defines the number of row descriptors
0x0042	HI	Frame_Format_Descriptor_0	16UI	0x55	DNW	X output size [15:12] - Pixel code [11:0] - X size (default 1304)
0x0043	LO			0x18		
0x0044	HI	Frame_Format_Descriptor_1	16UI	0x10	DNW	2 embedded data header lines [15:12] - Pixel code [11:0] - number of data header lines
0x0045	LO			0x02		
0x0046	HI	Frame_Format_Descriptor_2	16UI	0x53	DNW	Y output size [15:12] - Pixel code [11:0] - Y size (default 980)
0x0047	LO			0xD4		
0x0048	HI	Frame_Format_Descriptor_3	16UI	0x80	DNW	2 digital ASIL lines [15:12] - Pixel code [11:0] - number of ASIL lines
0x0049	LO			0x02		
0x004A	HI	Frame_Format_Descriptor_4	16UI	0x90	DNW	2 analog ASIL lines [15:12] - Pixel code [11:0] - number of ASIL lines
0x004B	LO			0x02		
0x004C	HI	Frame_Format_Descriptor_5	16UI	0xA0	DNW	6 embedded data trailer lines [15:12] - Pixel code [11:0] - number of data lines
0x004D	LO			0x06		
0x004E	HI	Frame_Format_Descriptor_6	16UI	0x00	DNW	unused descriptor
0x004F	LO			0x00		
0x0050	HI	Frame_Format_Descriptor_7	16UI	0x00	DNW	unused descriptor
0x0051	LO			0x00		
0x0052	HI	Frame_Format_Descriptor_8	16UI	0x00	DNW	unused descriptor
0x0053	LO			0x00		
0x0054	HI	Frame_Format_Descriptor_9	16UI	0x00	DNW	unused descriptor
0x0055	LO			0x00		

4.2.3 Setup registers [0x0100 to 0x0114]

Table 8. Setup registers [0x0100 to 0x0114]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0100		Mode_Select	8UI	0x00	RW	[7] - External sync mode: 0x0 - Master mode 0x1 - Slave mode [6] - Slave mode type: 0x0 - External pin slave mode 0x1 - I2C command slave mode [0] - Mode select: 0x00 = Standby 0x01 = Streaming
0x0101		Image_Orientation	8UI	0x00	RW	[7:2] - Reserved [1:0] - Image orientation: 0x0 = Normal 0x1 = Flip in X 0x2 = Flip in Y 0x3 = Flip in X and flip in Y
0x0103		Software_Reset	8UI	0x00	RW	Software reset returns the sensor to its power-on defaults 0x00 = Normal operation 0x01 = Software reset enabled The value of this register is automatically reset to 0x00
0x0104		Grouped_Parameter_Hold	8UI	0x00	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0x00 = Consume values as normal 0x01 = Do not consume values
0x0111		Signalling_Mode	8UI	0x02	RW	Determines which transmission signalling mode is to be used 0x02 = CSI2 output only 0x80 = Parallel/ITU output only 0x82 = CSI2 and parallel/ITU output together

Table 8. Setup registers [0x0100 to 0x0114] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0112	HI	Data_Format	16UI	0x16	RW	The value of this register contains the bit-depth of the uncompressed pixel data. The only valid value is 0x16 (22-bit).
0x0113	LO			0x0C		The value of this register contains the bit-depth of the compressed pixel data. The only valid value is 0x0C (12-bit).
0x0114		CSI_Lane_Mode	8UI	0x01	RW	The number of CSI2 data lanes in use. 0x00 = 1-lane. 0x01 = 2-lane.

4.2.4 Integration and gain status registers [0x0200 to 0x0229]

Table 9. Integration and gain status registers [0x0200 to 0x0229]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0200	HI	Fine_Integration_Time_ Long_Status	16UI	0x00	DNW	Not used in VG6640. Always reads back as zero.
0x0201	LO			0x00		
0x0202	HI	Coarse_Integration_Time_ Long_Status	16UI	0x00	DNW	Coarse integration time for the long exposure in lines.
0x0203	LO			0x00		
0x0204	HI	Analog_Gain_Status	16UI	0x00	DNW	Global analog gain (coded) 0x0000 = Gain x1.0 (+0dB) 0x0001 = Gain x1.07 (+0.6dB) 0x0002 = Gain x1.1 (+1.2dB) 0x0003 = Gain x1.2 (+1.8dB) 0x0004 = Gain x1.3 (+2.5dB) 0x0005 = Gain x1.5 (+3.3dB) 0x0006 = Gain x1.6 (+4.1dB) 0x0007 = Gain x1.8 (+5.0dB) 0x0008 = Gain x2.0 (+6.0dB) 0x0009 = Gain x2.3 (+7.2dB) 0x000A = Gain x2.7 (+8.5dB) 0x000B = Gain x3.2 (+10.1dB) 0x000C = Gain x4.0 (+12.0dB) 0x000D = Gain x5.3 (+14.5dB) 0x000E = Gain x8.0 (+18.0dB) 0x000F = Gain x16.0 (+24.0dB)
0x0205	LO			0x00		
0x0208	HI	Long2Medium_Line_Offset	16UI	0x00	RW	Exposure time offset between the long and medium pipes in lines.
0x0209	LO			0x62		
0x020A	HI	Medium2Short_Line_Offset	16UI	0x00	RW	Exposure time offset between the medium and short pipes in lines.
0x020B	LO			0x0F		
0x020E	HI	Digital_Gain_GreenR _Status	16UR	0x01	DNW	Green (red row) channel digital gain value
0x020F	LO			0x00		
0x0210	HI	Digital_Gain_Red_Status	16UR	0x01	DNW	Red channel digital gain value
0x0211	LO			0x00		
0x0212	HI	Digital_Gain_Blue_Status	16UR	0x01	DNW	Blue channel digital gain value
0x0213	LO			0x00		
0x0214	HI	Digital_Gain_GreenB _Status	16UR	0x01	DNW	Green (blue row) channel digital gain value.
0x0215	LO			0x00		
0x0216	HI	Coarse_Integration_Time _Medium_Status	16UI	0x00	DNW	Coarse integration time for the medium pipe in lines. Min = 0 lines Max = 96 lines
0x0217	LO			0x00		

Table 9. Integration and gain status registers [0x0200 to 0x0229] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0218	HI	Coarse_Integration_Time _Short_Status	16UI	0x00	DNW	Coarse integration time for the short pipe in lines. Min = 0 lines Max = 13 lines
0x0219	LO			0x00		
0x021B		PixelGain_Status	8UI	0x01	DNW	Pixel gain 0x01 = High gain 0x04 = Low gain
0x021C		Gop_Counter_Max	8UI	0x00	R/W	The max value that the GOP counter is allowed to count up to This register is consumed at the start of stream
0x021D		Gop_Counter_Status	8UI	0x00	DNW	Status of GOP counter
0x0226	HI	TokenId_Status	16UI	0x00	DNW	Token ID
0x0227	LO			0x00		
0x0228	HI	NextTokenId_Status	16UI	0x00	DNW	Next token ID
0x0229	LO			0x00		

4.2.5 Video timing registers [0x0300 to 0x0387]

Table 10. Video timing registers [0x0300 to 0x0387]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0300	HI	VT_Pix_Clk_Div	16UI	0x00	RW	Video timing pixel clock divider. Min = 1 Max = 8
0x0301	LO			0x06		
0x0302	HI	VT_Sys_Clk_Div	16UI	0x00	RW	Video timing system clock divider. Min = 1 Max = 8
0x0303	LO			0x01		
0x0304	HI	Pre_PLL_Clk_Div	16UI	0x00	RW	Pre PLL clock divider value. Valid values = 1, 2, 4, 8
0x0305	LO			0x02		
0x0306	HI	PLL_Multiplier	16UI	0x00	RW	PLL multiplier value. Min = 37 Max = 167
0x0307	LO			0x84		
0x0308	HI	Op_Pix_Clk_Div	16UI	0x00	RW	Output timing pixel clock divider. Valid value = 8
0x0309	LO			0x08		
0x030A	HI	Op_Sys_Clk_Div	16UI	0x00	RW	Output timing pixel clock divider. Min = 1 Max = 4
0x030B	LO			0x01		
0x0310	HI	ExtClk_Frequency_MHz	16UR	0x0C	RW	External clock frequency. This register must be set to the value of the clock applied to the EXTCLK_XTAL1 pin.
0x0311	LO			0x00		
0x0340	HI	Frame_Length_Lines _Status	16UI	0x03	DNW	Length of the video frame in lines Min = 159 Max = 65536.
0x0341	LO			0xFC		
0x0342	HI	Line_Length_PCK	16UI	0x05	RW	Length of a line of video in pixels. Min = 1438 (21.8uS @ 66MHz Pixel Clock) Max = 65536
0x0343	LO			0x9E		
0x0344	HI	X_Addr_Start	16UI	0x00	RW	X pixel address of the top left corner of the visible pixel data. Min = 0 Max = 1303
0x0345	LO			0x00		
0x0346	HI	Y_Addr_Start	16UI	0x00	RW	Y line address of the top left corner of the visible pixel data. Min = 0 Max = 979
0x0347	LO			0x00		
0x0348	HI	X_Addr_End	16UI	0x05	RW	X pixel address of the bottom right corner of the visible pixel data. Min = 0 Max = 1303
0x0349	LO			0x17		

Table 10. Video timing registers [0x0300 to 0x0387] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x034A	HI	Y_Addr_End	16UI	0x03	RW	Y line address of bottom right corner of the visible pixel data. Min = 0 Max = 979
0x034B	LO			0xD3		
0x034C	HI	X_Output_Size	16UI	0x05	RW	Width in pixels of the output image from the sensor. Min = 128 Max = 1304
0x034D	LO			0x18		
0x034E	HI	Y_Output_Size	16UI	0x03	RW	Height in lines of the output image from the sensor. Min = 128 Max = 980
0x034F	LO			0xD4		
0x0381		X_Even_Inc	8UI	0x01	RW	X address increment for even pixels. Min = 1 Max = 15
0x0383		X_Odd_Inc	8UI	0x01	RW	X address increment for odd pixels. Min = 1 Max = 15
0x0385		Y_Even_Inc	8UI	0x01	RW	Y address increment for even lines. Min = 1 Max = 15 NOTE - only odd values supported
0x0387		Y_Odd_Inc	8UI	0x01	RW	Y address increment for odd lines. Min = 1 Max = 15 NOTE - only odd values supported

4.2.6 System flag registers [0x211D to 0x2121]

Table 11. System flag registers [0x211D to 0x2121]

Index	Byte	Register name	Data type	Default	Type	Comment
0x211D		SystemFsm	8UI	0x02	DNW	Indicates the state of the state machine: 0x00 = SENSOR_HWRESET 0x01 = SENSOR_BOOT 0x02 = SENSOR_IDLE, sensor ready and waiting for command. 0x03 = SENSOR_STREAM _STARTUP 0x04 = SENSOR_STREAM, sensor is streaming images 0x05 = SENSOR_STOP _STREAMING, received stop command
0x211E		FirmwareRevision	8UI	0x20	DNW	Firmware revision
0x211F		VTimingRevision	8UI	0x30	DNW	Video timing revision

Table 11. System flag registers [0x211D to 0x2121] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2120		FwPatchRevision	8UI	0x00	DNW	Firmware patch revision
0x2121		SystemSetup	8UI	0x00	RW	[7:5] - FlashMapMode: Flicker Repair scheme and FlashMap output selection. 000: Disable 001: Long and Medium only bit on GPIO (sync-ed with ITU) 011: Long Medium and Short bit on GPIO (sync-ed with ITU) 101: Long and Medium only bit on data LSB (CSI2 and/or ITU) 111: Long Medium and Short bit on data LSB (CSI2 and/or ITU) [4] - bTempSensorsSwStbyEnable. Enable the temp sensors for a single measurement when in Standby mode 0: Disable 1: Enable (autoclear bit) [3] - bMonochromeEnable: Set dynamic defect correction in monochrome mode. 0: Disable 1: Enable [2] - bI2cFastModePlusEnable 0x0 = I2C Fast Mode compatible 0x1 = I2C Fast Mode+ compatible [1] - bUISetSelect: Selects between UISet0 and UISet1 when pingpong mode is not active. 0: UISet0 selected 1: UISet1 selected [0] - bPingPongMode 0x0 = UISet chosen by bit [1] 0x1 = Toggles between UISet_0 and UISet_1

4.2.7 User interface set 0 registers [0x2124 to 0x2286]

Two user interface register sets are provided to allow frame-by-frame context switching of exposure, frame length, HDR merge, defect correction, PWL compression parameters and statistics accumulation. While one frame is being streamed using the active context settings, new settings may be programmed to the non-active context, ready for use by the next frame.

These settings must be written with the grouped_parameter_hold flag set. The status of the integration and gain registers is reported in the frame status line.

Table 12. User interface set 0 Video timing registers [0x2124 to 0x2132]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2124		TokenId	8UI	0x01	RW	Token ID used for identification of this UI Set
0x2125	HI	CoarseTimeLong	16UI	0x03	RW	Coarse integration time for long pipe (lines) Min = 0 lines Max = framelength_lines - 115
0x2126	LO			0x5D		
0x2127	HI	CoarseTimeMedium	16UI	0x00	RW	Coarse integration time for medium pipe (lines) Min = 0 lines Max = 96
0x2128	LO			0x35		
0x2129	HI	CourseTimeShort	16UI	0x00	RW	Coarse integration time for short pipe (lines) Min = 0 lines Max = 13
0x212A	LO			0x03		
0x212B		AnalogGain	8C	0x00	RW	Global analog gain (coded) 0x00 = Gain x1.0 (+0dB) 0x01 = Gain x1.07 (+0.6dB) 0x02 = Gain x1.1 (+1.2dB) 0x03 = Gain x1.2 (+1.8dB) 0x04 = Gain x1.3 (+2.5dB) 0x05 = Gain x1.5 (+3.3dB) 0x06 = Gain x1.6 (+4.1dB) 0x07 = Gain x1.8 (+5.0dB) 0x08 = Gain x2.0 (+6.0dB) 0x09 = Gain x2.3 (+7.2dB) 0x0A = Gain x2.7 (+8.5dB) 0x0B = Gain x3.2 (+10.1dB) 0x0C = Gain x4.0 (+12.0dB) 0x0D = Gain x5.3 (+14.5dB) 0x0E = Gain x8.0 (+18.0dB) 0x0F = Gain x16.0 (+24.0dB)

Table 12. User interface set 0 Video timing registers [0x2124 to 0x2132] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x212C		PixelGain	8UI	0x01	RW	[2:0] - Pixel gain: 0x01 = High gain 0x04 = Low gain [7] - GopReset
0x212D	HI	FrameLengthLines	16UI	0x03	RW	Frame length (lines) Min = 159 Max = 65536
0x212E	LO			0xFC		
0x212F	HI	DarkOffsetMed	16UI	0x00	RW	
0x2130	LO			0x00		
0x2131	HI	DarkOffsetShort	16UI	0x00	RW	
0x2132	LO			0x00		

Table 13. User interface set 0 HDR merge registers [0x2133 to 0x2176]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2133	HI	WB_DGain_GreenInRed	16UR	0x01	RW	Green (Red row) channel digital gain value
0x2134	LO			0x00		
0x2135	HI	WB_DGain_Red	16UR	0x01	RW	Red channel digital gain value
0x2136	LO			0x00		
0x2137	HI	WB_DGain_Blue	16UR	0x01	RW	Blue channel digital gain value
0x2138	LO			0x00		
0x2139	HI	WB_DGain_GreenInBlue	16UR	0x01	RW	Green (Blue row) channel digital gain value
0x213A	LO			0x00		
0x213D	HI	HDR_DGain	16UR	0x01	RW	Post HDR digital gain applied on all color channels
0x213E	LO			0x00		
0x213F	HI	HDRLM_Startmerge	16UI	0x03	RW	Long Medium start merge threshold
0x2140	LO			0xFF		
0x2141	HI	HDRLM_Endmerge	16UI	0x0F	RW	Long Medium end merge threshold
0x2142	LO			0x2F		
0x2143	HI	HDRLM_Knee1	16UI	0x07	RW	Knee1 parameter Below this value is normalized low exposure data
0x2144	LO			0xFE		

Table 13. User interface set 0 HDR merge registers [0x2133 to 0x2176] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2145	HI	HDRLM_Knee2	16UI	0x0E	RW	Knee2 parameter Above this value is normalized high exposure data NOTE - One of the following conditions must be true: Knee1 == Knee2, or, (Knee2 - Knee1) > 7
0x2146	LO			0x63		
0x2147	HI	HDRLM_GainMedium	16UR	0x7F	RW	Normalization gain for low exposure data
0x2148	LO			0xFF		
0x2149	HI	HDRLM_GainLong	16UR	0x07	RW	Normalization gain for high exposure data
0x214A	LO			0xED		
0x214B	HI	HDRLM_FlashThres1	32UR	0x00	RW	Flash threshold value 1
0x214C				0x00		
0x214D				0x0C		
0x214E	LO			0xCD		
0x214F	HI	HDRLM_FlashThres2	32UR	0x00	RW	Flash threshold value 2
0x2150				0x00		
0x2151				0x0C		
0x2152	LO			0xCD		
0x2153	HI	HDRLM_FlashGain	16IR	0x7F	RW	Normalization gain for flash control
0x2154	LO			0xFF		
0x2155	HI	HDRLM_SigmaGhost Thresh1	16UI	0xFF	RW	Ghost free sigma threshold 1
0x2156	LO			0x00		
0x2157	HI	HDRLM_SigmaGhost Thresh2	16UI	0xFF	RW	Ghost free sigma threshold 2 NOTE - the following condition must be maintained GhostThresh2 - GhostThresh1 > 127
0x2158	LO			0xFF		
0x2159	HI	HDRLMS_Startmerge	32UR	0x00	RW	Start merge threshold Below this only linearization data
0x215A				0x00		
0x215B				0x7F		
0x215C	LO			0xE0		
0x214D	HI	HDRLMS_Endmerge	32UR	0x00	RW	End merge threshold Above this only linearization data
0x215E				0x01		
0x215F				0xE5		
0x2160	LO			0xED		

Table 13. User interface set 0 HDR merge registers [0x2133 to 0x2176] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2161	HI	HDRLMS_Knee1	32UR	0x00	RW	Knee point 1 Below this normalized low exposure data
0x2162				0x01		
0x2163				0x00		
0x2164	LO			0x00		
0x2165	HI	HDRLMS_Knee2	32UR	0x00	RW	Knee point 2 Above this normalized high exposure data NOTE - One of the following conditions must be true: Knee1 == Knee2, or, (Knee2 - Knee1) > 7
0x2166				0x01		
0x2167				0xCC		
0x2168	LO			0x5A		
0x2169	HI	HDRLMS_GainShort	16IR	0x7F	RW	Normalization gain for low exposure data
0x216A	LO			0xFF		
0x216B	HI	HDRLMS_GainLongMed	16IR	0x08	RW	Normalization gain for high exposure data
0x216C	LO			0x13		
0x216D	HI	HDRLMS_FlashThres1	32UI	0x00	RW	Flash threshold value 1 (when Flash mode is enabled)
0x216E				0x01		
0x216F				0x99		
0x2170	LO			0x9A		
0x2171	HI	HDRLMS_FlashThres2	32UI	0x00	RW	Flash threshold value 2 (when Flash mode is enabled)
0x2172				0x01		
0x2173				0x99		
0x2174	LO			0x9A		
0x2175	HI	HDRLMS_FlashGain	16IR	0x7F	RW	Normalization gain for flash control
0x2176	LO			0xFF		

Table 14. User interface set 0 defect correction registers [0x2177 to 0x217C]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2177		Long_SingletDefCor Weight	8UI	0x00	RW	Single defect correction in long pipe
0x2178		Long_Couplet_DefCor Weight	8UI	0x00	RW	Couplet defect correction in long pipe
0x2179		Medium_SingletDefCor Weight	8UI	0x00	RW	Single defect correction in medium pipe
0x217A		Medium_CoupletDefCor Weight	8UI	0x00	RW	Couplet defect correction in medium pipe

Table 14. User interface set 0 defect correction registers [0x2177 to 0x217C] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x217B		Short_SingletDefCor Weight	8UI	0x00	RW	Single defect correction in short pipe
0x217C		Short_CoupletDefCor Weight	8UI	0x00	RW	Couplet defect correction in short pipe

Table 15. User interface set 0 PWL compression registers [0x217D to 0x227D]

Index	Byte	Register name	Data type	Default	Type	Comment
0x217D		ExponentBias	8UI	0x15	RW	[7:5] - Reserved. [4:0] - Piecewise linear compression exponent bias
0x217E	HI	Abscissa_0	32UR	0x00	RW	[31:22] - Reserved [21:4] - 0th piecewise linear compression abscissa [3:0] - Reserved
0x217F				0x00		
0x2180				0x00		
0x2181	LO			0x00		
0x2182	HI	Abscissa_1	32UR	0x00	RW	[31:22] - Reserved [21:4] - 1st piecewise linear compression abscissa [3:0] - Reserved
0x2183				0x00		
0x2184				0x04		
0x2185	LO			0x00		
...	...	...	...	...	...	...
0x217E + 4.n	HI	Abscissa_n	32UR		RW	[31:22] - Reserved [21:4] - nth piecewise linear compression abscissa [3:0] - Reserved
0x217F + 4.n						
0x2180 + 4.n						
0x2181 + 4.n	LO					
...	...	...	...	...	...	...
0x21FA	HI	Abscissa_31	32UR	0x00	RW	[31:22] - Reserved [21:4] - 31st piecewise linear compression abscissa [3:0] - Reserved
0x21FB				0x30		
0x21FC				0xF0		
0x21FD	LO			0x50		
0x21FE	HI	Lut_0	32UR	0xB0	RW	[31:8] - 0th piecewise linear compression look-up table value [7:0] - Reserved
0x21FF				0x00		
0x2200				0x00		
0x2201	LO			0x00		

Table 15. User interface set 0 PWL compression registers [0x217D to 0x227D] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2202	HI	Lut_1	32UR	0xA9	RW	[31:8] - 1st piecewise linear compression look-up table value [7:0] - Reserved
0x2203				0x81		
0x2204				0x00		
0x2205	LO			0x00		
...	...	...	...	...	...	...
0x21FE + 4.n	HI	Lut_n	32UR		RW	[31:8] - nth piecewise linear compression look-up table value [7:0] - Reserved
0x21FF + 4.n						
0x2200 + 4.n						
0x2201 + 4.n	LO					
...	...	...	...	...	...	...
0x227A	HI	Lut_31	32UR	0x0C	RW	[31:8] - 31st piecewise linear compression look-up table value [7:0] - Reserved
0x227B				0x7F		
0x227C				0x28		
0x227D	LO			0x00		

Table 16. User interface set 0 statistics control register [0x227E to 0x2286]

Index	Byte	Register name	Data type	Default	Type	Comment
0x227E		Hist0_Control	8UI	0x28	RW	[6:2] -HDRPixelSlice [1:0] -DataPipeSel: 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame
0x227F		Hist0_BarrelShift	8UI	0x00	RW	
0x2280		Hist1_Control	8UI	0x28	RW	[6:2] -HDRPixelSlice [1:0] -DataPipeSel: 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame
0x2281		Hist1_BarrelShift	8UI	0x00	RW	

Table 16. User interface set 0 statistics control register [0x227E to 0x2286] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2282		Hist2_Control	8UI	0x28	RW	[6:2] -HDRPixelSlice [1:0] - DataPipeSel 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame
0x2283		Hist2_BarrelShift	8UI	0x00	RW	
0x2284		Hist3_Control	8UI	0x28	RW	[6:2] -HDRPixelSlice [1:0] - DataPipeSel 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame
0x2285		Hist3_BarrelShift	8UI	0x00	RW	
0x2286		Accumulator_Control	8UI	0x18	RW	[6:2] - HDRPixelSlice [1:0] - DataPipeSel 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame

4.2.8 User interface set 1 registers [0x2287 to 0x23E9]

Two user interface register sets are provided to allow frame-by-frame context switching of exposure, frame length, HDR merge, defect correction, PWL compression parameters and statistics accumulation. While one frame is being streamed using the active context settings, new settings may be programmed to the non-active context, ready for use by the next frame.

These settings must be written with the grouped_parameter_hold flag set. The status of the integration and gain registers is reported in the frame status line.

Table 17. User interface set 1 integration and gain registers [0x2287 to 0x2295]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2287		TokenId	8UI	0x05	RW	Token ID used for identification of this UI Set
0x2288	HI	CoarseTimeLong	16UI	0x03	RW	Coarse integration time for long pipe (lines) Min = 0 lines Max = framelength_lines - 115
0x2289	LO			0x84		
0x228A	HI	CoarseTimeMedium	16UI	0x00	RW	Coarse integration time for medium pipe (lines) Min = 0 lines Max = 96
0x228B	LO			0x5F		
0x228C	HI	CourseTimeShort	16UI	0x00	RW	Coarse integration time for short pipe (lines) Min = 0 lines Max = 13
0x228D	LO			0x0D		
0x228E		AnalogGain	8C	0x00	RW	Global analog gain (coded) 0x00 = Gain x1.0 (+0dB) 0x01 = Gain x1.07 (+0.6dB) 0x02 = Gain x1.1 (+1.2dB) 0x03 = Gain x1.2 (+1.8dB) 0x04 = Gain x1.3 (+2.5dB) 0x05 = Gain x1.5 (+3.3dB) 0x06 = Gain x1.6 (+4.1dB) 0x07 = Gain x1.8 (+5.0dB) 0x08 = Gain x2.0 (+6.0dB) 0x09 = Gain x2.3 (+7.2dB) 0x0A = Gain x2.7 (+8.5dB) 0x0B = Gain x3.2 (+10.1dB) 0x0C = Gain x4.0 (+12.0dB) 0x0D = Gain x5.3 (+14.5dB) 0x0E = Gain x8.0 (+18.0dB) 0x0F = Gain x16.0 (+24.0dB)

Table 17. User interface set 1 integration and gain registers [0x2287 to 0x2295] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x228F		PixelGain	8UI	0x01	RW	[2:0] - Pixel gain: 0x01 = High gain 0x04 = Low gain [7] - GopReset
0x2290	HI	FrameLengthLines	16UI	0x03	RW	Frame length (lines) Min = 159 Max = 65536
0x2291	LO			0xFC		
0x2292	HI	DarkOffsetMed	16UI	0x00	RW	
0x2293	LO			0x00		
0x2294	HI	DarkOffsetShort	16UI	0x00	RW	
0x2295	LO			0x00		

Table 18. User interface set 1 HDR merge registers [0x2296 to 0x22D9]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2296	HI	WB_DGain_GreenInRed	16UR	0x01	RW	Green (Red row) channel digital gain value
0x2297	LO			0x00		
0x2298	HI	WB_DGain_Red	16UR	0x01	RW	Red channel digital gain value
0x2299	LO			0x00		
0x229A	HI	WB_DGain_Blue	16UR	0x01	RW	Blue channel digital gain value
0x229B	LO			0x00		
0x229C	HI	WB_DGain_GreenInBlue	16UR	0x01	RW	Green (Blue row) channel digital gain value
0x229D	LO			0x00		
0x22A0	HI	HDR_DGain	16UR	0x10	RW	Post HDR digital gain applied on all color channels
0x22A1	LO			0x00		
0x22A2	HI	HDRLM_Startmerge	16UI	0x0F	RW	Long Medium start merge threshold
0x22A3	LO			0xFF		
0x22A4	HI	HDRLM_Endmerge	16UI	0x0F	RW	Long Medium end merge threshold
0x22A5	LO			0xFF		
0x22A6	HI	HDRLM_Knee1	16UI	0x0F	RW	Knee 1 parameter Below this value is normalized low exposure data
0x22A7	LO			0xFF		

Table 18. User interface set 1 HDR merge registers [0x2296 to 0x22D9] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x22A8	HI	HDRLM_Knee2	16UI	0x0F	RW	Knee 2 parameter Above this value is normalized high exposure data NOTE - One of the following conditions must be true: Knee1 == Knee2, or, (Knee2 - Knee1) > 7
0x22A9	LO			0xFF		
0x22AA	HI	HDRLM_GainMedium	16UR	0x04	RW	Normalization gain for low exposure data
0x22AB	LO			0x00		
0x22AC	HI	HDRLM_GainLong	16UR	0x04	RW	Normalization gain for high exposure data
0x22AD	LO			0x00		
0x22AE	HI	HDRLM_FlashThres1	32UR	0x00	RW	Flash threshold value 1
0x22AF				0x00		
0x22B0				0x0C		
0x22B1	LO			0xCD		
0x22B2	HI	HDRLM_FlashThres2	32UR	0x00	RW	Flash threshold value 2
0x22B3				0x00		
0x22B4				0x0C		
0x22B5	LO			0xCD		
0x22B6	HI	HDRLM_FlashGain	16IR	0x04	RW	Normalization gain for flash control
0x22B7	LO			0x00		
0x22B8	HI	HDRLM_SigmaGhost Thresh1	16UI	0xFF	RW	Ghost free sigma threshold 1
0x22B9	LO			0x00		
0x22BA	HI	HDRLM_SigmaGhost Thresh2	16UI	0xFF	RW	Ghost free sigma threshold 2 NOTE - the following condition must be maintained: GhostThresh2 - GhostThresh1 > 127
0x22BB	LO			0xFF		
0x22BC	HI	HDRLMS_Startmerge	32UR	0x00	RW	Start merge threshold Below this only linearization data
0x22BD				0x01		
0x22BE				0xFF		
0x22BF	LO			0xFF		
0x22C0	HI	HDRLMS_Endmerge	32UR	0x00	RW	End merge threshold Above this only linearization data
0x22C1				0x01		
0x22C2				0xFF		
0x22C3	LO			0xFF		

Table 18. User interface set 1 HDR merge registers [0x2296 to 0x22D9] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x22C4	HI	HDRLMS_Knee1	32UR	0x00	RW	Knee point 1 Below this normalized low exposure data
0x22C5				0x01		
0x22C6				0xFF		
0x22C7	LO			0xFF		
0x22C8	HI	HDRLMS_Knee2	32UR	0x00	RW	Knee point 2 Above this normalized high exposure data NOTE - One of the following conditions must be true: Knee1 == Knee2, or, (Knee2 - Knee1) > 7
0x22C9				0x01		
0x22CA				0xFF		
0x22CB	LO			0xFF		
0x22CC	HI	HDRLMS_GainShort	16IR	0x04	RW	Normalization gain for low exposure data
0x22CD	LO			0x00		
0x22CE	HI	HDRLMS_GainLongMed	16IR	0x04	RW	Normalization gain for high exposure data
0x22CF	LO			0x00		
0x22D0	HI	HDRLMS_FlashThres1	32UI	0x00	RW	Flash threshold value 1 (when Flash mode is enabled)
0x22D1				0x01		
0x22D2				0x99		
0x22D3	LO			0x9A		
0x22D4	HI	HDRLMS_FlashThres2	32UI	0x00	RW	Flash threshold value 2 (when Flash mode is enabled)
0x22D5				0x01		
0x22D6				0x99		
0x22D7	LO			0x9A		
0x22D8	HI	HDRLMS_FlashGain	16IR	0x04	RW	Normalization gain for flash control
0x22D9	LO			0x00		

Table 19. User interface set 1 defect correction registers [0x22DA to 0x22DF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x22DA		Long_SingletDefCor Weight	8UI	0x00	RW	Single defect correction in long pipe
0x22DB		Long_Couplet_DefCor Weight	8UI	0x00	RW	Couplet defect correction in long pipe
0x22DC		Medium_SingletDefCor Weight	8UI	0x00	RW	Single defect correction in medium pipe

Table 19. User interface set 1 defect correction registers [0x22DA to 0x22DF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x22DD		Medium_CoupletDefCor Weight	8UI	0x00	RW	Couplet defect correction in medium pipe
0x22DE		Short_SingletDefCor Weight	8UI	0x00	RW	Single defect correction in short pipe
0x22DF		Short_CoupletDefCor Weight	8UI	0x00	RW	Couplet defect correction in short pipe

Table 20. User interface set 1 PWL registers [0x22E0 to 0x23E0]

Index	Byte	Register name	Data type	Default	Type	Comment
0x22E0		ExponentBias	8UI	0x1B	RW	[7:5] - Reserved. [4:0] - Piecewise linear compression exponent bias
0x22E1	HI	Abscissa_0	32UR	0x00	RW	[31:22] - Reserved [21:4] - 0th piecewise linear compression abscissa [3:0] - Reserved
0x22E2				0x00		
0x22E3				0x00		
0x22E4	LO			0x00		
0x22E5	HI	Abscissa_1	32UR	0x00	RW	[31:22] - Reserved [21:4] - 1st piecewise linear compression abscissa [3:0] - Reserved
0x22E6				0x00		
0x22E7				0x08		
0x22E8	LO			0x40		
...	...	...	...	...	...	...
0x22E1 + 4.n	HI	Abscissa_n	32UR		RW	[31:22] - Reserved [21:4] - nth piecewise linear compression abscissa [3:0] - Reserved
0x22E2 + 4.n						
0x22E3 + 4.n						
0x22E4 + 4.n	LO					
...	...	...	...	...	...	...
0x235D	HI	Abscissa_31	32UR	0x00	RW	[31:22] - Reserved [21:4] - 31st piecewise linear compression abscissa [3:0] - Reserved
0x235E				0x00		
0x235F				0xFF		
0x2360	LO			0xF0		

Table 20. User interface set 1 PWL registers [0x22E0 to 0x23E0] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2361	HI	Lut_0	32UR	0xF0	RW	[31:8] - 0th piecewise linear compression look-up table value [7:0] - Reserved
0x2362				0x00		
0x2363				0x00		
0x2364	LO			0x00		
0x2365	HI	Lut_1	32UR	0xF0	RW	[31:8] - 1st piecewise linear compression look-up table value [7:0] - Reserved
0x2366				0x00		
0x2367				0x84		
0x2368	LO			0x00		
...	...	...	...	...	...	...
0x2361 + 4.n	HI	Lut_n	32UR		RW	[31:8] - nth piecewise linear compression look-up table value [7:0] - Reserved
0x2362 + 4.n						
0x2363 + 4.n						
0x2364 + 4.n	LO					
...	...	...	...	...	...	...
0x23DD	HI	Lut_31	32UR	0x00	RW	[31:8] - 31st piecewise linear compression look-up table value [7:0] - Reserved
0x23DE				0x0F		
0x23DF				0xFF		
0x23E0	LO			0x00		

Table 21. User interface set 1 statistics control registers [0x23E1 to 0x23E9]

Index	Byte	Register name	Data type	Default	Type	Comment
0x23E1		Hist0_Control	8UI	0x28	RW	[6:2] - HDRPixelSlice [1:0] - DataPipeSel 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame
0x23E2		Hist0_BarrelShift	8UI	0x00	RW	

Table 21. User interface set 1 statistics control registers [0x23E1 to 0x23E9] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x23E3		Hist1_Control	8UI	0x28	RW	[6:2] -HDRPixelSlice [1:0] -DataPipeSel 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame
0x23E4		Hist1_BarrelShift	8UI	0x00	RW	
0x23E5		Hist2_Control	8UI	0x28	RW	[6:2] - HDRPixelSlice [1:0] - DataPipeSel 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame
0x23E6		Hist2_BarrelShift	8UI	0x00	RW	
0x23E7		Hist3_Control	8UI	0x28	RW	[6:2] - HDRPixelSlice [1:0] - DataPipeSel 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame
0x23E8		Hist3_BarrelShift	8UI	0x00	RW	
0x23E9		Accumulator_Control	8UI	0x18	RW	[6:2] - HDRPixelSlice [1:0] - DataPipeSel 0 = HDR 1 = Short Exposed Frame 2 = Medium Exposed Frame 3 = Long12Bit Exposed Frame

4.2.9 Temperature sensor registers [0x2429 to 0x242D]

Table 22. Temperature sensor registers [0x2429 to 0x242D]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2429		TempSensorStatus	8UI	0x00	DNW	[3] - TempSensorTopOverflow: 1 = Overflow [2]- TempSensorBottomOverflow: 1 =Overflow [1:0] - Calibration: 0 = No calibration 1 = Single point calibration 2 =Dual point calibration 3 = Cal error
0x242C		TempSensorTop	8SI	0x00	DNW	Current temperature from sensor top
0x242D		TempSensorBottom	8SI	0x00	DNW	Current temperature from sensor bottom

4.2.10 Dark cal control registers [0x244D - 0x2470]

Table 23. Darkcal control register [0x244D - 0x2470]

Index	Byte	Register name	Data type	Default	Type	Comment
0x244D	HI	DarkCal_DarkOffset Longx4	16UI	0x00	RW	Dark Offset added to the data on Longx4 (Longx1 pipe will get wDarkOffsetLongx1 >> 2). This register is consumed at the start of stream
0x244E	LO			0x00		
0x244F	HI	DarkCal_DarkOffset ChannelComp	16UI	0x00	RW	[15:14] - Short_darkcompGiB [13:12] - Short_darkcompBlu [11:10] - Short_darkcompRed [9:8] - Short_darkcompGiR [7:6] - Med_darkcompGiB [5:4] - Med_darkcompBlu [3:2] - Med_darkcompRed [1:0] - Med_darkcompGiR
0x2450	LO			0x00		
0x2451	HI	DarkAvg_Longx4 _GreenInRed	16UI	0x00	RW	Average dark level
0x2452	LO			0x00		
0x2453	HI	DarkAvg_Longx4_Red	16UI	0x00	RW	Average dark level
0x2454	LO			0x00		
0x2455	HI	DarkAvg_Longx4_Blue	16UI	0x00	RW	Average dark level
0x2456	LO			0x00		
0x2457	HI	DarkAvg_longx4 _GreenInBlue	16UI	0x00	RW	Average dark level
0x2458	LO			0x00		

Table 23. Darkcal control register [0x244D - 0x2470] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2459	HI	DarkAvg_Longx1 _GreenInRed	16UI	0x00	RW	Average dark level
0x245A	LO			0x00		
0x245B	HI	DarkAvg_Longx1_Red	16UI	0x00	RW	Average dark level
0x245C	LO			0x00		
0x245D	HI	DarkAvg_Longx1_Blue	16UI	0x00	RW	Average dark level
0x245E	LO			0x00		
0x245F	HI	DarkAvg_Longx1 _GreenInBlue	16UI	0x00	RW	Average dark level
0x2460	LO			0x00		
0x2461	HI	DarkAvg_Medium _GreenInRed	16UI	0x00	RW	Average dark level
0x2462	LO			0x00		
0x2463	HI	DarkAvg_Medium_Red	16UI	0x00	RW	Average dark level
0x2464	LO			0x00		
0x2465	HI	DarkAvg_Medium_Blue	16UI	0x00	RW	Average dark level
0x2466	LO			0x00		
0x2467	HI	DarkAvg_Medium _GreenInBlue	16UI	0x00	RW	Average dark level
0x2468	LO			0x00		
0x2469	HI	DarkAvg_Short _GreenInRed	16UI	0x00	RW	Average dark level
0x246A	LO			0x00		
0x246B	HI	DarkAvg_Short_Red	16UI	0x00	RW	Average dark level
0x246C	LO			0x00		
0x246D	HI	DarkAvg_Short_Blue	16UI	0x00	RW	Average dark level
0x246E	LO			0x00		
0x246F	HI	DarkAvg_Short _GreenInBlue	16UI	0x00	RW	Average dark level
0x2470	LO			0x00		

4.2.11 Test pattern registers [0x2475 to 0x2481]

Table 24. Test pattern control registers [0x2475 to 0x2481]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2475		TestPatternControl	8UI	0x01	RW	[6:2] - TestPatternSelect 0 = None 1 = Solid color 2 = 100% color bars 3 = Fade to grey color bars 16 = Horizontal grey scale 17 = Vertical grey scale 18 = Diagonal grey scale 19 = PN28 pseudo random pattern 20 = Smearing test [1:0] - Test pattern mode 0 = Standard mode 1 = Digital ASIL mode (default) 2 = HDR ramp mode
0x2476	HI	HDRPattern_Y_Start	16UI	0x00	RW	HDR pattern y start position
0x2477	LO			0x00		
0x2478	HI	HDRPattern_Y_Size	16UI	0x03	RW	HDR pattern y size
0x2479	LO			0xD6		
0x247A	HI	HDRPattern_Lx4_Ramp_Incr	16UR	0x06	RW	HDR pattern Lx4 ramp incr
0x247B	LO			0x00		
0x247C	HI	HDRPattern_Lx1_Ramp_Incr	16UR	0x03	RW	HDR pattern Lx1 ramp incr
0x247D	LO			0x00		
0x247E	HI	HDRPattern_M_Ramp_Incr	16UR	0x02	RW	HDR pattern M ramp incr
0x247F	LO			0x00		
0x2480	HI	HDRPattern_S_Ramp_Incr	16UR	0x01	RW	HDR pattern S ramp incr
0x2481	LO			0x93		

4.2.12 Defect map register [0x2483]

Table 25. Defect map register [0x2483]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2483		BruceNbCouplets	8UI	0x00	DNW	Contains the number of mapped defect pixels stored in NVM

4.2.13 Gain merge compensation control registers [0x248B - 0x2492]

Table 26. Gain merge compensation control registers [0x248B - 0x2492]

Index	Byte	Register name	Data type	Default	Type	Comment
0x248B		HDRLong12_control	8UI	0x00	RW	[1] - Refstream: 0 = LongX1 reference 1 = LongX4 reference [0] - Mergemode: 0 = Linearise 1 = Merge only
0x248C	HI	HDRLong12_gainlongx1	16UR	0x0F	RW	Gain applied on LongX1 (fixed point 2.10).
0x248D	LO			0xFF		
0x248E	HI	HDRLong12_gainlongx4	16UR	0x04	RW	Gain applied on LongX4 (fixed point 2.10).
0x248F	LO			0x00		
0x2490		HDRLM_control	8UI	0x02	RW	[6] - EnableGhostFree: 1 = Enable ghost free mode [5] - EnableFlash: 1 = Enable flash repair mode [4] - Refstream: 0 = Long12 1 = Medium [3] - DecideOnShort: 0 = Luma comparisons made on Long 1 = Luma comparisons made on Medium [2:0] - MergeMode: 0 = Linearise 1 = Merge only 2 = Merge/Linearize 3 = Grad to add 4 = Grad to merge

Table 26. Gain merge compensation control registers [0x248B - 0x2492] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2491		HDRLMS_control	8UI	0x02	RW	[5] - EnableFlash: 1 = Enable flash repair mode [4] - Refstream: 0 = Long12 1 = Medium [3] - DecideOnShort: 0 = Luma comparisons made on LongMedium 1 = Luma comparisons made on Short [2:0] - MergeMode: 0 = Linearise 1 = Merge only 2 = Merge/Linearize 3 = Grad to add 4 = Grad to merge
0x2492		PWL_control	8UI	0x01	RW	[1] - PWLBypassMode: 0 = MSB only 1 = LSB only [0] - PWLEnable: 1 = PWL enabled

4.2.14 Output interface control registers [0x249B - 0x24A3]

Table 27. Output interface control registers [0x249B - 0x24A3]

Index	Byte	Register name	Data type	Default	Type	Comment
0x249B		SlcTrailerControl	8UI	0x00	RW	[1:0] - Stat source: 0 = Short expo pipe 1 = Medium expo pipe 2 = Longx1 expo pipe 3 = Longx4 expo pipe
0x249C		SmiaOutIF_Control	8UI	0x01	RW	[2] - CSI2 DataClip enable: 0 = Data unclipped 1 = Data clipped to 16 min [1] - CSI2 ULPS mode enable: 0 = ULPS disabled 1 = ULPS enable [0] - UIx4AutoEnable: 0 = Manual UIx4 value control 1 = Automatic UIx4 value control
0x24A2		ParOutIF_Drive	8UI	0x02	RW	[1:0] - PinDriveStrength: 1 = All signals low drive strength except PIXCLK and GPIO. 2 = All signals normal drive strength
0x24A3		ParOutIF_Control	8UI	0x04	RW	[7] - SyncCodeProtect: 0 = Raw data 1 = Data sync code protected [6] - InvertPixelClock: 1 = Invert pixel clock [5] - InterframeClockGating: 0 = Interframe clock gated [4] - InterlineClockGating 0 = Interline clock gated [3] - BlankLineClockGating 0 = Blank line clock gated [2] - GatingControl: 0 = Gating control enabled 1 = Free running clock (default) [1] - VSyncPolarity: 1 = VSync active low [0] - HSyncPolarity 1 = HSync active low NOTE - use of some clock gating combinations may mean the PIXCLK is not active during the period the HSYNC and VSYNC signals are valid.

4.2.15 Statistics control registers [0x24A6 - 0x24D3

In *Table 28* below, data refers only to RGB.

Table 28. Statistics control registers [0x248B - 0x24D3]

Index	Byte	Register name	Data type	Default	Type	Comment
0x24A6		StatsControl	8UI	0x00	RW	[0] - bAccZoneErrorStatus: 0 = Accumulation zone fully within pixel array. 1 = Accumulation zone extends beyond pixel array.
0x24A7		Acc8x6_Control	8UI	0x04	RW	[5:4] - AccColorSel: 0 = Green in red 1 = Red 2 = Blue 3 = Green in blue [2] - AccType: 0 = Zoned 1 = Flat [1:0] - AccMode: 0 = Full pixel value 1 = Clip pixel val 2 = Histogram 3 = No accumulation
0x24A8	HI	Axx8x6_XSize	16UI	0x00	RW	Accumulator X size
0x24A9	LO			0x64		
0x24AA	HI	Axx8x6_YSize	16UI	0x00	RW	Accumulator Ysize
0x24AB	LO			0x64		
0x24AC	HI	Axx8x6_XOffset	16UI	0x00	RW	Accumulator X offset
0x24AD	LO			0xFC		
0x24AE	HI	Axx8x6_YOffset	16UI	0x00	RW	Accumulator Y offset
0x24AF	LO			0xBE		
0x24B0		Histo0_Control	8UI	0x00	RW	[2:0] - HistogramColorSelect: 0 = Green in red 1 = Red 2 = Blue 3 = Green in blue 4 = All green 5 = All colors
0x24B1	HI	Histo0_XSize	16UI	0x03	RW	Histogram0 X size
0x24B2	LO			0x20		
0x24B3	HI	Histo0_YSize	16UI	0x02	RW	Histogram0 Ysize
0x24B4	LO			0x58		
0x24B5	HI	Histo0_XOffset	16UI	0x00	RW	Histogram0 X offset
0x24B6	LO			0xFC		

Table 28. Statistics control registers [0x248B - 0x24D3] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x24B7	HI	Histo0_YOffset	16UI	0x00	RW	Histogram0 Yoffset
0x24B8	LO			0xBE		
0x24B9		Histo1_Control	8UI	0x00	RW	[[2:0] - HistogramColorSelect: 0 = Green in red 1 = Red 2 = Blue 3 = Green in blue 4 = All green 5 = All colors
0x24BA	HI	Histo1_XSize	16UI	0x03	RW	Histogram1 X size
0x24BB	LO			0x20		
0x24BC	HI	Histo1_YSize	16UI	0x02	RW	Histogram1 Y size
0x24BD	LO			0x58		
0x24BE	HI	Histo1_XOffset	16UI	0x00	RW	Histogram1 X offset
0x24BF	LO			0xFC		
0x24C0	HI	Histo1_YOffset	16UI	0x00	RW	Histogram1 Y offset
0x24C1	LO			0xBE		
0x24C2		Histo2_Control	8UI	0x00	RW	[[2:0] - HistogramColorSelect: 0 = Green in red 1 = Red 2 = Blue 3 = Green in blue 4 = All green 5 = All colors
0x24C3	HI	Histo2_XSize	16UI	0x03	RW	Histogram2 X size
0x24C4	LO			0x20		
0x24C5	HI	Histo2_YSize	16UI	0x02	RW	Histogram2 Y size
0x24C6	LO			0x58		
0x24C7	HI	Histo2_XOffset	16UI	0x00	RW	Histogram2 X offset
0x24C8	LO			0xFC		
0x24C9	HI	Histo2_YOffset	16UI	0x00	RW	Histogram2 Y offset
0x24CA	LO			0xBE		
0x24CB		Histo3_Control	8UI	0x00	RW	[2:0] - HistogramColorSelect: 0 = Green in red 1 = Red 2 = Blue 3 = Green in blue 4 = All green 5 = All colors

Table 28. Statistics control registers [0x248B - 0x24D3] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x24CC	HI	Histo3_XSize	16UI	0x03	RW	Histogram3 X size
0x24CD	LO			0x20		
0x24CE	HI	Histo3_YSize	16UI	0x02	RW	Histogram3 Y size
0x24CF	LO			0x58		
0x24D0	HI	Histo3_XOffset	16UI	0x00	RW	Histogram3 X offset
0x24D1	LO			0xFC		
0x24D2	HI	Histo3_YOffset	16UI	0x00	RW	Histogram3 Y offset
0x24D3	LO			0xBE		

4.2.16 NVM buffer data registers [0x2A00 to 0x2BFF]

The contents of the NVM are buffered to the registers detailed below when the sensor boots up.

Table 29. NVM buffer data registers [0x2A00 to 0x2BFF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x2A00	HI	nvm_buffer_data_0	32UI	0x00	RW	
0x2A01				0x00		
0x2A02				0x00		
0x2A03	LO			0x00		
0x2A04	HI	nvm_buffer_data_1	32UI	0x00	RW	
0x2A05				0x00		
0x2A06				0x00		
0x2A07	LO			0x00		
...	...	...	...	...	...	...
0x2A00 + 4.n	HI	nvm_buffer_data_n	32UI	0x00	RW	
0x2A01 + 4.n				0x00		
0x2A02 + 4.n				0x00		
0x2A03 + 4.n	LO			0x00		
...	...	...	...	...	...	...

Table 29. NVM buffer data registers [0x2A00 to 0x2BFF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x2BFC	HI	nvm_buffer_data_127	32UI	0x00	RW	
0x2BFD				0x00		
0x2BFE				0x00		
0x2BFF	LO			0x00		

4.2.17 I2C bus slave address register [0x41A8]

This register holds the I^2C bus slave address of the sensor.

Table 30. I2C slave registers[0x41A8]

Index	Byte	Register name	Data type	Default	Type	Comment
0x41A8		I2C_Slave_Addr	8UI	0x20	RW	[7] - Must be set to zero. [6:1] - The slave address of the sensor. [0] - Must be set to zero.

5 Video data interface

The video data stream is output from the image sensor through either the camera serial interface (CSI-2) or the parallel ITU interface. Both interfaces can transmit video data and other auxiliary information.

5.1 MIPI CSI-2 serial data link

Image data may be transferred to the companion device through a dual-lane MIPI CSI-2 serial interface. The CSI-2 interface is capable of transmitting at up to 528 Mbit/s per lane. Full resolution images (in 22:12-bit compressed format) may be transferred at up to 45 fps and 720p resolution images at up to 60 fps.

The CSI-2 interface is low EMI and more suitable for use over longer transmission distances when compared with the parallel interface. The CSI-2 interface is suitable for use in potentially noisy environments.

For full details of the MIPI CSI-2 interface, refer to the *MIPI Alliance Standard for Camera Serial Interface (CSI-2) - Version 1.00*.

5.1.1 Features

The image sensor is MIPI CSI-2 D-PHY v1.1 compliant.

The CSI-2 clock and data lane transmitters support:

- unidirectional master
- HS-TX, high speed transmit
- LP-TX, low power transmit
- CIL-MUYN function (data transmitter only)
- CIL-MCNN function (clock transmitter only)

Physical layer

The physical layer (D-PHY) of the CSI-2 interface is based on LVDS signalling, resulting in reduced EMI and excellent EMC, suitable for use in potentially noisy environments. Data and clock signals are transmitted over balanced 100 Ω differential-impedance transmission lines.

The CSI-2 MIPI D-PHY physical layer comprises of:

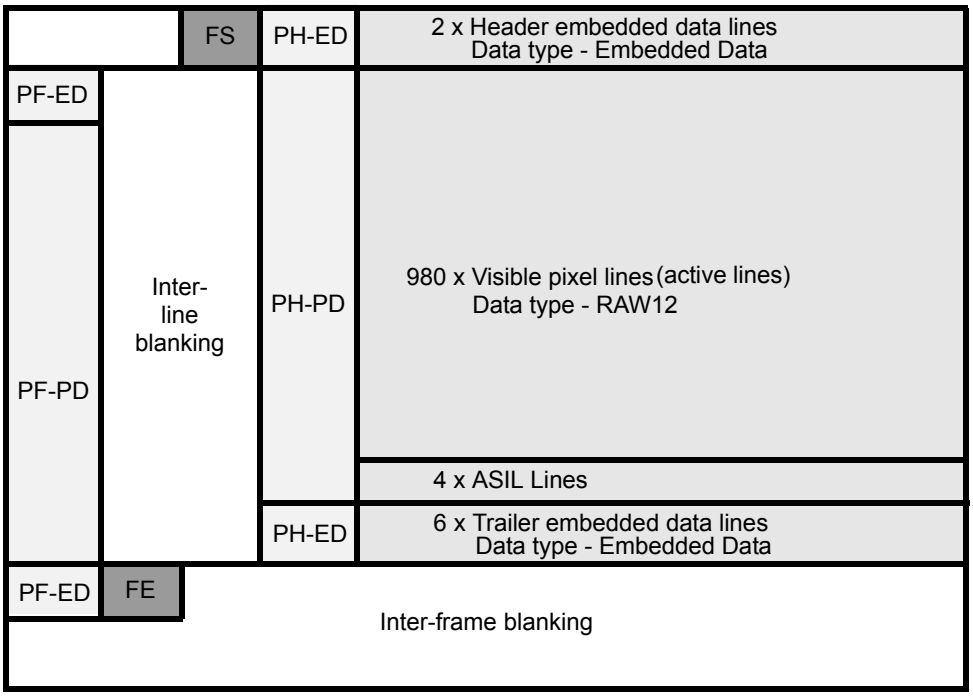
- one clock lane and two data lanes
- unidirectional clock lane supporting ultra low power mode (ULPM)
- unidirectional data lane supporting ULPM (using forward escape mode)
- power on/off and reset sequences are defined as transitions to/from ULPM

The CSI-2 interface may be configured as single or dual lane. The data lanes may be swapped if required. Similarly, the sense of a data lane may be switched. The slew rate of the clock and data lanes is configurable. The CSI-2 interface will remain in a high impedance state if the parallel interface has been selected as the output interface.

5.1.2 Frame format

The structure of the image frame for the CSI-2 interface is shown in *Figure 16* and described by the data types in *Table 31* and *Table 32*.

Figure 16. CSI-2 frame format



FS - Frame start (short packet)
FE - Frame end (short packet
PH-ED - Packet header for embedded data (long packet)
PF-ED - Packet footer for embedded data (long packet)
PH-PD - Packet header for pixel data (long packet)
PF-PD - Packet footer for pixel data (long packet)

Table 31. CSI-2 short packet data types

Name	Description	Data type
FS	Frame start	0x00
FE	Frame end	0x01

Table 32. CSI-2 long packet data types

Name	Description	Data type
PH-ED	Embedded data	0x12
PH-PD	RAW12 (pixel data)	0x2C

Visible pixel lines

The visible pixels contain valid image data. The image sensor only supports the RAW12 data format which is a 12-bit depth raw Bayer format.

ASIL data lines

There are always 4 ASIL data lines immediately following the visible pixel lines.

Embedded data lines

The embedded data lines provide a mechanism to embed non-image data such as sensor configuration details and image statistics values within a frame of CSI-2 data.

There are always 2 leading data lines and 6 trailing data lines transmitted with each image frame.

Inter-line blanking

During inter-line blanking the CSI-2 interface remains in the low power (LP) state. (There is no concept of line blanking being transmitted, the interface simply spends longer in the LP state between active line data.)

Inter-frame padding/frame blanking

During inter-frame blanking the CSI-2 interface remains in the low power (LP) state. (There is no concept of frame blanking being transmitted, the interface simply spends longer in the LP state between active frame data.)

5.2 Parallel ITU data link

Image data may be transferred to the companion device through a 12-bit parallel ITU interface. The parallel ITU interface is capable of transmitting at up to 792 Mbit/s (66 MHz). Full resolution images (in 22:12-bit compressed format) may be transferred at up to 45 fps and 720p resolution images at up to 60 fps.

5.2.1 Features

Physical layer

The physical layer (D-PHY) of the parallel interface is via open-ended signal lines and therefore care should be taken to minimize their length, EMI and crosstalk. Data is transmitted over 12 signal lines and clocked by a pixel clock (PIX-CLK). The parallel interface will remain in a high impedance state if deselected.

Embedded data lines

The embedded data lines provide a mechanism to embed non-image data such as sensor configuration details and image statistics values within a frame of ITU data.

There are always 2 leading data lines and 10 trailing data lines transmitted with each image frame.

Data synchronization methods

External capture systems may synchronize with the data output using ITU-R BT.601 compatible hardware synchronization signals, consisting of horizontal sync (HSYNC) and vertical sync (VSYNC).

The synchronization signals can be configured to meet the needs of the companion device.

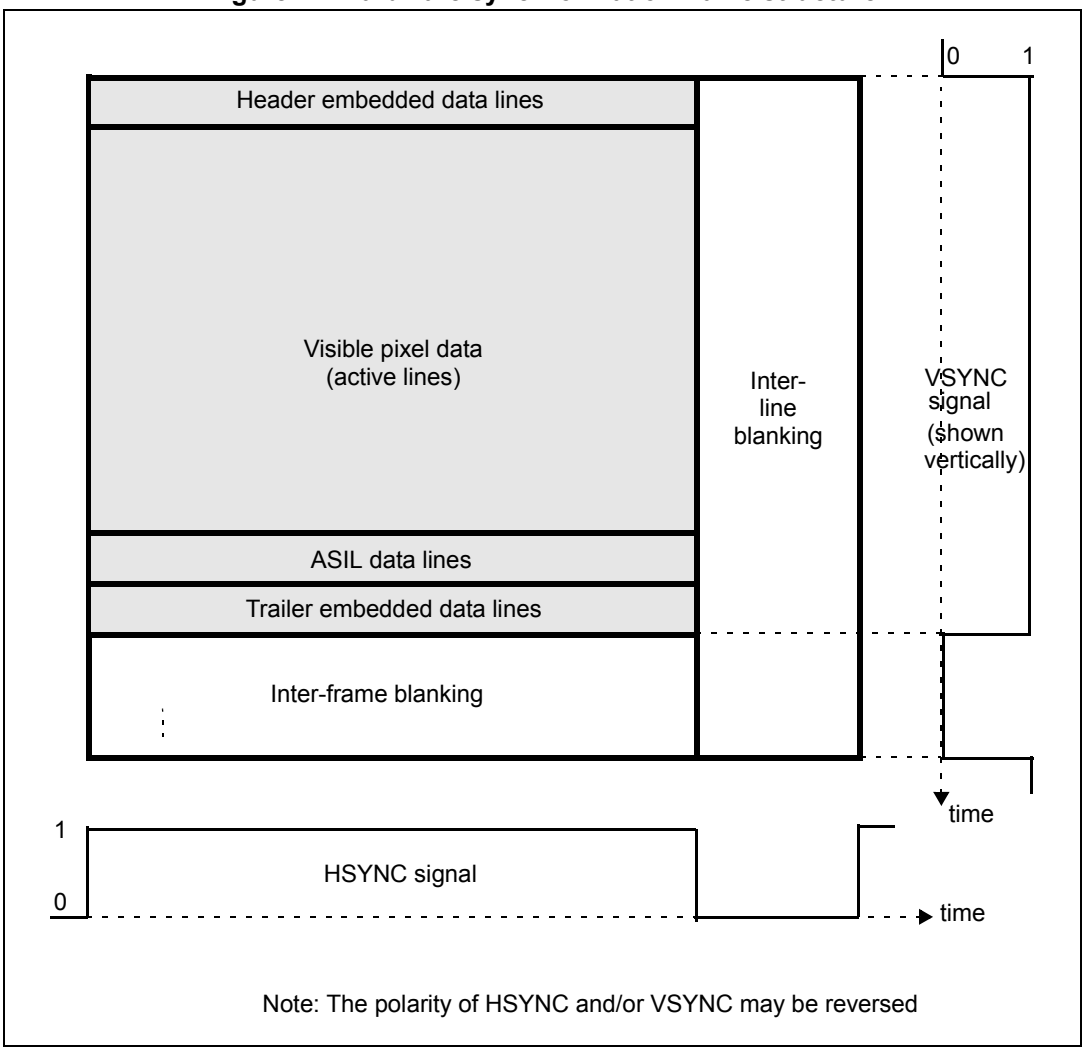
Pixel clock (PIX-CLK)

The pixel clock is programmable such that data may be clocked on the rising or falling edge of the pixel clock.

5.2.2 Frame format - hardware synchronization

The image sensor provides two programmable hardware synchronization signals: VSYNC and HSYNC. The position of these signals within the image frame is automatically set so that the signals track the active video portion of the output frame regardless of its size.

Figure 17. Hardware synchronization frame structure



Horizontal synchronization (HSYNC) signal

The HSYNC signal envelops all the visible pixel data (active lines) on every line in the image frame regardless of the programmed image size.

The HSYNC signal is programmable with the following options:

- enable/disable
- select polarity
- HSYNC during all lines (active lines as well as inter-frame blanking lines) or during active lines only

Vertical synchronization (VSYNC) signal

The VSYNC signal envelops all the visible (active) video lines in the image frame regardless of the programmed image size.

The VSYNC signal is programmable with the following options:

- enable/disable
- select polarity

6 Video timing

This chapter should be read in conjunction with the section on video timing found within the SMIA Functional Specification (Section 5 - Video Timing).

The following video timing features are supported:

- external synchronization of frame start using an I^2C command or a hardware signal
- single region windowing (window of interest)
- dual register banks are available in firmware to allow per frame context switching between different timing sets
- subsampling of pixel data
- programmable line and frame blanking
- vertical and/or horizontal image mirroring

6.1 Programmable image size

The native size of the pixel array is 1304 x 980.

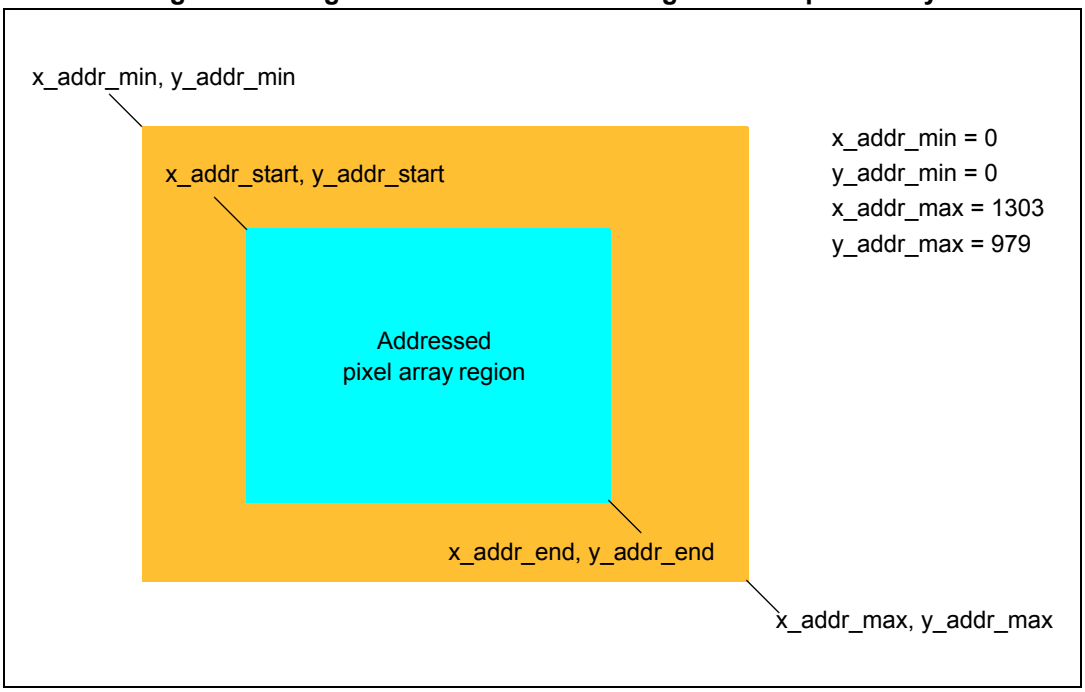
A region of the pixel array may be defined by programming the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers. The addressed region of the array is used in any subsequent subsampling.

The x_output_size and y_output_size registers are not intended as the primary cropping controls. They are intended to define the position of the frame end[(a)] so that the sensor does not need to calculate this based on the window of interest, digital crop or sub-sampling settings.

The companion device should set the output sizes to exactly enclose the output image data. If the companion device does not do this, the image sensor will treat the output sizes as being calculated from the top left hand corner of the output array. If the programmed output sizes are smaller than the output data size, the output data is cropped from the bottom and right limits. If the programmed output sizes are larger than the output data, the additional data lines are padded out to the defined output size with undefined data.

a. In the case of CSI-2 output interface, the frame end is marked by the FE code, refer to *Figure 16: CSI-2 frame format on page 67*. In the case of the parallel output interface, the frame end is marked by the VSYNC transition, refer to *Figure 17: Hardware synchronization frame structure on page 69*.

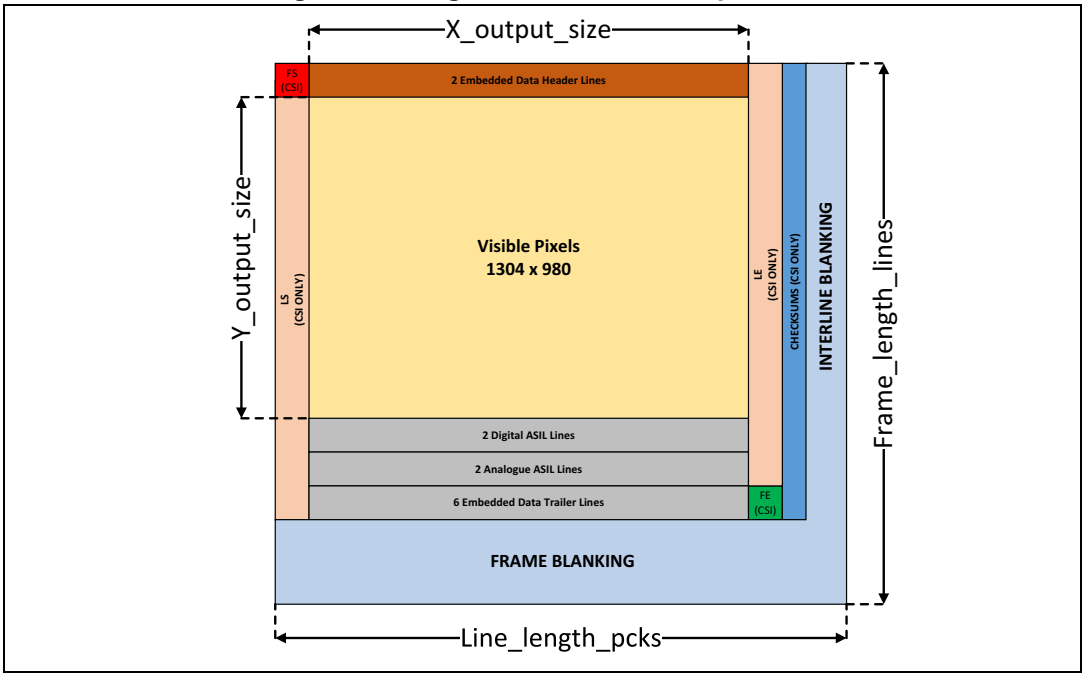
Figure 18. Programmable addressable region of the pixel array



The host must ensure that:

- the end address is greater than the start address
- the x and y start addresses are restricted to even numbers only, and the x and y end addresses are restricted to odd numbers only (this is to ensure that there is always an even number of pixels readout)
- the window of interest is not smaller than 264 x 264

Figure 19. Programmable frame output size



The host must ensure that the following frame timings are respected:

- frame_length_lines limits = (264 + 12datalines + 31minimum blanking) min, 65536 max.
- line_length_pck limits = 1438 min, 65536 max.
- x_start_addr limits = 0 min, 1039 (1303 - 264) max,
- y_start_addr limits = 0 min, 715 (979 - 264) max.
- x_op_size limits = 264min, 1304 max.
- y_op_size limits = 264min, 980 max.

6.2 Sub-sampled readout mode

Subsampling may be enabled by programming the x_odd_inc, y_odd_inc, x_even_inc and y_even_inc registers.

Table 33. Typical subsampling settings

Subsampling	x_odd_inc	y_odd_inc	x_even_inc	y_even_inc
Disabled	1	1	1	1
Bayer 2 x 2	3	3	1	1
Bayer 2 x 4	3	7	1	1
Bayer 4 x 4	7	7	1	1

If the pixel being readout has an even address then the address is incremented by the even increment value, either x_even_inc or y_even_inc. If the pixel being readout has an odd address then the address is incremented by the odd increment value, either x_odd_inc or y_odd_inc.

Subsampling acts upon the addressed region of the array which is determined by the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers.

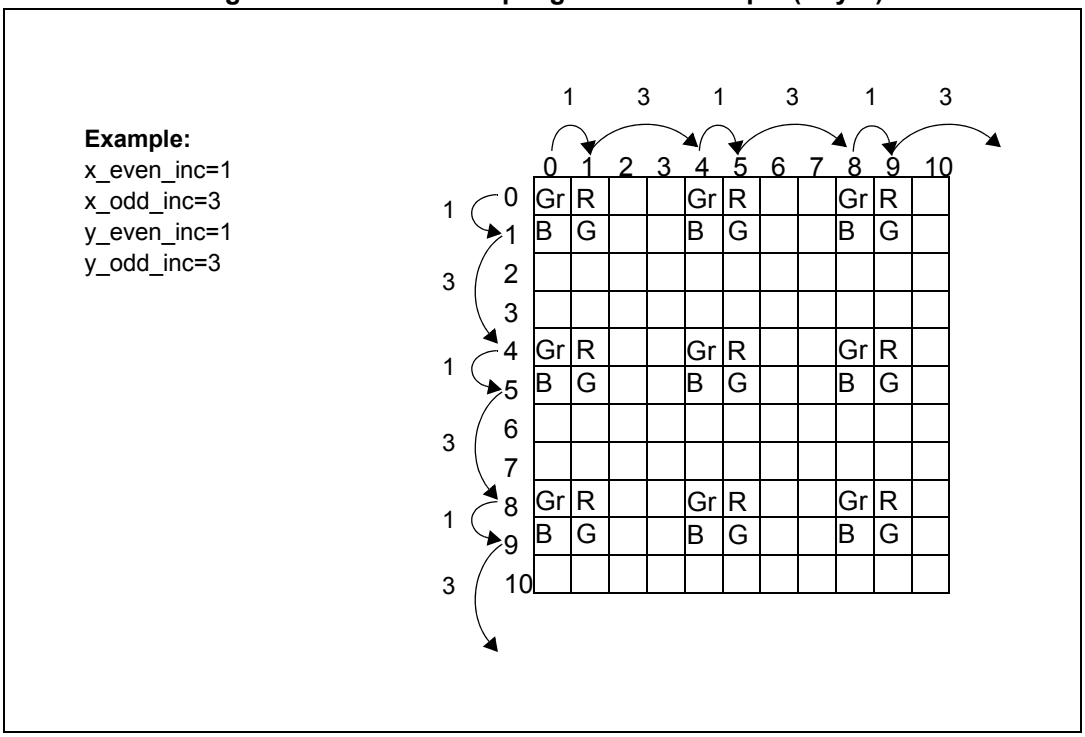
The host must ensure that the following limits are respected:

- x_odd_inc limits = 1 min, 15 max
- x_even_inc limits = 1 min, 15 max
- y_odd_inc limits = 1 min, 15 max, only odd values (1,3,5, etc) supported
- y_even_in limits = 1 min, 15 max, only odd values (1,3,5, etc) supported

The subsampling factor may be calculated as follows:

$$\text{sub\_sampling\_factor} = \frac{\text{even\_inc} + \text{odd\_inc}}{2}$$

Figure 20. 2 x 2 subsampling readout example (Bayer)



1. *Figure 20* valid only for RGB

6.3 External clock to pixel clock relationship

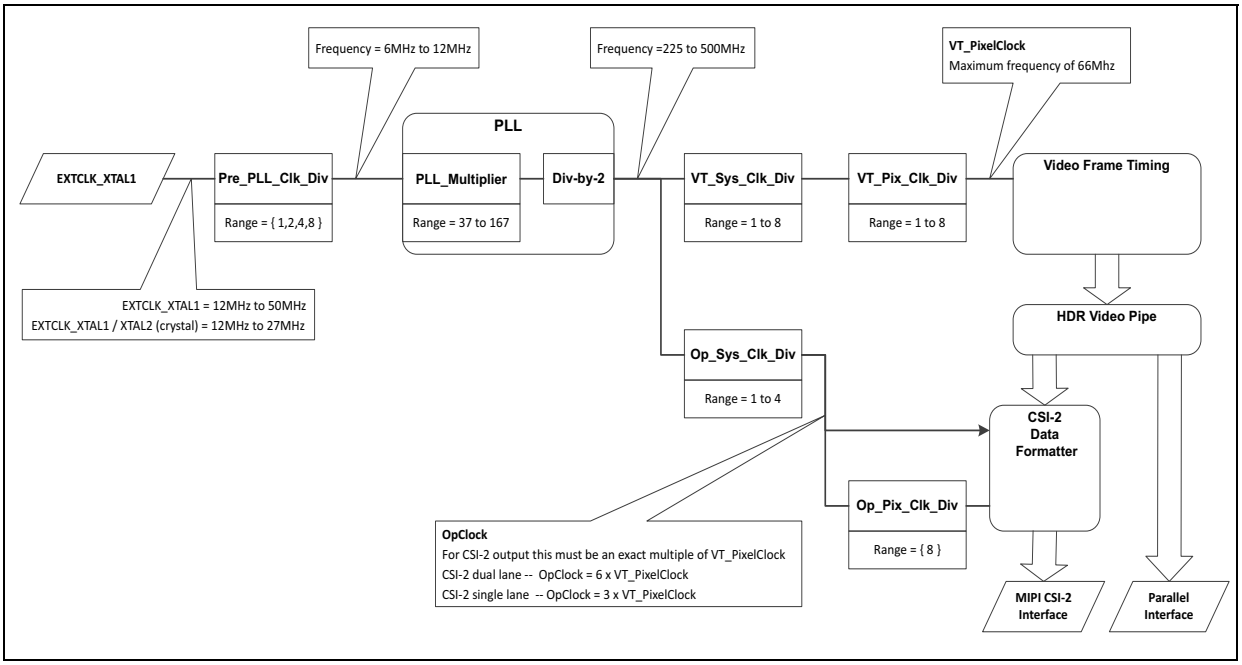
The image sensor has a clock generation block which contains a PLL (phase locked loop). This block generates all the necessary internal clocks from a single external clock input. Changes to the PLL settings on the image sensor will only be consumed when they are changed during standby.

Figure 21 shows the internal functional blocks, which define the relationship between the external input clock frequency and the pixel clock frequency.

The majority of the logic within the device is clocked by VT_PixelClock including the 12bit ITU interface if selected. If the CSI2 interface is used then the data rate is defined by OpClock giving a bit rate on the CSI2 interface of OpClock bytes or a maximum of 66MHz * 8bits = 528Mbits/sec

When the device is not streaming the PLL is bypassed and the internal digital logic, including the I^2C block, is clocked directly from the EXTCLK_XTAL1 input clock.

Figure 21. Clock settings



The equations relating the input clock frequency to pixel clock frequencies are:

$$VT\_PixelClock\_MHz = \frac{ExtClk\_Xtal1\_MHz \times PLL\_Multiplier}{Pre\_PLL\_Clk\_Div \times 2 \times VT\_Sys\_Clk\_Div \times VT\_Pix\_Clk\_Div}$$

$$OpClock\_MHz = \frac{ExtClk\_Xtal1\_MHz \times PLL\_Multiplier}{Pre\_PLL\_Clk\_Div \times 2 \times OP\_Sys\_Clk\_Div \times OP\_Pix\_Clk\_Div}$$

NOTE:

a) OP_Pix_Clk_Div must be kept at 8 for correct operation of CSI-2 interface.

b) The user must write the frequency of clock applied to the EXTCLK_XTAL1 input to the register 0x0310, ExtClk_Frequency_MHz.

6.3.1 Spread spectrum

The PLL contains a spread spectrum clock generator (SSCG) block for the purposes of EMI reduction. This feature is off by default and is intended for use if RF channel blocking becomes an issue on the host system. The modulation period and depth are fully programmable. The spread mode is selectable between center spread (default) or down spread. The SSCG registers must only be reprogrammed with new values when the sensor is in standby mode.

6.4 Variable line length and frame length

The frame rate of the array readout and therefore the output is governed by the line length, the frame length and the video timing pixel clock frequency.

The frame rate in frames per second (fps) may be calculated as:

$$\text{Framerate} = \frac{\text{VT\_PixelClock\_MHz}}{\text{line\_length\_pck} \times \text{frame\_length\_lines}}$$

where:

- line_length_pck is the line length, register Line_Length_PCK (0x0342)
- frame_length_lines is the frame length, register FrameLengthLines(0x212d)

The output frame rate of image sensor may be reduced by extending either the line length or the frame length. The extension is achieved by adding extra blank pixels at the end of a line or blank lines to act as timing padding.

Reducing the frame rate by extending the frame length (and not the line length) has the advantage that it does not reduce the pixel readout rate or the active frame time. Therefore it minimises potential unwanted motion artefacts in the image.

Frame timing examples are shown in *Table 34*.

Table 34. External clock frequency examples, full FOV, 45 fps

Ext Clk Freq	Pre-PLL Clk Div	PLL multiplier	VT Sys Clk Div	VT pixel Clk Div	VT pixel clock	OP Sys Clk Div	OP pixel Clk Div	OP pixel clock	Line length	Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Integer	Integer	MHz	Pixel Clks	Lines (Dec)
12	2	132	1	6	66	1	8	49.50	1438	1023
24	4	132	1	6	66	1	8	49.50	1438	1023
27	4	117	1	6	65.81	1	8	49.36	1438	1023
45	4	70	1	6	65.63	1	8	49.22	1438	1023
50	8	126	1	6	65.63	1	8	49.22	1438	1023

7 Video system

7.1 Image and video capabilities

The image sensor supports various video modes ranging from full field of view@45 fps to HD video, 720p@60 fps. Example configurations and output interface data rates are given in *Table 35*.

Table 35. Examples of video mode capabilities

Type	Resolution	Max frame rate (fps)	Mode	Format	No. of CSI-2 lanes	Lane datarate (Mbps)	PIX-CLK (MHz)
Full FOV	1304 x 980	45	Full Frame	RAW12	2	396.00	66.00
	1304 x 980	25	Full Frame	RAW12	2	396.00	66.00
HD video	720p	60	Vertical Crop	RAW12	2	396.00	66.00
	720p	30	Vertical Crop	RAW12	2	396.00	66.00
Others	VGA	88	FFOV with 2x2 subsampling	RAW12	2	396.00	66.00
	QVGA	120	FFOV with 4x4 subsampling	RAW12	2	396.00	66.00

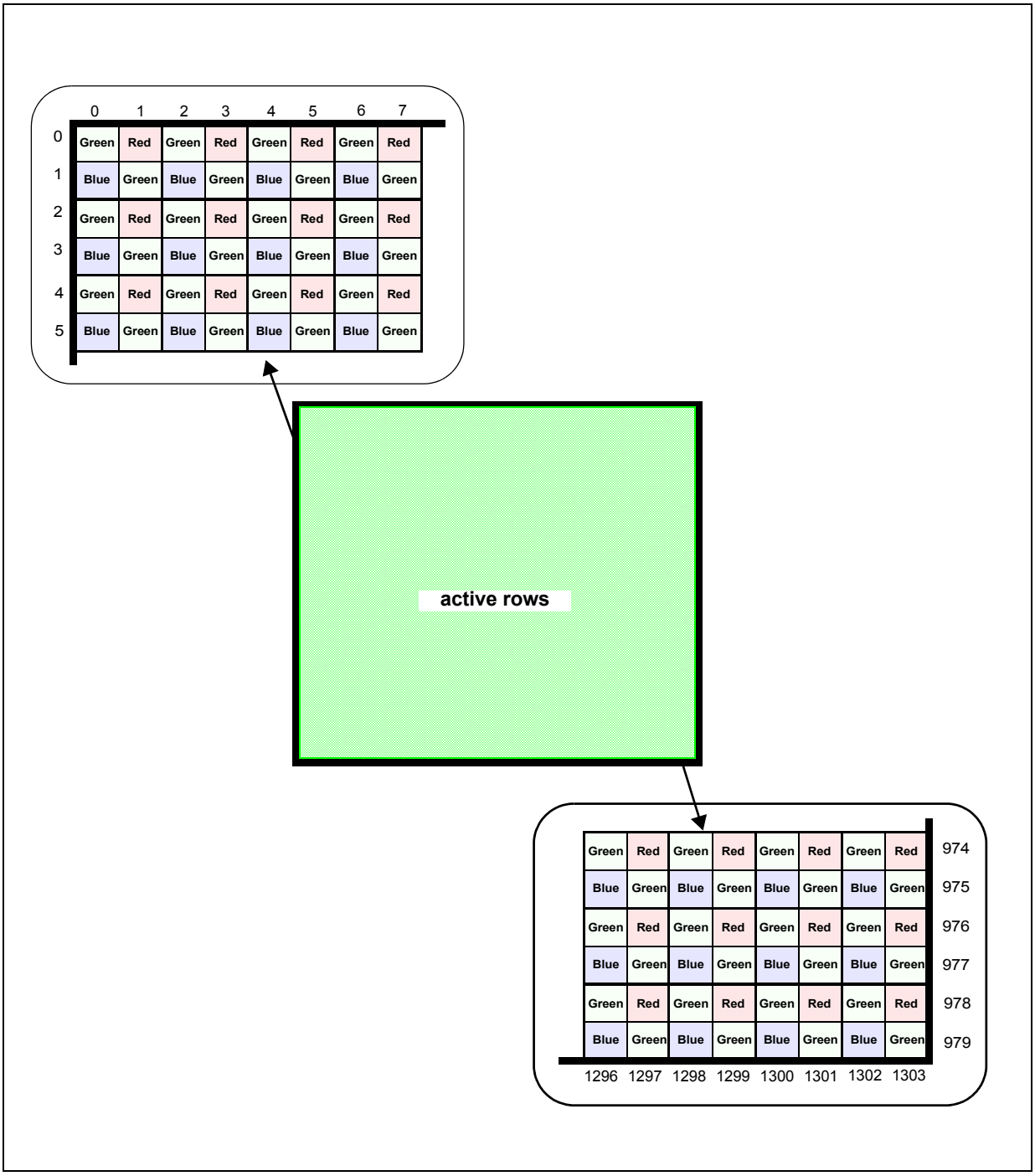
7.2 Bayer pattern

The three color (red, green, and blue) filters are arranged over the pixel array in a repeated 2 x 2 arrangement known as the Bayer pattern. When the sensor array is read, the output order of red, green, blue depends on the settings of vertical flip and horizontal mirror.

Figure 22 shows the read-out order for a sensor of 980 rows by 1304 columns, for the default settings of vertical flip and horizontal mirror (both disabled). Lines are read from left to right, then from top to bottom. Hence the order is green, red, green, red, and so on for the first line, followed by blue, green, blue, green, and so on for the second line.

If vertical flip is enabled, the first line order becomes blue, green, blue, green, and so on. If horizontal mirror is enabled, the first line order becomes red, green, red, green, and so on.

Figure 22. Bayer pattern



1. *Figure 22* valid only for RGB

7.3 Exposure and gain control

The image sensor does not contain any form of automatic exposure control. To produce a correctly exposed image the integration periods, analog gain and digital gain for the pixels must be calculated by an exposure control algorithm implemented externally. The parameters are then written to the image sensor using the control interface.

The exposure control parameters available on the image sensor are:

- long integration time
- medium integration time
- short integration time
- analog gain
- digital gain

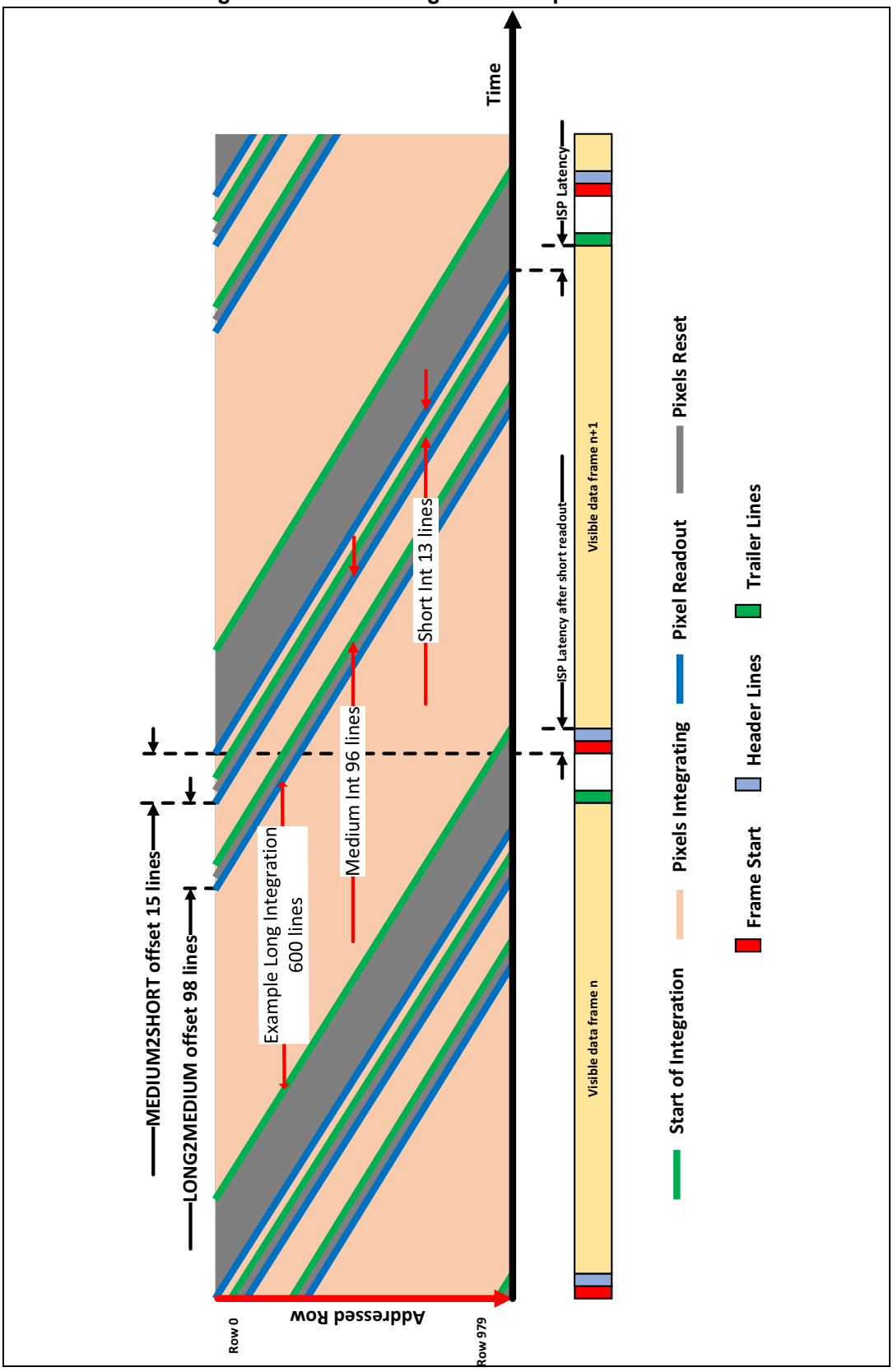
7.3.1 Coarse integration time

The integration time is the amount of time between a row of pixels being reset and when this row is read. The longer the time then the more light that is captured.This sensor supports only Coarse Integration in which the Integration period is measured in integer line times which is derived from the pixel clock.

The sensor provides HDR output by integrating each pixel three times per frame and then merging the data. These exposures comprise a long, medium and short integration time. At the end of the long integration time, the long information is read in a given row, then stored in memory. The read out pixel row is reset, then the medium integration time starts in that row. After the end of the medium integration time, the medium information is read and then also stored in memory. The read out pixel row is then reset again, the short integration time then starts. Finally, the short information is read out of the pixel array. The three data values are then digitally merged within the sensor to give a single output frame.

Figure 23 shows an example of applying a long integration of 600 lines, followed by a medium integration of 96 lines, then a short integration of 13 lines. This diagram shows the point at which pixels are reset, before starting integration, the integration period, then read out. There is a latency between integration starting for the long exposure and the data being output by the device. This latency is dependent on the integration times, fixed offsets and the delay through ISP processing.

Figure 23. Coarse integration and pixel readout.



The dynamic range of the pixels is increased through the capture of three different exposures from each pixel. Only coarse integration times can be set, in multiples of lines.

Table 36. Integration time limits

Exposure	Long Exposure	Medium Exposure	Short Exposure
Variable Name	INT_LONG_LINE	INT_MED_LINE	INT_SHORT_LINE
Purpose	Coarse Long Integration Time in Num of Lines	Coarse Med Integration Time in Num of Lines	Coarse Short Integration Time in Num of Lines
Register Name	course_time_long	course_time_medium	course_time_short
Minimum Value (lines)	0	0	0
Maximum Value (lines)	FRAMELENGTH_LINES - 115	96	13
Other Limits	<= OFFSET_L-2	<= OFFSET_M-2	<= OFFSET_S-2
Fine Exposure (pixel clks)	812	398	398

7.3.2 Analog gain model

The selected analog gain applies to all of the sub-images (Long, Medium and Short). When the Long Exposure is being taken, each pixel is read by two AD Converters simultaneously of which one has a gain of x1 and the other, a gain of x4. These data pipes are referred to as Long1 and Long4. These are merged at the end of the Long Integration period to give a 12bit result and stored while the Medium and Short integrations are performed. This means that the last three analog gain options are outside the normal operating conditions and so, should not be used.

Figure 24 describes the analog gain register (1 byte) for the image sensor.

Figure 24. Analog gain register format

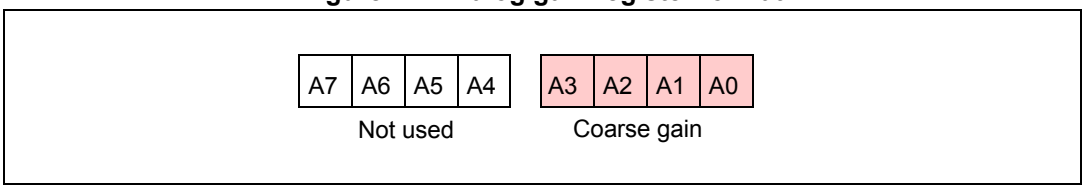


Table 37 specifies the valid analog gain values for the image sensor.

Table 37. Analog gain control

Gain value	Coarse gain code [A3:A0]	Analog gain(L1)	Analog gain(L4)
0x00	0000	0.0 dB (x1.00)	0.0 dB (x4.00)
0x01	0001	0.6 dB (x 1.07)	0.6 dB (x 4.28)
0x02	0010	1.2 dB (x1.1)	1.2 dB (x4.4)
0x03	0011	1.8 dB (x1.2)	1.8 dB (x4.8)
0x04	0100	2.5 dB (x1.3)	2.5 dB (x5.2)
0x05	0101	3.3 dB (x1.5)	3.3 dB (x6.0)
0x06	0110	4.1 dB (x1.6)	4.1 dB (x6.4)

Table 37. Analog gain control (continued)

Gain value	Coarse gain code [A3:A0]	Analog gain(L1)	Analog gain(L4)
0x07	0111	5.0 dB (x1.8)	5.0 dB (x7.2)
0x08	1000	6.0 dB(x2.0)	6.0 dB(x8.0)
0x09	1001	7.2 dB (x2.3)	7.2 dB (x9.2)
0x0A	1010	8.5 dB (x2.7)	8.5 dB (x10.8)
0x0B	1011	10.1 dB (x3.2)	10.1 dB (x12.8)
0x0C	1100	12.0 dB (x4.0)	12.0 dB (x16.0)
0x0D	1011	14.5 dB (x5.3)	14.5 dB (x21.2)
0x0E	1110	18.0 dB (x8.0)	18.0 dB (x32.0)
0x0F	1111	24.0 dB (x16.0)	24.0 dB (x64.0)

7.3.3 Digital gain

To compensate for the relatively coarse analog gain steps and differences in integration times between the short, medium and long frames, the image sensor contains digital multipliers to increase the granularity of the gain system.

The details of the digital gain implementation are listed below.

- One set of white balance digital gain before the merge of the medium- and long integration frames
- One set of digital gain multipliers at the output of the final merge of the short, medium, and long integration frames.

Each set of digital gain multipliers consists of:

- Four individual 16-bit digital channel gains (one per Bayer channel)
  - digital_gain_greenR
  - digital_gain_red
  - digital_gain_blue
  - digital_gain_greenB
- The digital gain range for each channel is 0.000 to 255.9961 in steps of 0.0039 (1/256), i.e. 8 integer bits and 8 fractional bits
  - digital_gain_min = 0x0000 (0.000)
  - digital_gain_max = 0xFFFF (255.9961)

Note: Text refers only to RGB

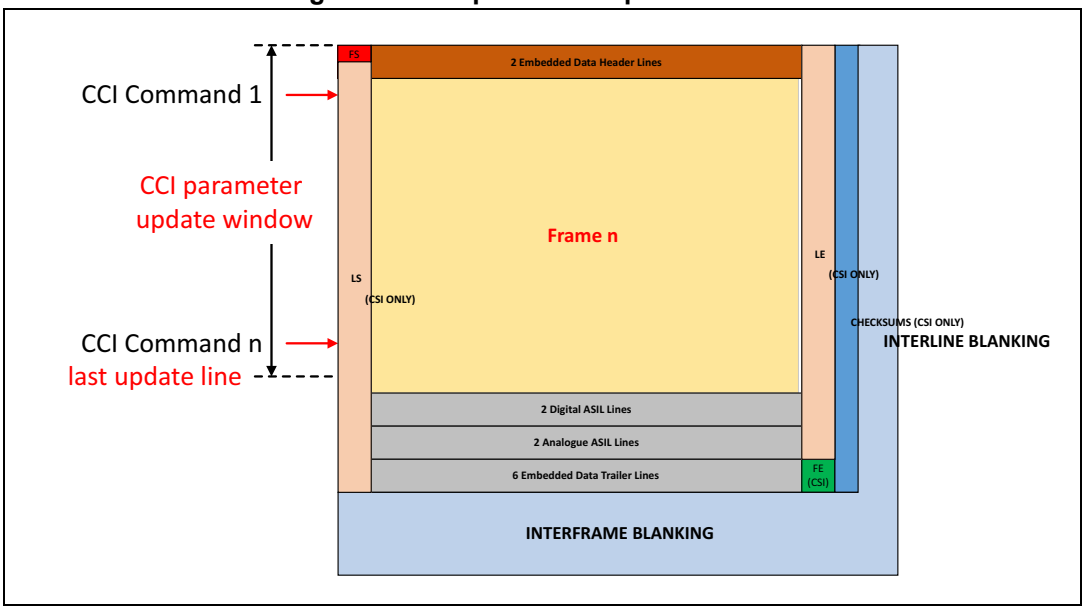
7.3.4 Pixel gain

The imaging sensor has a feature whereby the readout pixels can be operated in two different conversion gain modes. In low-light conditions, a high conversion gain can be used to improve sensitivity. In high-light conditions, a low conversion gain is selected to improve signal SNR. The gain modes are set in the pixel_gain register (0x212c). Typically the highgain / lowgain ratio will be approximately 5.8

7.3.5 Integration and gain parameter re-timing

Due to the triple exposure architecture and various latencies the period in the frame where a specific register can be set to be consumed before the next frame starts is as shown in *Figure 25*

Figure 25. CCI parameter update window

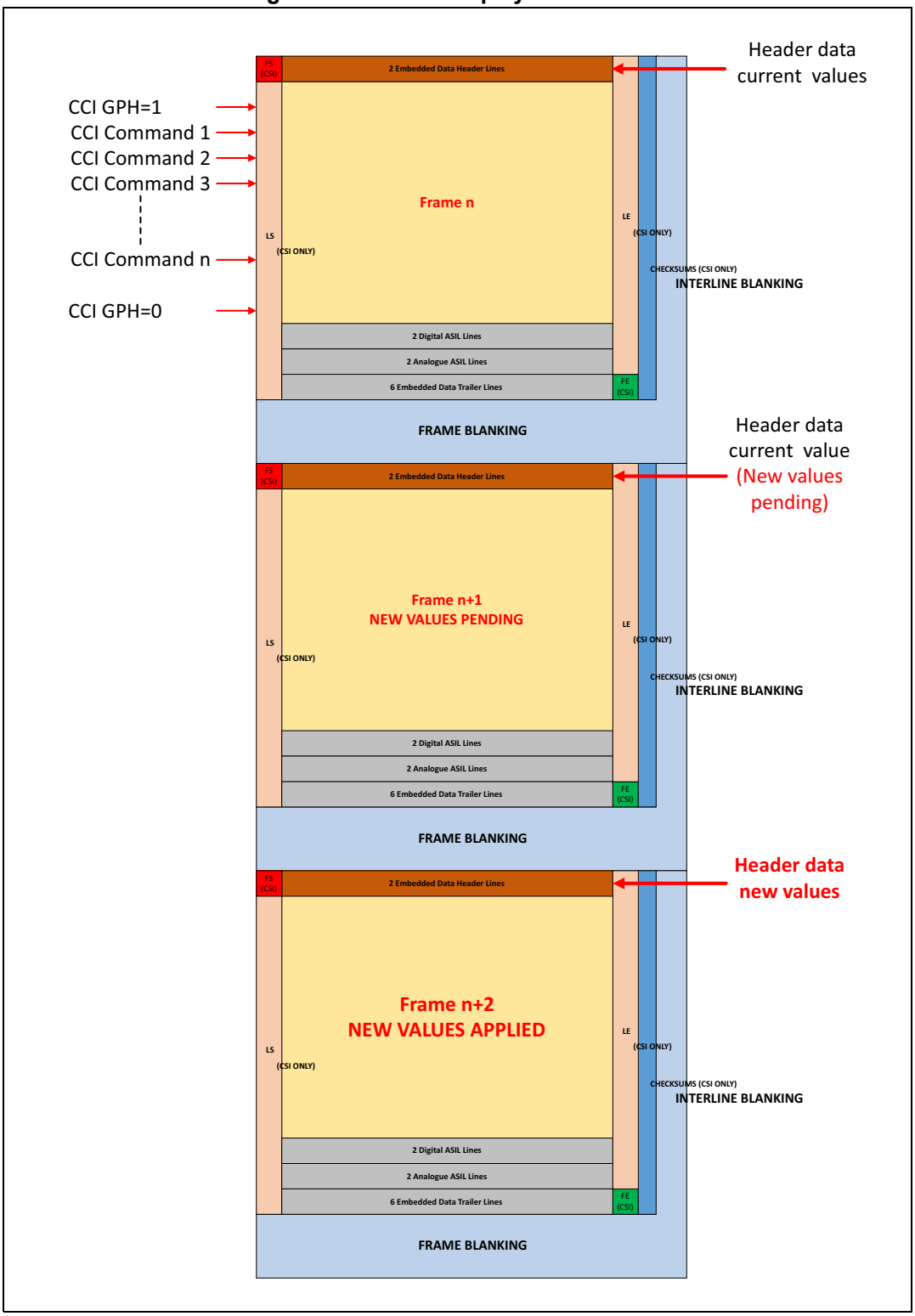


The last moment to update registers so that they will apply to next frame integration tracks with the start of the next frame: 113 lines to end of current frame + 46 lines inter frame = 159 lines to before the start of next frame. If you increase the inter frame, then the moment remains defined as: 159 lines before the start of the next frame.

7.3.6 Grouped register settings

If a large number of registers are required to be set in a single frame, due to the timing of the CCI commands some transactions may be consumed in the immediate frame, the remainder in the next frame. To avoid this problem, bit 0 of the Grouped_Parameter_Hold (0x0104) register should be used to inhibit the application of new register values until the complete set of new values have been written to the sensor. Bit 0 should be set to 1, registers written, then the bit cleared. This will ensure that all registers are consumed at the same time. An example of the multiple CCI grouped writes is shown in *Figure 26*.

Figure 26. Control loop synchronisation



8 Test pattern generation

The VG6640 sensor contains a test pattern generator that can inject deterministic test patterns into the pixel data path. The test patterns are injected independently into the long, medium and short exposure data paths before they are merged together. Because of this the test patterns can be used to test the correctness of the entire video system on the VG6640. However, it also means that the video pipe of the VG6640 must be correctly configured to give the expected output of the test patterns.

The test pattern generator block can operate in one of three modes, determined by the TestPatternMode field of the TestPatternControl register

a) Standard mode. Full frame test pattern determined by the TestPatternSelect field.

b) Digital ASIL mode. HDR ramp outputted on the digital ASIL lines that immediately follow the active image lines. This is the default mode for VG6640.

c) HDR ramp mode. A hdr grey scale ramp is outputted across a programmable number of lines of the image. Ramp characteristics are determined by the settings in the “HDRPattern_xxxxxxx” registers.

Note: Changes to the TestPatternControl register only take affect during a transition from STANDBY to STREAMING state.

8.1 Standard mode patterns

The selection of the test pattern type is done with the TestPatternSelect field of the TestPatternControl register. Test patterns available are as follows.

Table 38. Test pattern types

TestPatternSelect	Name	Description
0	None	No test pattern outputted.
1	Solid color	Solid color. Programmable value for Bayer pixels on long, medium and short data paths.
2	100% color bars	Color bar pattern (see *Section 8.1.1*)
3	Fade to grey color bars	Color bars that fade to grey towards the bottom of image (see *Section 8.1.2*).
16	Horizontal grey scale	Horizontal grey scale ramp across the image.
17	Vertical grey scale	Vertical grey scale ramp down the image.
18	Diagonal grey scale	Diagonal grey scale ramp.
19	PN28 pseudo-random	Pseudo-random series of pixel values.
20	Smearing test	Injects a rectangular area of solid color pixels while passing through normal image pixels for the rest of the image.

8.1.1 100% color bars pattern mode

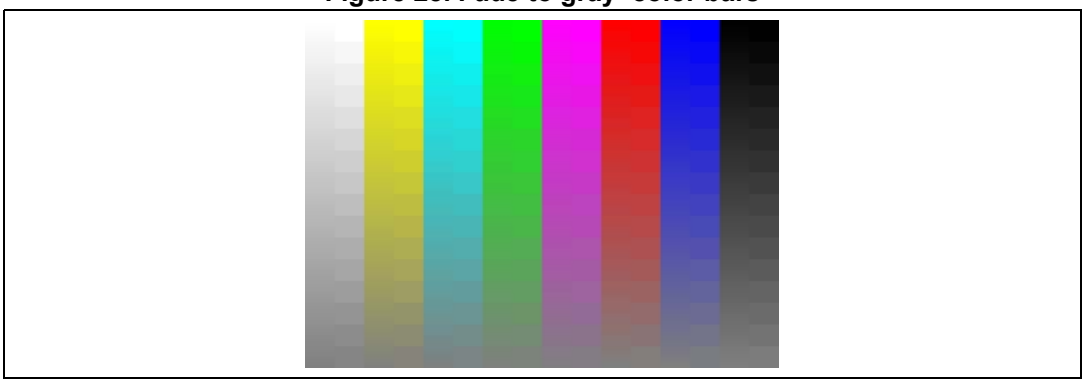
In the ‘100% color bar’ test pattern mode, all pixel data is replaced with a Bayer version of an 8-bar color bar pattern. In each bar all pixels are either 0% or 100% full scale.

Figure 27. 100% color bars

8.1.2 ‘Fade to gray’ color bar mode

In the ‘fade to gray’ color bar test pattern mode, all pixel data is replaced with a color bar that fades vertically from 100% color bars to mid gray. The ‘fade to gray’ color bar pattern is designed to exercise more of the color space than 100% bars. *Figure 28*gives an indication of the pattern (although the pattern is generated as Bayer data).

Figure 28. Fade to gray’ color bars



The pattern is made up of eight vertical bars that fade vertically from one of the 100% color bar colors towards a mid-gray at the bottom. The bars follow the same order as standard color bars. Each of the bars is sub-divided vertically into a left hand side that contains a smooth gradient and a right hand side that contains a quantized version.

The aim of the quantized portion is to offer areas of flat-field Bayer data that should be large enough to result in known data values even after demosiac (independently of the demosiac algorithm). To ensure maximum dynamic range in the quantized data, the LSBs of the quantized data are generated by copying the MSBs of the unquantized data (rather than forcing them to 0). The pattern repeats after 256 lines.

9 Electrical characteristics

9.1 Parameter classification

The electrical parameters shown in this datasheet are guaranteed by various methods. To give the customer a better understanding, the classifications listed *Table 39* are used and the parameters are tagged accordingly in the tables.

Table 39. Parameter classification

Classification (C)	Tag description
PA	These parameters are guaranteed during production testing on individual devices - automotive grade order codes only.
P	These parameters are guaranteed during production testing on individual devices - all order codes.
C	These parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	These parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.
D	These parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables.

9.2 Absolute maximum ratings

Table 40. Absolute maximum ratings

Symbol	C	Parameter	Minimum	Maximum.	Unit
V_{CORE}	D	Digital core power supply	-0.3	1.32	V
V_{DIG}	D	Digital I/O power supply	-0.3	3.3	V
V_{ANA}	D	Analog power supply	-0.3	3.2	V
V_{IP}	D	Digital input voltage(1)	-0.3	3.3	V
T_{STO}	D	Storage temperature	-40	+125(2)	°C
V_{ESD}	D	Electrostatic discharge model(3) Human body model (HBM) Charge device model (CDM) Machine model (MM)	 -2.0 -500 -100	 2.0 500 100	 kV V V

1. Digital input: EXTCLK_XTAL1, EXTCLK_EN, XSHUTDOWN, RESET_N, FSYNC_IN, GPIO, SCL, SDA.
2. This is a maximum long term standard storage temperature, see soldering profile for short term high temperature tolerance.
3. ESD tests are performed in compliance with AEC-Q100ESD Grade 2.

Caution: Stresses above those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.3 Operating conditions

Table 41. Operating conditions

Symbol	C	Parameter	Minimum	Typical	Maximum	Unit
V_{CORE}	C	Digital core power supply	1.08	1.2	1.32	V
V_{DIG}	C	Digital I/O power supply	1.62	1.8	1.92	V
V_{ANA}	C	Analog power supply	2.66	2.8	2.94	V
V_{IP}	C	Digital input voltage(1)	-0.3		2.3	V
T_{JF}	C	Junction temperature (operating functionally)	-40		+125	°C
T_{JN}	PA	Junction temperature (operating normally and producing acceptable images)	-40		+105	°C
T_{AO}	T	Ambient temperature (operating optimally)	+5		+40	°C
T_{ATR}	PA	Ambient room temperature during test(2)	+20		+30	°C
T_{ATH}	PA	Ambient high temperature during wafer test(3)	+103	+105		°C
	P	Ambient high temperature during wafer test(3)	+58	+60		
T_{ATL}	PA	Ambient low temperature during wafer test(3)	-40		-38	°C
θ_{JA-F}	D	Junction to ambient thermal resistance for device attached to a PCB in free air		50		°C/W
θ_{JA-H}	D	Junction to ambient thermal resistance for device attached to a PCB on an infinite heatsink		23		°C/W

1. Digital input: EXTCLK_XTAL1, EXTCLK_EN, XSHUTDOWN, RESET_N, FSYNC_IN, GPIO, SCL, SDA.
2. 100% tested parameters are measured at this temperature.
3. A subset of parameters are measured at this temperature.

9.4 Average current consumption

Table 42. Typical current consumption in reset and standby

Conditions[1]	Reset	Reset	Standby[2]	Standby[2]
C	C	C	C	C
VCORE source	Internal	External	Internal	External
VCORE	3.5 mA	5 µA	NA	4.1 mA
VDIG	5 uA	5 uA	5 mA	0 mA
VANA	5 uA	5 uA	0.3 mA	0.3 mA

1. VDIG=1.8V, 12MHz external clock, tested at 25C junction temperature
2. In the case when the CSI-2 interface is used and the sensor has returned to STANDBY, after having previously been in STREAMING state, then VANA current will be higher than stated here as it is used to maintain the LP11 CSI-2 bus state.

Table 43. Typical current consumption while streaming

	Mode 1	Mode 2	Mode 3	Mode 4	Mode5
Conditions[1]	**Worst case**	**Standard**	**Low power**	**Night mode**	**Very low power**
C	C	C	C	C	C
Resolution	1304x980	1280x960	1280x960	1280x960	1280x720
Frame rate (fps)	45	45	30	15 (by frame extension)	15
Pixel Clk (MHz)	66	66	44	44	16.5
Output interface	ITU Parallel	DL-CSI2	DL-CSI2	DL-CSI2	DL-CSI2
Scene	n.a.	n.a.	Test Chart	Dark image	Dark image
Image source	PN28 Random	HDR Test Pattern	HDR Test Pattern	Long12 Image	Long12 Image
VCORE source	Internal	Internal	External	External	External
VCORE (mA)	NA	NA	75	75	40
VDIG (mA)	180	120	4	4	4
VANA (mA)	100	110	100	100	100

1. Mode 1 VDIG = 2.8 V, 12 MHz external clock, tested at 25 °C junction temperature
Modes 2, 3, 4, and 5 VDIG = 1.8 V, 12 MHz external clock, tested at 25 °C junction temperature

Table 44. Maximum current consumption while streaming

	Mode 1	Mode 2	Mode 3	Mode 4	Mode5
Conditions(1)	**Worst case**	**Standard**	**Low power**	**Night mode**	**Very low power**
C	C	C	C	C	C
VCORE (mA)	NA	NA	90	90	75
VDIG (mA)	200	150	4	4	4
VANA (mA)	140	150	140	140	140

1. Mode 1 VDIG = 2.8 V, 12 MHz external clock, tested at 25 °C junction temperature
Modes 2, 3, 4, and 5 VDIG = 1.8 V, 12 MHz external clock, tested at 25 °C junction temperature

9.5 System clock

Table 45. EXTCLK_XTAL1 - characteristics

Symbol	C	Parameter	Minimum	Maximum	Unit
$V_{EXTCLKL}$	T	DC-coupled square wave low level input	-0.5	0.5	V
$V_{EXTCLKH}$	T	DC-coupled square wave high level input	1.3	2.3	V
f_{EXTCLK}	T	Clock frequency input	12	50	MHz
$I_{EXTCLKL}$	P	Input leakage current(1)		10	µA

1. For $V_{GND} \leq V_{EXTCLK} \leq V_{DIG}$

Table 46. System clock - crystal

Symbol	C	Parameter	Minimum	Maximum	Unit
f_{XTAL}		Crystal resonant frequency	12(tbc)	27(tbc)	MHz

Table 47. PLL timing characterics

Symbol	C	Parameter	Minimum	Maximum	Unit
$f_{PLLINPUT}$	P	PLL input frequency (after internal pre-divider)	6	12	MHz
t_{JITTER}	T	Maximum allowable clock jitter on input to PLL		100	ps
$f_{PLLOUTPUT}$	C	PLL output frequency (after fixed divide by 2)	225	500	MHz

9.6 Reset input

The RESET input signal has the following characteristics.

Table 48. RESET input - timing characteristics

Symbol	C	Parameter	Minimum	Maximum	Unit
t_{RL}	C	RESET low time (EXTCLK_XTAL1 clock periods)	4		clock periods

9.7 Digital inputs

The digital input signals include XSHUTDOWN, RESET_N, EXTCLK_EN, FSYNC_IN, GPIO, JTAG_TMS, JTAG_TCK, JTAG_TDI

Table 49. Digital input - signal characteristics

Symbol	C	Parameter	Minimum	Maximum	Unit
V_{IL}	C	Low level input voltage	-0.5	0.5	V
V_{IH}	C	High level input voltage	1.3	2.3	V
I_{IL}	P	Input leakage current(1)		10	µA

1. For $V_{GND} \leq V_I \leq V_{DIG}$

9.8 Digital outputs

The digital output signals include FSYNC_OUT, ECC_OUT, JTAG_TDO and GPIO

Table 50. Digital output - signal characteristics

Symbol	C	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	C	Output low level	$-I_{OL}$ = 4 mA			0.15	V
V_{OH}	C	Output high level	I_{OH} = 4 mA	1.65			V
I_{max}	C	Maximum current				4	mA

9.9 I²C interface - SDA, SCL

Table 51. I²C interface - signal characteristics

Symbol	C	Parameter	Minimum	Typical	Maximum	Unit
V_{SL}	T	Low level input voltage (SDA, SCL)	-0.5		0.5	V
V_{SH}	T	High level input voltage (SDA, SCL)	1.3		2.3	V
C_O	T	Capacitive load on SCL or SDA			550	pF
I_{SL}	P	Input leakage current(1) (SDA, SCL)	-10		10	µA
I_{SDAF}	D	SDA output sink current (Fast mode)			4	mA
I_{SDAFP}	D	SDA output sink current (Fast+ mode)			20	mA
V_{OL}	T	SDA output voltage low level (Fast+ mode, 20mA, VDIG=1.8V)			0.4	V
V_{OL}	T	SDA output voltage low level (Fast+ mode, 20mA, VDIG=2.8V)			0.4	V

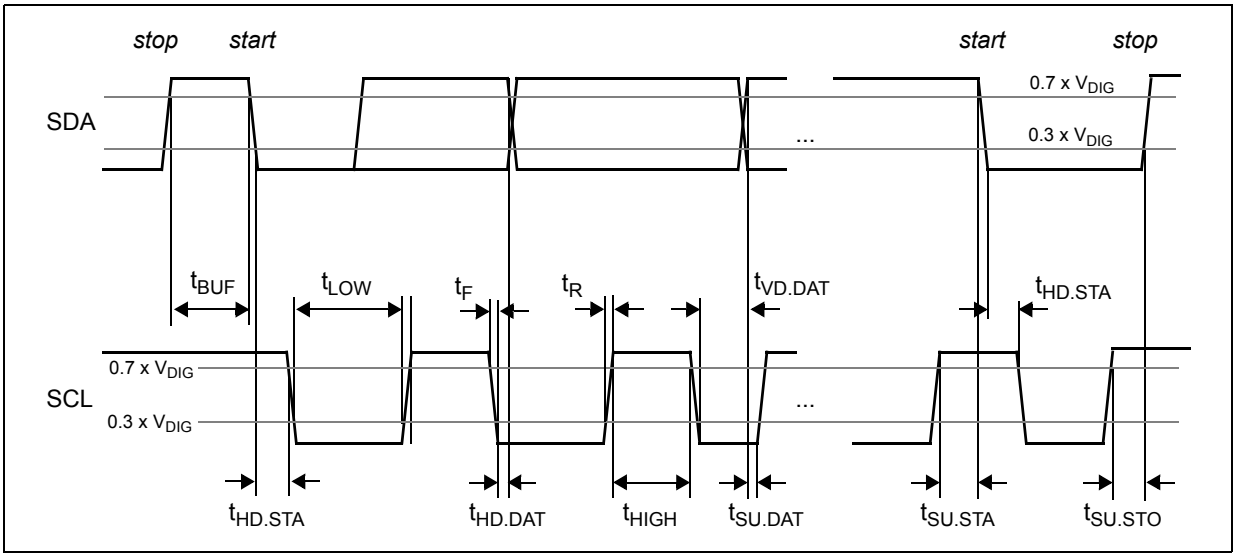
1. For $0.1 \times V_{DIG} \leq V_{SL} \leq 0.9 \times V_{DIG}$

Table 52. I²C interface - timing characteristics

Symbol	C	Parameter	Minimum	Typical	Maximum	Unit
t_{SCL}	T	SCL clock frequency			1000(1)	kHz
t_{LOW}	T	Clock pulse width low	0.5			µs
t_{HIGH}	T	Clock pulse width high	0.26			µs
t_{SP}	T	Pulse width of spikes which are suppressed by the input filter	0		50	ns
t_{BUF}	T	Bus free time between transmissions	0.5			µs
$t_{HD.STA}$	T	Start hold time	0.26			µs
$t_{SU.STA}$	T	Start set-up time	0.26			µs
$t_{SU.DAT}$	T	Data in set-up time	50			ns
$t_{HD.DAT}$	T	Data in hold time	16			ns
$t_{VD.DAT}$	T	Data out valid time			0.45	µs
t_R	T	SCL/SDA rise time			120	ns
t_F	T	SCL/SDA fall time			120	ns
$t_{SU.STO}$		Stop set-up time	0.26			µs

1. To achieve the maximum 1MHz SCL rate on a bus with worst case capacitance it is required that the EXTCLK_XTAL1 input is driven with a clock of at least 19MHz frequency.

Figure 29. I²C interface timing



All timings are measured from either 0.3 x V_{DIG} or 0.7 x V_{DIG}. For further information on the I²C interface refer to the specification document: *SMIA 1.0 part 2: CCP Specification*.

9.10 CSI-2[(b)] interface

Table 53. CSI-2 interface - high speed mode - signal characteristics

Symbol	C	Parameter	Minimum	Typical	Maximum	Unit
V_{CMTX}	T	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	T	HS transmit differential voltage[(1)]	140	200	270	mV
V_{OHHS}	T	HS output high voltage[(1)]			360	mV
Z_{OS}	T	Single ended output impedance	40	50	62.5	Ω

1. Value when driving into load impedance anywhere in the Z_{ID} range (80-125Ω).

Table 54. CSI-2 interface - low power mode - signal characteristics

Symbol	C	Parameter	Minimum	Typical	Maximum	Unit
V_{OH}	T	Output high level	1.1	1.2	1.3	V
V_{OL}	T	Output low level	-50		50	mV
Z_{OLP}	T	Output impedance of LP transmitter	110			Ω

Table 55. CSI-2 interface - high speed mode - timing characteristics

Symbol	C	Parameter	Minimum	Typical	Maximum	Unit
R_T	T	Total data rate	80		792	Mbit/s
R_{LN}	T	Data rate per lane	80		396	Mbit/s
t_{clkp}	T	Average data period	1.25			ns
t_r and t_f	T	20% - 80% rise time and fall time	100		0.3UI[(1)]	ps
t_{skew}	T	Data to clock skew	-0.15UI		0.15UI	ps

1. UI is equal to 1/(2*fh) where fh is the fundamental frequency of the transmission for a certain bit rate, for example, for 600 Mbit/s fh is 300 MHz.

Table 56. CSI-2 interface - low power mode - timing characteristics

Symbol	C	Parameter	Minimum	Typical	Maximum	Unit
t_r and t_f	T	15% - 85% rise time and fall time			25	ns

For further information on the physical layer of the CSI-2 interface refer to the specification document: *MIPI Alliance Standard for D_PHY version 1.1*.

b. Copyright © 2007 MIPI Alliance Inc.

9.11 Parallel (ITU) interface

Table 57. Parallel interface - signal characteristics

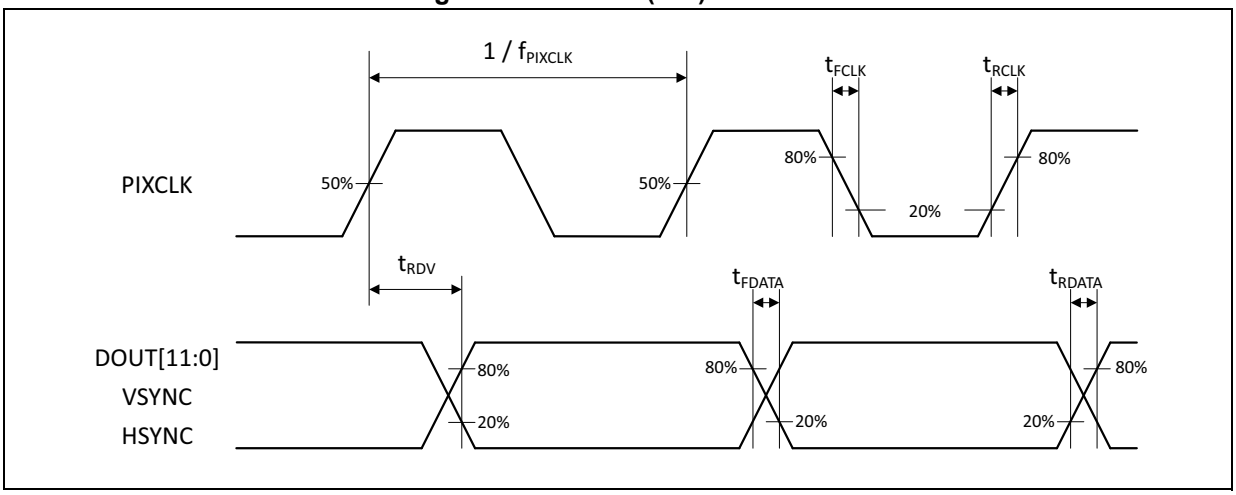
Symbol	C	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OL}	C	Output low level	$-I_{OL}$ = 4 mA			0.15	V
V_{OH}	C	Output high level	I_{OH} = 4 mA	1.65			V

Table 58. Parallel interface - timing characteristics

Symbol	C	Parameter	Conditions		Minimum	Typical	Maximum	Unit
f_{PIXCLK}	T	PIXCLK frequency	Load capacitance C_L = 15pF				66.5	MHz
D_{PIXCLK}	T	PIXCLK duty cycle			43	50	58	%
t_{RCLK}	T	PIXCLK rise time (20 - 80%)				1.3	2.0	ns
t_{FCLK}	T	PIXCLK fall time (80 - 20%)				1.2	1.7	ns
t_{RDATA}	T	DOUT[11:0], VSYNC, HSYNC rising (20 - 80%)		Normal drive(1)		2	3.1	ns
	T			Low drive		2.5	3.8	ns
t_{FDATA}	T	DOUT[11:0], VSYNC, HSYNC falling (80 - 20%)		Normal drive		2	3.1	ns
	T			Low drive		2.5	3.6	
t_{RDV}	T	PIX-CLK rising (50%) to output data valid (20% or 80%)		Normal drive	1.4	4.6	9.0	ns
				Low drive	2.1	6.3	11.5	

1. Normal drive and low drive modes are selected by writing to register ParOutIF_Drive (0x24A2).

Figure 30. Parallel (ITU) interface



10 Electro-optical characteristics

Note: The same parameter classification as described in Chapter 9.1: Parameter classification is used to classify the electro-optical characteristics.

10.1 Array characteristics

Table 59. Electro-optical characteristics

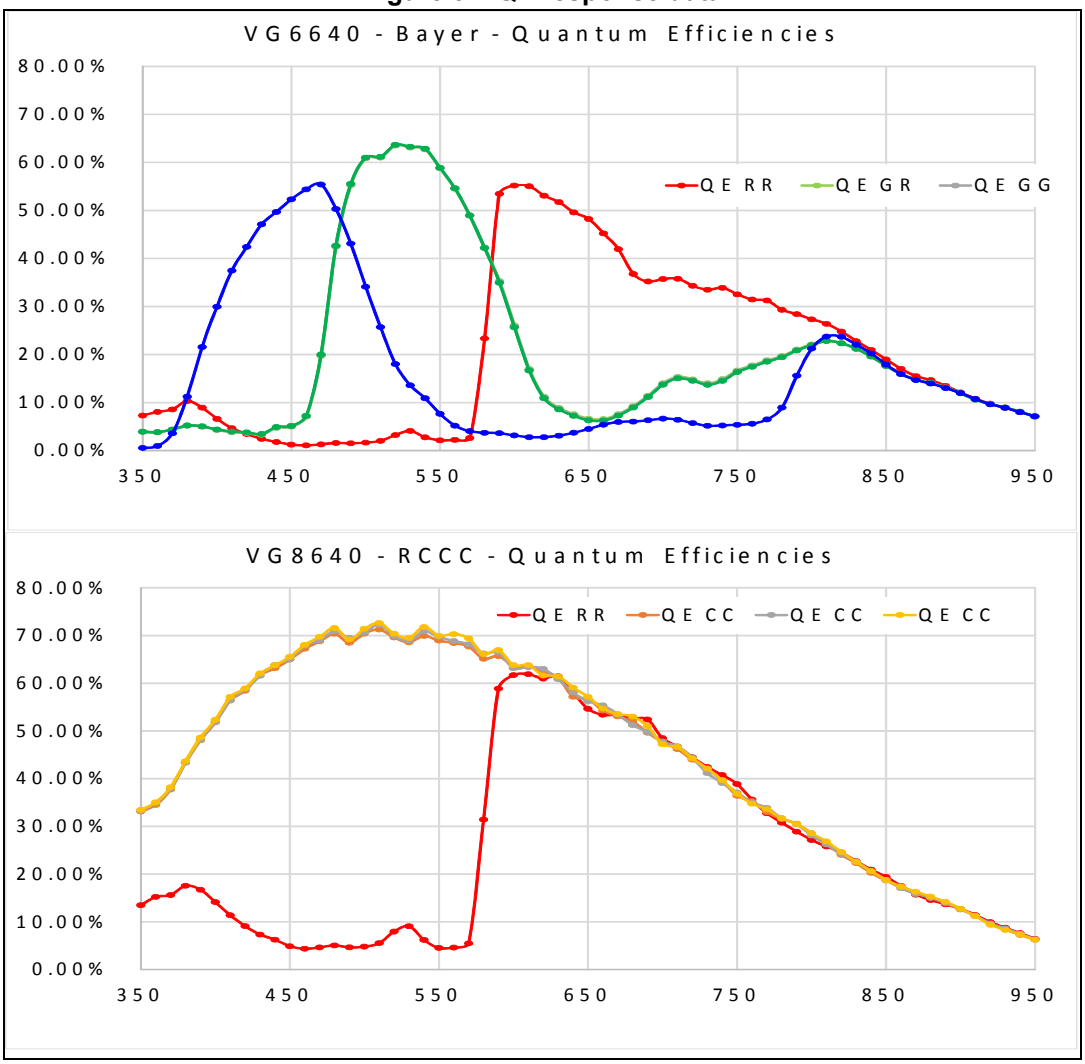
Characteristic	C	Value
Pixel sensitivity (without colour filter)	D	>=32V/lxsec @3200K
Minimum illumination on pixel (no color filter, 30ms integration time, 5000K color temperature)	T	1.0 mlux @ SNR 1
Dynamic range (linear mode)	T	72 dB
Dynamic range (in scene)	T	132 dB
Peak signal to noise ratio (on pixel, Low CG)	T	42 dB @ 12 lux
Peak quantum efficiency	T	>=60% @ 520 nm
NIR cut-off wavelength(1)	T	>=10% QE @ <900 nm
Fixed pattern noise (FPN)	T	<0.01% @ 20°C
Temporal read noise	T	<0.025% @ full swing
Image lag (10Ke signal)	T	<0.1%

1. NIR cut-off data is only valid for parts that do not have AR (anti-reflective) coating. By default all parts delivered will have an AR coating on the cover glass. For samples without AR coating please contact your local STMicroelectronics sales representative.

10.2 Quantum efficiency

Below is the typical spectral response of the packaged VG6640.

Figure 31. QE response data



11 Application

11.1 Schematics

11.1.1 Example ethernet camera application

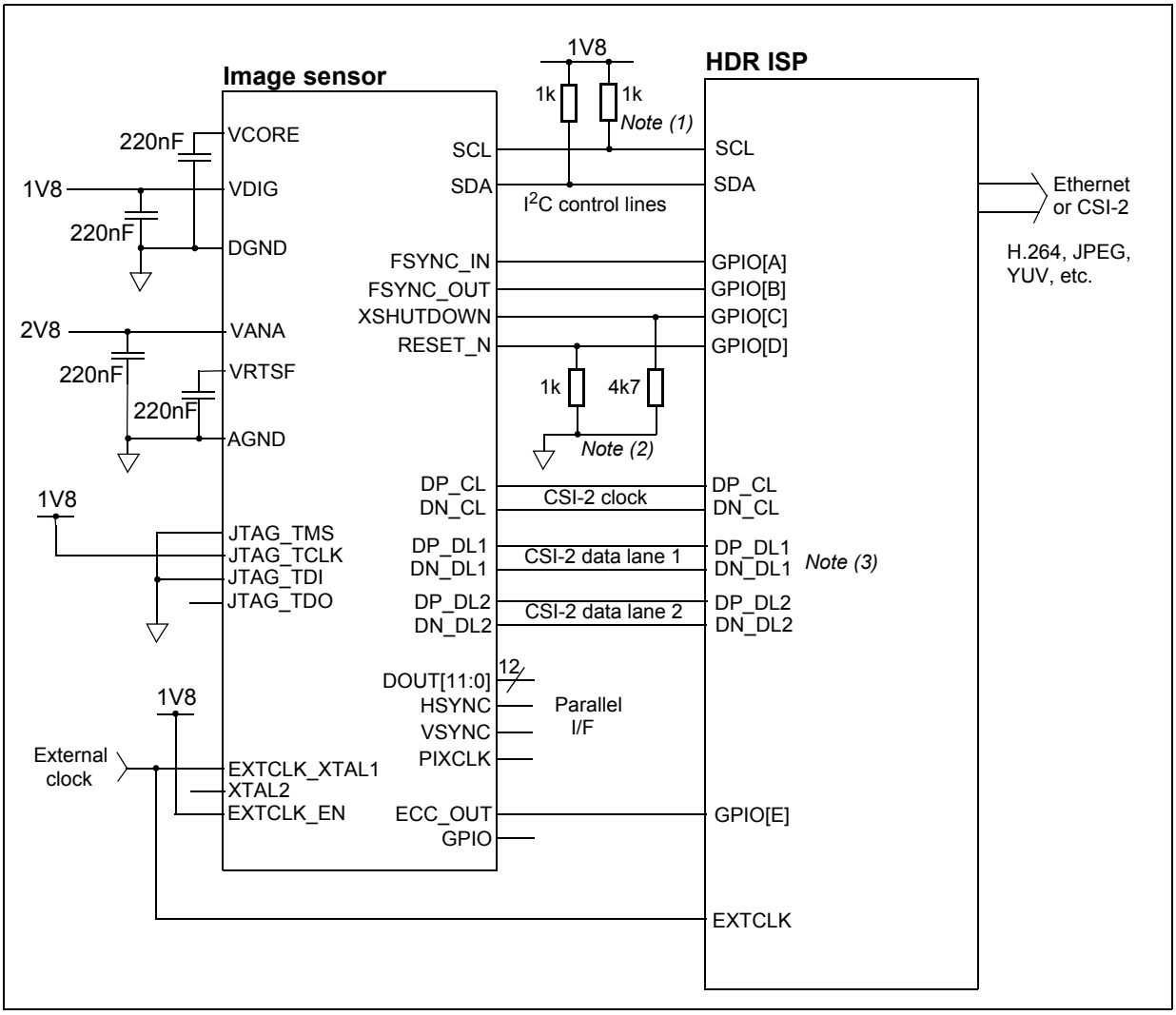
The image sensor can be used in conjunction with an high dynamic range (HDR) imaging system processor (ISP) as shown in *Figure 32*. This combination allows exceptionally high quality images to be streamed over an Ethernet or CSI-2 interface. A range of output formats (for example, H.264, JPEG, YUV) is possible.

In this example the image sensor is shown:

- sharing an external clock source with the HDR ISP;
- with the HDR ISP handling its synchronization, allowing this camera system to synchronize with other similar camera systems in the final application;
- with VCORE generated internally using the internal LDO regulator;
- with 1V8 I/O interfaces;
- using the CSI2 output interface (the parallel output interface is in a high-impedance state).

Note: The settings described above are for example only, other settings may be used in an Ethernet camera application.

Figure 32. Example ethernet camera application



1. Not required if the companion device contains its own I²C pull-up resistors. Values depend on bus speed and capacitance See *Section 11.5: I2C pull-up resistors*
2. Pull-down resistors are required to hold the sensor inputs at the correct state during companion device reset.
3. It is assumed in this schematic that the companion device contains internal termination resistors for CSI2.

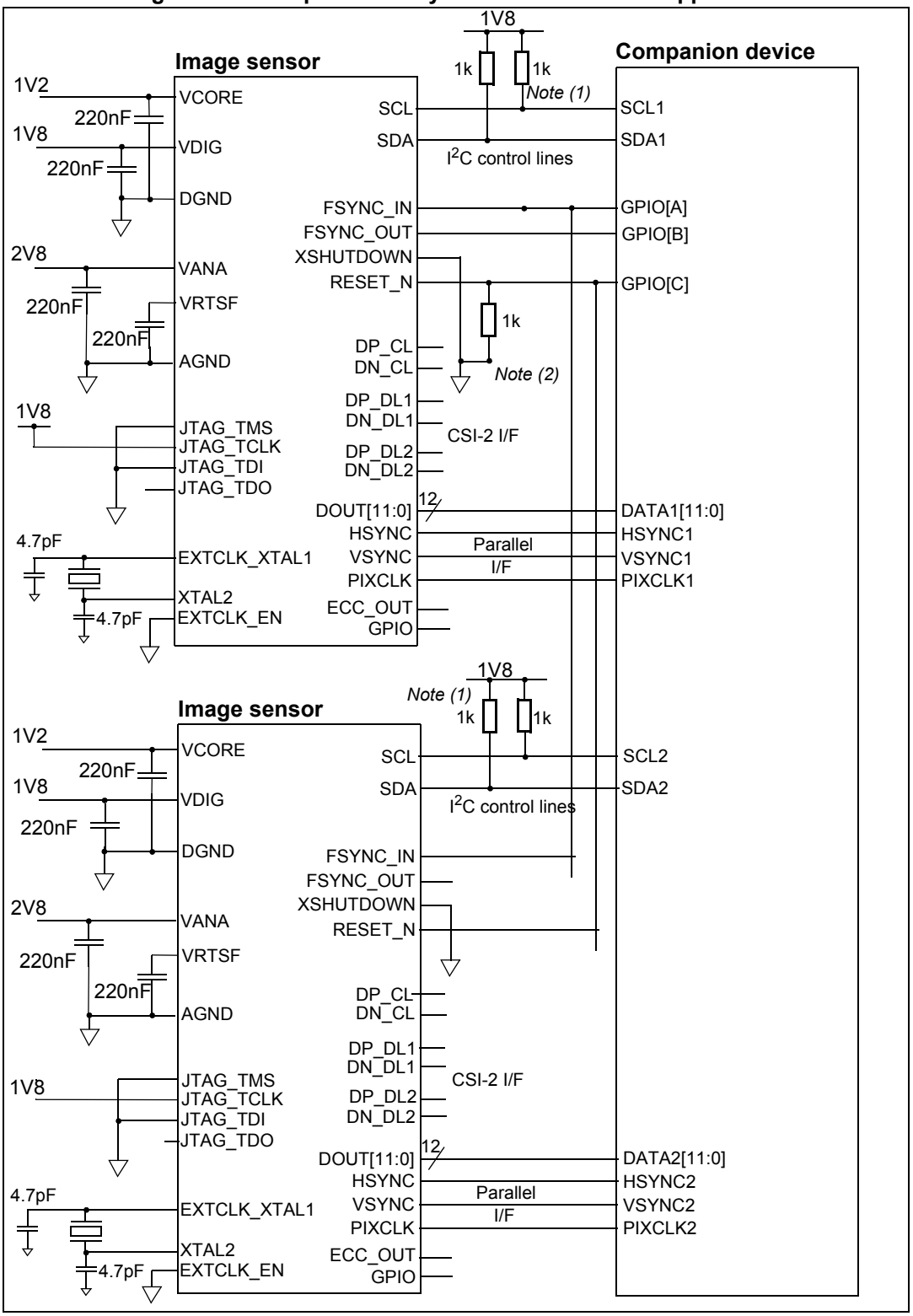
11.1.2 Example stereo synchronized cameras application

Figure 33 shows two synchronized image sensors used in conjunction with a companion device. In this example the image sensors are shown:

- clocked by its own crystal;
- with the companion device handling a common synchronization of both image sensors;
- with VCORE supplied externally;
- using the parallel (ITU) output interface (the CSI2 output interface is in a high-impedance state).

Note: The settings described above are for example only, other settings may be used in a Stereo synchronized cameras application.

Figure 33. Example stereo synchronized cameras application



1. Values depend on bus speed and capacitance See *Section 11.5: I2C pull-up resistors*
2. Pull-down resistors are required to hold the sensor inputs at the correct state during companion device reset.

11.2 PCB layout guidelines

Normal good PCB design practice should be observed for the layout of the image sensor:

- Power and ground planes should be used to supply power to image sensor.
- Join both grounds, AGND and DGND into one, single, solid GND plane underneath the sensor.
- Connect this GND plane to sensor balls with one via per GND-ball.
- To limit the number of interruptions of this GND plane fan out the non-GND and non-supply pads laterally on the top side of the PCB.
- External decoupling capacitors must be added to all four supply voltages, with values of:
  - 1 x 220nF between VDIG and DGND;
  - 1 x 220nF between VANA and DGND,
  - 1 x 220nF between VCORE and DGND,
  - 1 x 220nF between VRTSF and AGND.
- The decoupling caps for the supplies must be placed on the bottom side of the PCB, as close as possible to the supply balls.
- Connect the supply balls on top with the decoupling caps on bottom taking care to ensure.
  - The lowest possible impedance.
  - At least one via for every supply ball.
- To minimize risk of emissions, shield all the Vias and tracks attached to these supplies by their respective GND nets.
- The high speed signal pairs (CLOCK+, CLOCK-), (DP_DL1, DN_DL1), and (DP_DL2, DN_DL2) should be routed as balanced transmission lines with a characteristic differential impedance (Z_{odiff}) of between 80Ω to 120Ω. The two traces in the signal pair should be routed together and should be matched in length to within ±1 mm. The related clock and data pairs should be matched in length to within ±4 mm.
- The VANA supply is very sensitive to noise and therefore care should be taken when designing the 2V8 power supply. The noise level on VANA should be kept below $1mV_{rms}$. For designs with a very noisy 2V8 supply, a filtering scheme (for example, Π-type filter and/or linear regulator) should be considered.
- Quartz crystal - special care should be taken during layout to control the parasitic capacitances associated with the crystal. Refer to *Section 11.4.2: Quartz crystal*
- Maximise copper fill on power planes near the sensor and use vias to improve heat transfer from the sensor. Consider including heatsinking close to the sensor if it is to be used at high temperatures.

11.3 Power management

11.3.1 Power-up procedure

The digital and analog supply voltages can be powered up in any order.

If VCORE is supplied externally, XSHUTDOWN must remain LO to disable the internal 1V2 regulator.

The EXTCLK clock can either be initially low and then enabled during reset or EXTCLK can be a free running clock.

On power-up, the host must issue a reset to ensure that the register values are initialized correctly to their default values.

Table 60. Power-up sequence timing constraints

Symbol	C	Parameter	Minimum	Maximum	Units
t0		VANA rising to VDIG rising	VANA and VDIG may rise in any order, the rising edge separation can vary from 0 ns to indefinite		
t1		VDIG rising to VANA rising			
t2		VANA/VDIG to RESET_N rising	RESET_N must not rise before both power supplies (VDIG and VANA) are stable (to within ±5%)		
t3	C	XSHUTDOWN to RESET_N rising	1		ms
t4	C	RESET_N to first I^2C transaction	247000		clock periods
t5	C	EXTCLK_XTAL1(1) to RESET_N rising	4		clock periods
t6	C	Issuing the streaming mode command to first frame start sequence(2)		10 + coarse integration time	ms
t7	C	VDIG - External 1.2V rising(3)	100		us

1. When using an external clock. Not valid when using an external crystal.
2. Dependent on the image sensor clock frequency and the coarse exposure setting. A fast clock speed and zero exposure will result in the shortest startup time.
3. If the 1.2V rises before VDIG then it pulls up VDIG through a substrate diodein the on-chip VCORE regulator.

Figure 34. Power-up sequence with internal 1.2V regulator in MIPI CSI-2 mode

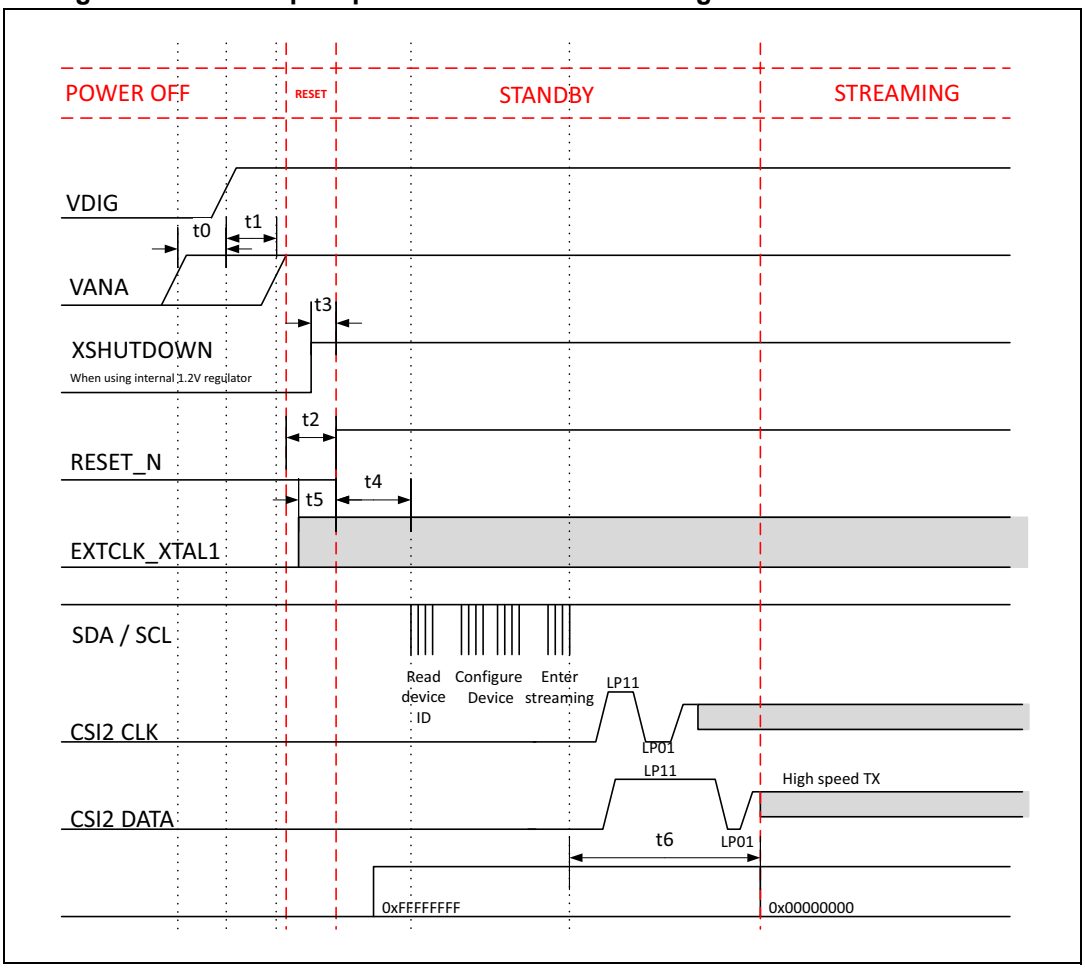
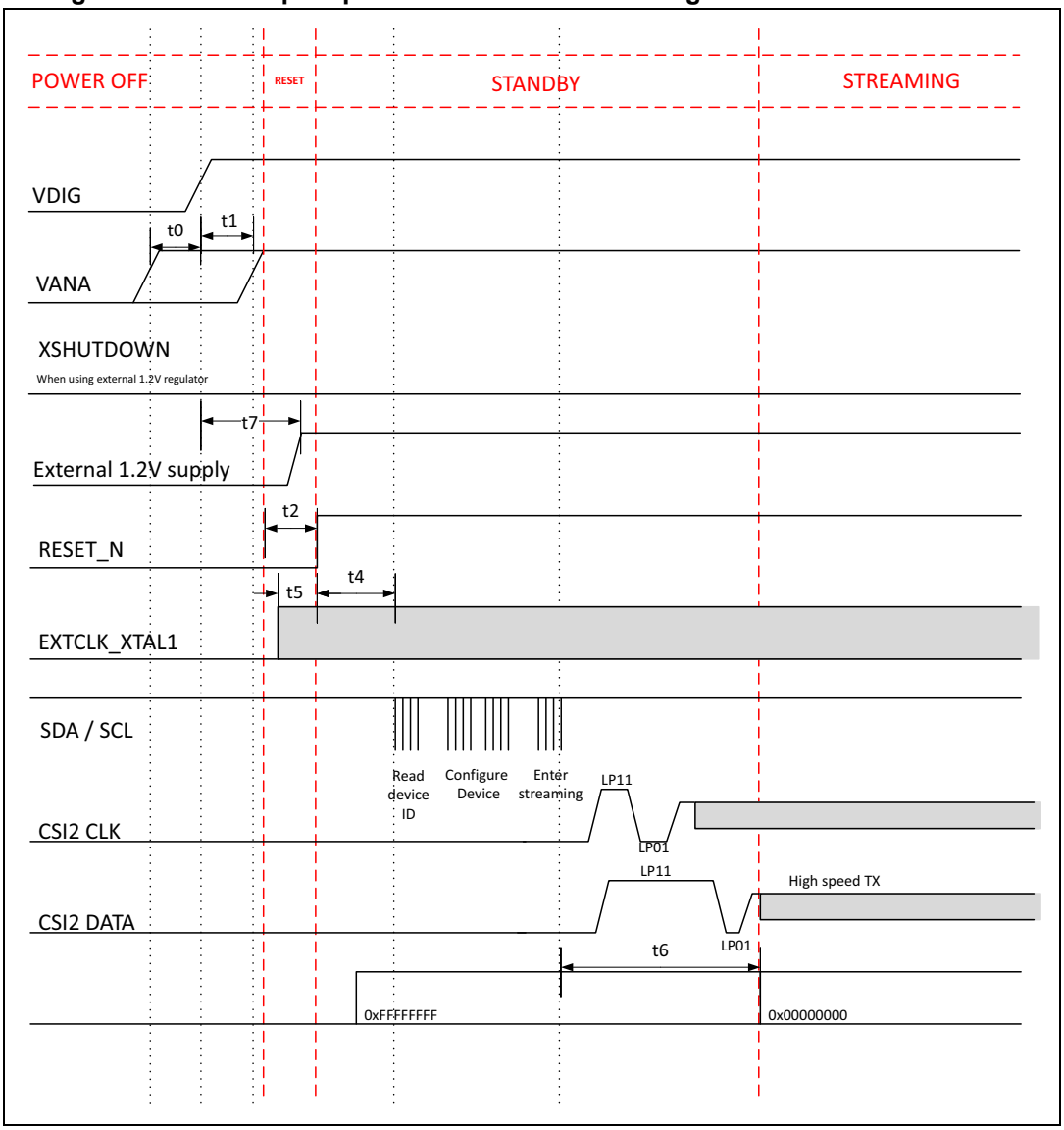


Figure 35. Power-up sequence with external 1.2V regulator in MIPI CSI-2 mode



11.3.2 Power-down procedure

Table 61. Power-down sequence timing constraints

Symbol	C	Parameter	Minimum	Maximum	Units
t8		Last I^2C transaction to frame end(1)		1	frames
t9		Frame end to RESET_N falling	512		clock cycles
t10		RESET_N falling to XSHUTDOWN falling		∞	ms
t11		RESET_N falling to EXTCLK_XTAL1 stopping		∞	ms
t12		VDIG falling to VANA falling	VANA and VDIG may fall in any order, the falling edge separation can vary from 0 ns to indefinite		
t13		VANA falling to VDIG falling			

1. The power down sequence is triggered by the I^2C power down request, however the power down sequence will only start after the end of the frame when all active data has been transferred to the output interface. Once complete, the CSI-2 data signals enter LP11. The CSI-2 clock will enter LP11 with a delay of 5 µs (corresponding to Tclk_post + Tclk_trail) after the data signals. The device will remain in LP11 unless the sensor restarts streaming or RESET_N is pulled low.

Figure 36. Power-down sequence with internal 1.2V regulator in MIPI CSI-2 mode

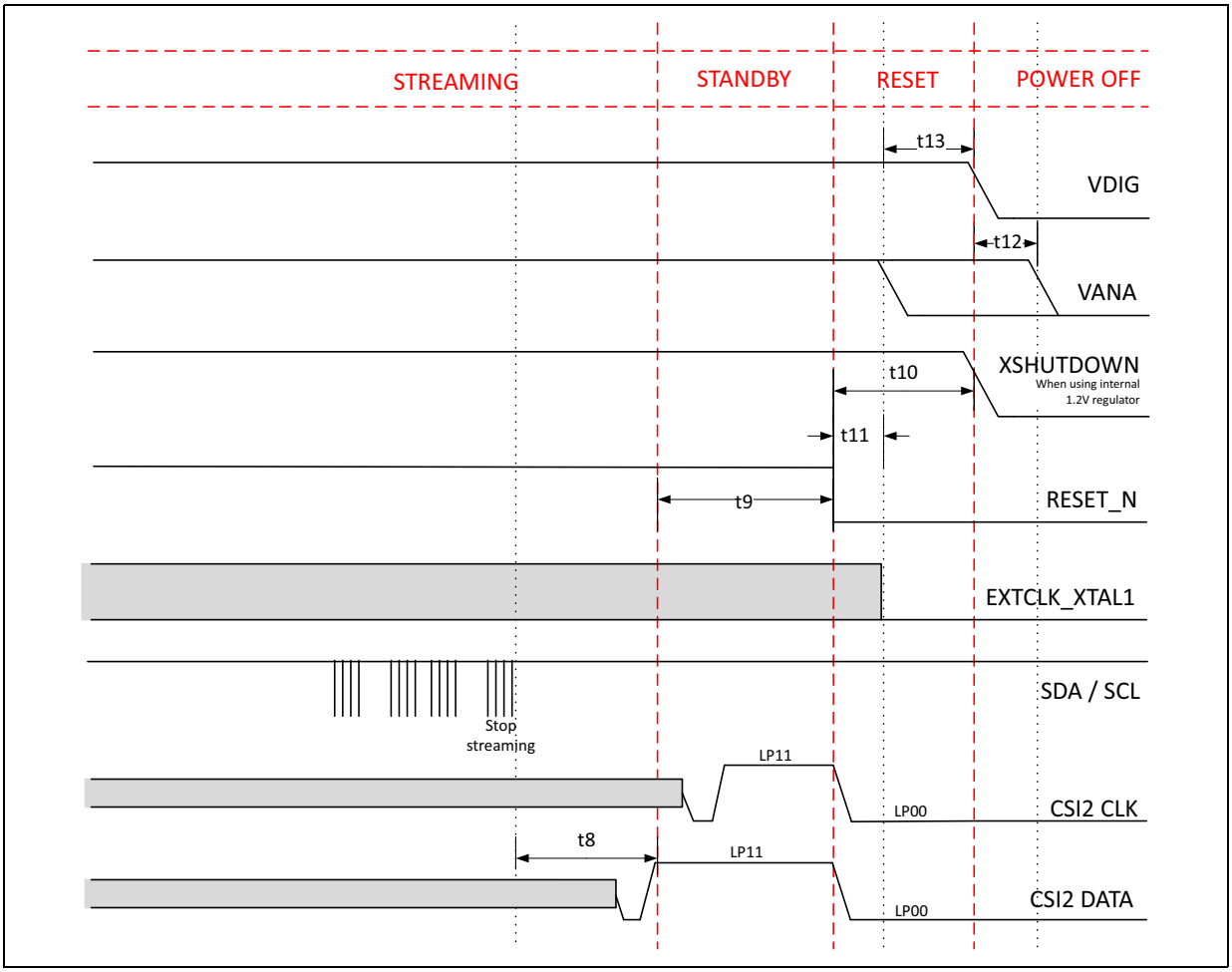
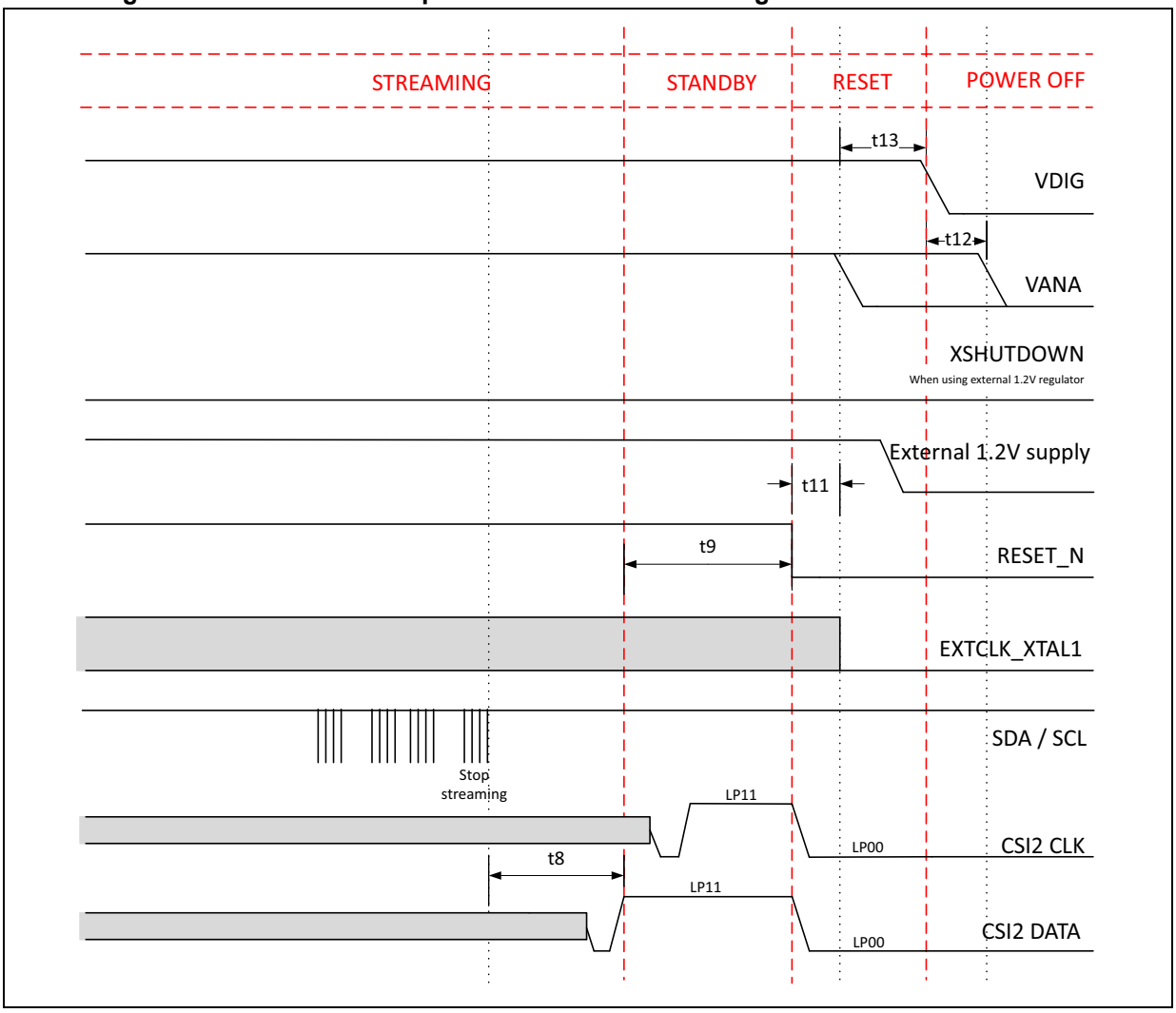


Figure 37. Power-down sequence with external 1.2V regulator in MIPI CSI-2 mode



11.3.3 Power off conditions

To avoid unnecessary leakage currents, all signals connected to the image sensor must be either at a low state or high impedance when power is removed from the device. The exceptions to this rule are the EXTCLK_XTAL1, RESET_N, XSHUTDOWN and the I^2C signals which are high impedance when the image sensor is powered-down.

11.4 External clock input

The image sensor may be clocked either using an external clock source, or by its own oscillator driven by an external crystal. The EXTCLK_EN signal selects either the external clock source (EXTCLK_EN is HI) or the external crystal (EXTCLK_EN is LO).

11.4.1 Clock source

The image sensor can accept a square wave clock input of any frequency in the range of 12MHz to 50MHz.

The clock input has a Schmitt trigger and is high impedance in any mode including the power off state.

11.4.2 Quartz crystal

When using a quartz crystal in combination with the image sensor's internal oscillator block, the crystal must meet the following specification.

Figure 38. Equivalent model of crystal

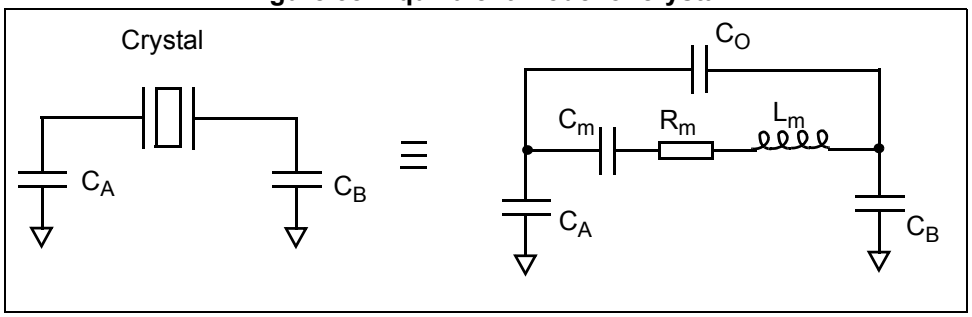


Table 62. Recommended crystal specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_L	Crystal load capacitance(1)		8		15	pF
C_O	Total crystal shunt capacitance	8pF < C_L < 12pF	0		3	pF
		12pF < C_L < 15pF	0		5	
C_A, C_B	Total input or output capacitance(2)	8pF < C_L < 12pF	10		19	pF
		12pF < C_L < 15pF	14		27	

1. $C_L = C_A*C_B/(C_A+C_B) + C_O$
2. Including ball, board, component and parasitic capacitances

The internal oscillator block is not designed to operate with overtone type crystals.

Please contact your local STMicroelectronics support representative for further information regarding the use of the crystal oscillator feature.

11.5 I2C pull-up resistors

If the I2C interface is to only be used in Fast mode (400KHz) then a pull-up resistor value of around 1K ohm is recommended for the SDA signal.

If the I2C interface is to be used in Fast+ mode (1MHz) then the value of pull-up resistor must be chosen to ensure I2C bus constraints are met in both Fast and Fast+ mode. This is due to the fact the 6640 will initially be in Fast mode, with a low current sink capability on SDA, then will be switched to Fast+ mode via an I2C write. To ensure that the SDA signal can correctly ACK a transaction in Fast mode the pull-up resistance must not be too low. A value of around 600 ohms is appropriate to meet this constraint.

Correct characteristics of the I2C signals should always be check by measurements on actual circuit boards as PCB parasitic capacitance can affect the signal rise and fall times.

11.6 External sync input

The image sensor can accept an external synchronization (sync) input from either an I^2C signal or an external signal.

For an external signal (FSYNC_IN), the synchronization occurs on the rising edge of the signal only.

The image sensor measures the delay between the external sync signal and the internal frame start and records the value in a status register. Re-synchronizing the frame will not cause corruption to the current image streaming. If the initial sync signal occurs during the active part of a frame, the sensor will complete the current frame, then output the next frame as soon as possible (i.e. with minimum frame blanking). In that way, the output frames will synchronize with the frame sync signal after several frames have been streamed and with no loss or corruption of frames.

The image sensor also provides a frame synchronization output (FSYNC_OUT) that provides a rising edge when integration of the frame starts.

11.7 Error correcting code (ECC) output

Error correcting code (ECC) checking is provided on the MCU SRAM memories.

If a single bit error occurs, the error is corrected. In this case, a flag is set and a counter is incremented in the registers and status line.

If double bit error occurs, it cannot be corrected. In this case, a flag is set and the ECC_OUT signal is latched and will remain HI. Normally the companion device would reset the image sensor in this case, since the internal firmware of the sensor may be corrupted.

12 Non-volatile memory (NVM)

The image sensor contains 4 Kbits of one-time programmable memory. This memory space may be used to store manufacturing specific data such as revision number, anti-vignetting parameters, couplet information, customer-specific data and so on.

13 Package information

13.1 Im2BGA package information

The package is compliant with ST's ECOPACK2 standard of environmental protection (including RoHS compliance and "Halogen Free"). ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

Note: The terminal A1 corner is identified on the top surface by using a corner chamfer, ink or metrallized markings, or other feature of package body.

Figure 39. Im2BGA top view

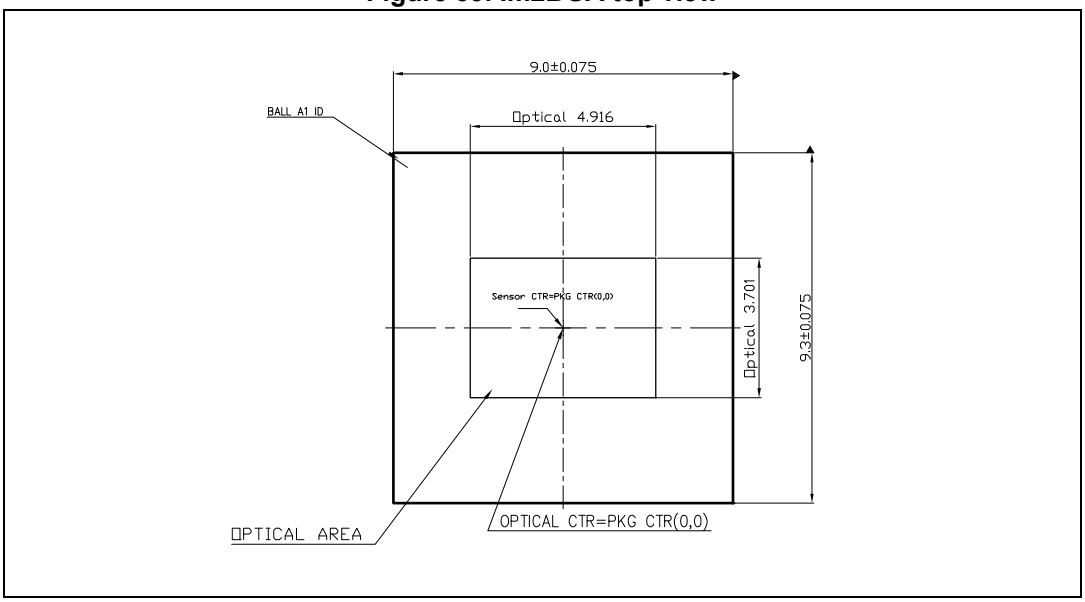


Figure 40. Im2BGA bottom view

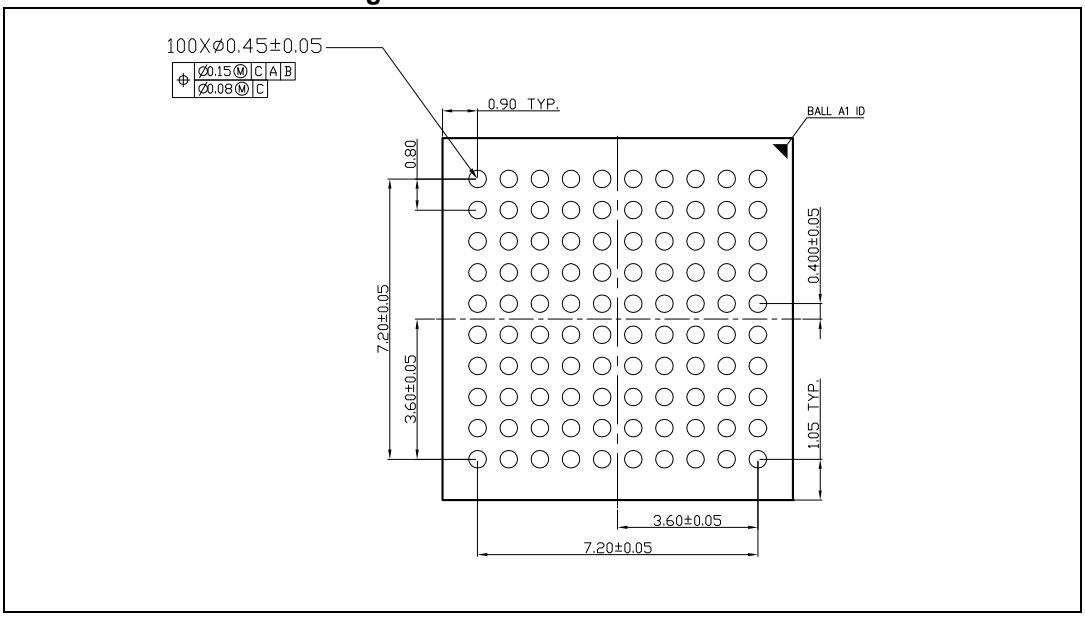


Figure 41. Im2BGA side view

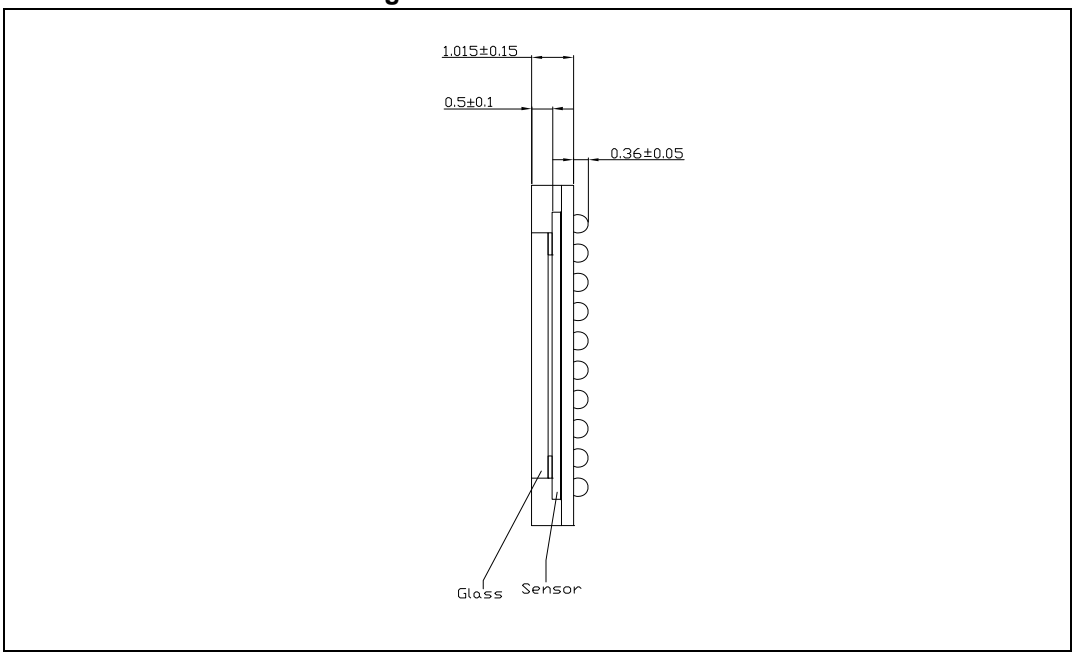
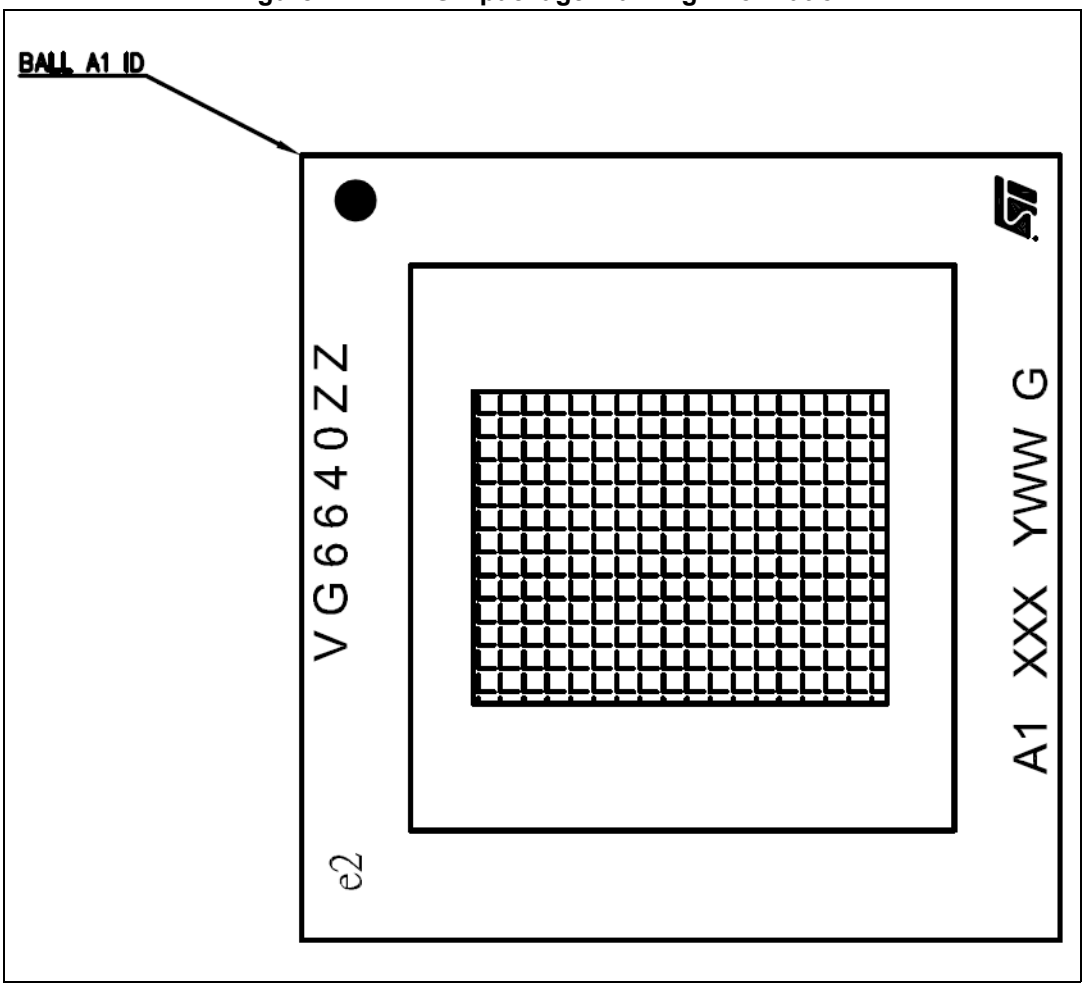


Diagram above shows typical ball height as delivered is 0.36mm.

13.2 Im2BGA package marking information

Figure 42. Im2BGA package marking information



13.3 Delivery of packaged parts

Packaged parts may be delivered with or without a protective glass liner. The protective glass liner can be removed manually or by using a horizontal blade of air to prevent glass contamination/scratches. ST are not liable for damage caused during removal of the liner.

14 Ordering information

Table 63. Ordering information

Ordering code	Color filter	Device package	Packing	Automotive
VG6640AB1M/1	RGB Bayer	Im2BGA	Tape and reel	Yes
VG6640AB1M			Tray (1)	
VG6640CB1M/1			Tape and reel	No
VG6640CB1M			Tray (1)	
VD6640CB/UW		Bare die	Tested wafer	

1. Sample quantities only

15 Acronyms and abbreviations

Table 64. Acronyms and abbreviations

Acronym/ abbreviation	Definition
ASIL	Automotive safety integrity level
CDM	Charged device model
CRC	Cyclic redundancy check
CSI	Camera serial interface
DPCM	Differential pulse code modulation
ECC	Error correction code
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOF	End of frame
EOT	End of transmission
FE	Frame end
FFOV	Full field of view
FIFO	First-in, first out (memory)
FOV	Field of view
fps	Frames per second
FS	Frame start
GPIO	General purpose input/output
HBM	Human body model
HDR	High dynamic range
HS	High speed; identifier for operation mode
HS-RX	High speed receiver (low-swing differential)
HS-TX	High speed transmitter (low-swing differential)
I^2C	Inter integrated circuit (bus)
LDO	Low dropout (regulator)
LE	Line end
LLP	Low level protocol
LS	Line start
LSB	Least significant byte
LP	Low power; identifier for operation mode
LP-RX	Low power receiver (large-swing single ended)
LP-TX	Low power transmitter (large-swing single ended)
LVDS	Low voltage differential signaling

Table 64. Acronyms and abbreviations (continued)

Acronym/ abbreviation	Definition
Mbps	Megabits per second
MCU	Microcontroller unit
MIPI	Mobile industry processor interface
MSB	Most significant byte
PCK	Pixel clock
PCM	Pulse code modulation
PF	Packet footer
PH	Packet header
PI	Packet identifier
PT	Packet type
PHY	Physical layer
PLL	Phase locked loop
POR	Power on reset
RO	Read only
ROI	Region of interest
RW	Read/write
SCL	Serial clock (for I^2C)
SDA	Serial data (for I^2C)
SMIA	Standard mobile imaging architecture
SOT	Start of transmission
SOF	Start of frame
SSCG	Spread spectrum clock generator
SubLVDS	Sub-low voltage differential signaling
ULPM	Ultra low power mode
WOI	Window of interest

16 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

17 Revision history

Table 65. Document revision history

Date	Revision	Changes
04-Sep-2012	1	Initial release.
29-Oct-2012	2	Minor correction to application schematic
08-Oct-2013	3	Minor updates throughout. Updated*: Features on page 1* Updated *Table 2: Technical specifications on page 9* Added *Chapter 2: Signal, ball assignment, pad, and wafer description on page 14* Updated *Figure 4: Block diagram on page 19* Updated *Figure 5: Custom analog block (CAB) block diagram on page 21* Updated *Section 3.2.4: HDR rescaling on page 24* Updated *Section 3.2.6: Status and trailer lines on page 24* Updated *Section 3.3.2: Reset state on page 25* Updated *Chapter 4: Control interface on page 27* Updated *Section 4.1: Register formats on page 30* Added *Section 4.2: Register map on page 32* Updated *Table 33: Typical subsampling settings on page 73* Removed sections 5.1.3 and 5.1.4 from Rev 2. Updated *Section 8.1.5: HDR grayscale mode on page 86* Minor update throughout Updated cursor control register addresses Updated power up state diag. Updated diag showing Int and readout timing Added Diag showing CCI update window and retiming in frame Updated clock options and removed figure 32 Updated Min and Max values for Video timing Updated registers Update test pages
19-May-2014	4	updates and corrections throughout updates to test patterns updates to register map more details on ITU interface updates to package information updated section 9 power up / power down diag to include external 1V2 supply updated MIPI references Updated RO registers to Do Not Write (DNW) small corrections before release

Table 65. Document revision history (continued)

Date	Revision	Changes
4-Nov--2014	5	Minor correction to application schematic. Update specification to match cut2.0 Update register map for cut2.0 Update video timing for cut2.0 Remove reference to cursor in test modes Updated max freq of ITU interface Updated package info and drawings Package references changed to Im2BGA Add QE graph for VG8640 RCCC part Correct fine integration times Correct text describing Digital Gains Change references to RO in the register map to DNW Updated clock relationship diag to reflect cut2.0 Add details of defect correction options Include extra features in Features section more detail re PWL curve more detail on ASIL lines Corrected timing formulae to include /2 added color part number to Bayer discussion Detail added to Pixel Gain detail added to HDR merge diag added pixel sensitivity to table 2 correct spelling made timing diag more legible changed I2C resistor values in Example applications Changed front page image to g2BGA package Corrected min frame length

Table 65. Document revision history (continued)

Date	Revision	Changes
10-May-2015	6	Updated Table 36 to reflect min frame length of 1023 lines for Full FoV Changed package information to Im2BGA Added EXTCLK_XTAL1 and XTAL2 pins to signal Description Table. Update to Signal Description table. Update to Ball Assignment diagram. Removed references to ULPM Changed names of CSI2 interface signals to DP_L1 format. Updates to *Table 2: Technical specifications* Removed RCCC modes from *Table 33: Typical subsampling settings*. Added notes to state only odd values supported by Y_xxx_INC registers. Changed “software standby”state name to “standby”. Changed “hardware standby” state name to “reset”. Updates to the layout guidelines in section 10. Updates to some register descriptions. Correction to ordering codes. Changed “Max Storage Temperature” to 125C Revisions to *Figure 16: CSI-2 frame format*
09-Oct-2015	7	VDIG max voltage to 2.94V Current consumption in *Table 42*, *Table 43* and *Table 44*. Added *Table 49*, modification to *Table 51*, *Table 52* Updates to *Table 59* Electro-optical characteristics moved from Section 1 to, newly created, *Section 10* Power consumption in *Table 2* changed to 400mW. Removed “peak current consumption” table. Updated ITU Timing Diagram Replaced “Fig 20: Clock relationships” with new “Clock Tree” diagram and updated equations below to match. Removed *Section .4.1.1: Multi-byte registers index space* Added constraints to Knee1/2 and SigmaGhostThresh1/2 values. Added ParOutIF_Drive (0x24A2) register. Added warning about the use of the clock gating options available in the ParOutIF_Control (0x24A3) register. Added *Table 1: Device summary* to cover page. Renamed *Section 4.2.9* to “Temperature sensor registers”

Table 65. Document revision history (continued)

Date	Revision	Changes
14-Dec-2015	8	Improved consistency of bit field representation in register map. Naming of some registers and bit fields to match User Manual usage. Note about external clock rate needed for 1MHz SCL. Removed corrupt frame masking registers. Test pattern generator section re-written. Electrical characteristics section updated with latest test results. Removed Cut1.0 register “Dgain_Legacy”
11-May-2016	9	Figure 31 - Changed I2C pull-ups from 2V8 to 1V8. Removed “exposure” from section name 3.2.1. Replaced “Marking information” diagram. Added Automotive” to document title. Changed name of section “Mechanical” to “Package information” I2C pulse width suppression ($t_{SP)}$ max set to 50ns. I2C hold time ($t_{HD.DAT)}$ minimum set to 16ns. Modifications to Figures 32 to 35: added “in MIPI CSI-2 mode” to title; modified state names to match state diagram in Section 3; LP11 state extended to all of standby period in power down diagrams. Correction to Section 3.3.3. to mention LP11 state in Standby state. Added footnote to Table 42 about VANA current in standby state when CSI-2 interface used. Table 46 - removed classification, added tbc to frequency limits. Added into Section 11.4.2. a note to saying to contact ST support for further information. Section 7.3.3 changed lower limit of digital gains to zero.

Table 65. Document revision history (continued)

Date	Revision	Changes
06-Dec-2016	10	Update *Figure 42: Im2BGA package marking information*
22-Jun-2018	11	Updated document status which is no longer confidential Removed all products which remained at the development stage and were never released to customers: VG5640, VG8640, VD5640, and VD8640. Removed all mentions of support for 2.8 V: *Table 2: Technical specifications*, *Section 1.2: Power supplies*, *Table 4: Signal description with Im2BGA 100 balls*, and *Section 11.1.2: Example stereo synchronized cameras application*. Renamed *Table 1: Device summary* Renamed *Section 2: Signal, ball assignment, pad, and wafer description* Removed *Section 2.2: Ball assignment* Added *Figure 2: IO ring pad layout* and *Figure 3: Wafer description and stack*. *Section 4.2.15: Statistics control registers [0x24A6 - 0x24D3*: added “data refers only to RGB”. *Figure 20* and *Figure 22*: added “valid only for RGB”. Updated *Section 7.2: Bayer pattern* *Section 7.3.3: Digital gain*: added “text refers only to RGB”. Updated *Table 39: Parameter classification* Updated *Table 41: Operating conditions* Updated *Table 42: Typical current consumption in reset and standby*. Updated *Table 45: EXTCLK_XTAL1 - characteristics* Updated *Table 49: Digital input - signal characteristics* Updated *Table 50: Digital output - signal characteristics* Updated *Table 51: I2C interface - signal characteristics* Updated *Table 57: Parallel interface - signal characteristics* *Table 59: Electro-optical characteristics*: replaced “specification” in table title with “characteristics”; replaced all “P” classifications by “T”. Added *Section 13.3: Delivery of packaged parts* *Table 63: Ordering information*: removed all CPNs which remained in the development stage.