STI40N65M2, STP40N65M2

N-channel 650 V, 0.087 Ω typ., 32 A MDmesh™ M2 Power MOSFET in I²PAK and TO-220 packages

Datasheet - production data

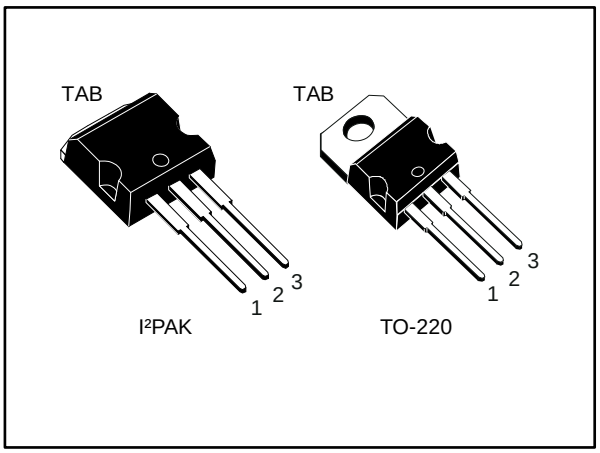
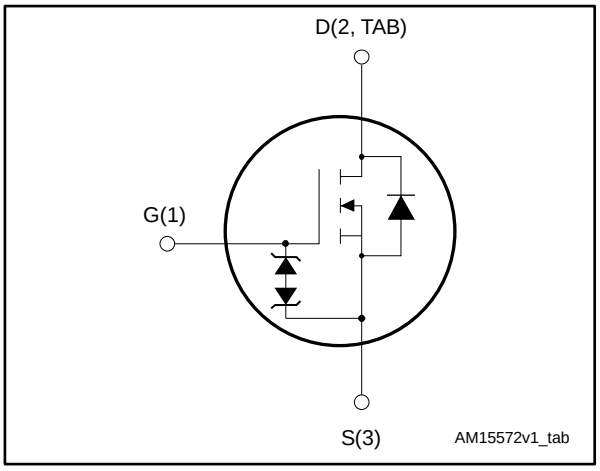


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STI40N65M2	650 V	0.099 Ω	32 A
STP40N65M2			

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STI40N65M2	40N65M2	I²PAK	Tube
STP40N65M2		TO-220	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	32	A
I_D	Drain current (continuous) at T_C= 100 °C	20	A
I_{DM} (1)	Drain current (pulsed)	128	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	

Notes:

(1) Pulse width limited by safe operating area.

(2) $I_{SD} \leq 32$ A, di/dt ≤ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD} = 400 V

(3) $V_{DS} \leq 520$ V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	820	mJ

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 16 A		0.087	0.099	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	2355	-	pF
C_{oss}	Output capacitance		-	102	-	pF
C_{rss}	Reverse transfer capacitance		-	2.7	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 V to 520 V, V_{GS} = 0 V	-	380	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, open drain	-	4.5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 32 A, V_{GS} = 10 V (see *Figure 15: "Gate charge test circuit"*)	-	56.5	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	24	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 16 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Switching times test circuit for resistive load"* and *Figure 19: "Switching time waveform"*)	-	15	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	96.5	-	ns
t_f	Fall time		-	12	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		32	A
I_{SDM} (1)	Source-drain current (pulsed)		-		128	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 32 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 32 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 16: " Test circuit for inductive load switching and diode recovery times"*)	-	468		ns
Q_{rr}	Reverse recovery charge		-	8.7		µC
I_{RRM}	Reverse recovery current		-	37.5		A
t_{rr}	Reverse recovery time	I_{SD} = 32 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 16: " Test circuit for inductive load switching and diode recovery times"*)	-	610		ns
Q_{rr}	Reverse recovery charge		-	11.7		µC
I_{RRM}	Reverse recovery current		-	39		A

Notes:

(1)Pulse width is limited by safe operating area

(2)Pulse test: pulse duration = 300 µs, duty cycle 1.5%

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

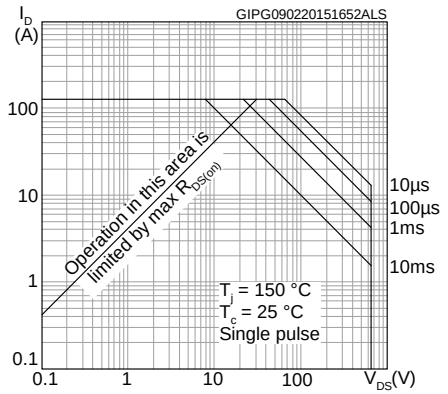


Figure 3: Thermal impedance

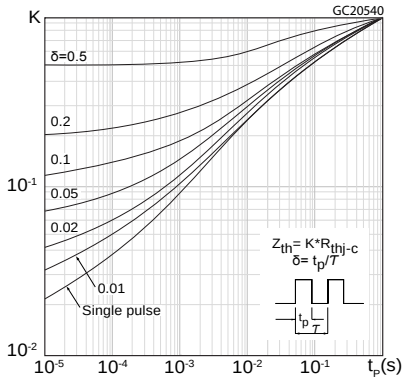


Figure 4: Output characteristics

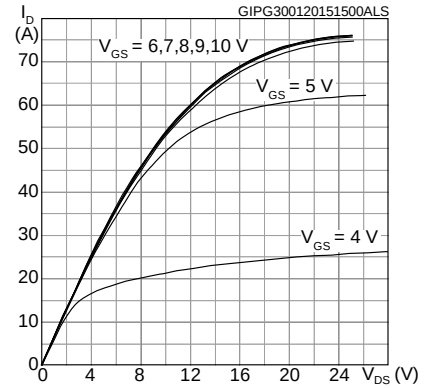


Figure 5: Transfer characteristics

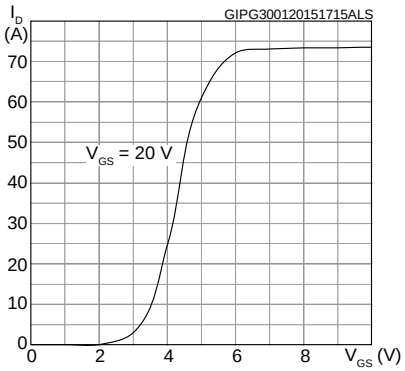


Figure 6: Normalized gate threshold voltage vs temperature

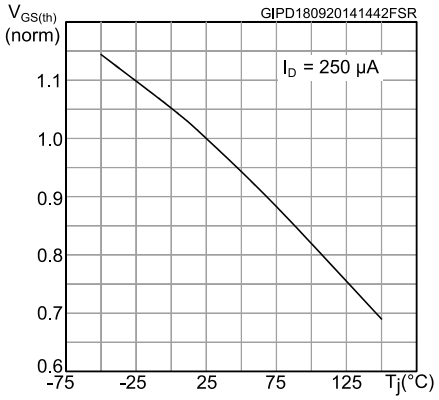


Figure 7: Normalized V(BR)DSS vs temperature

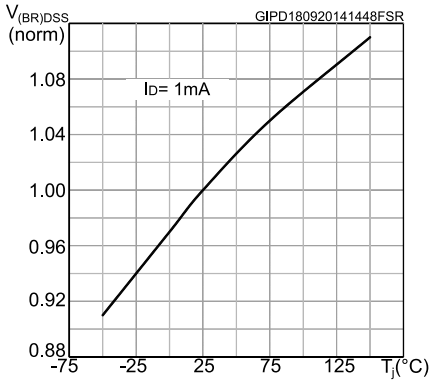


Figure 8: Static drain-source on-resistance

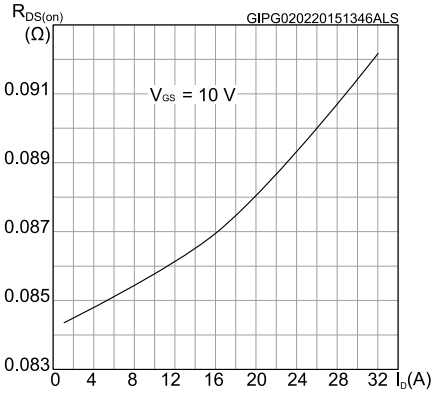


Figure 9: Normalized on-resistance vs. temperature

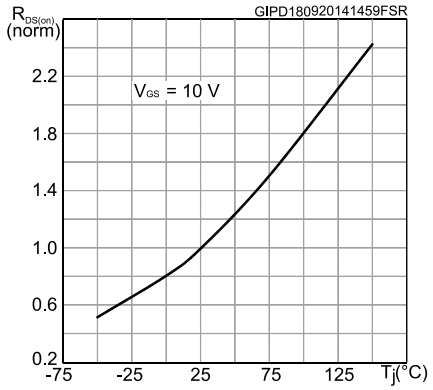


Figure 10: Gate charge vs. gate-source voltage

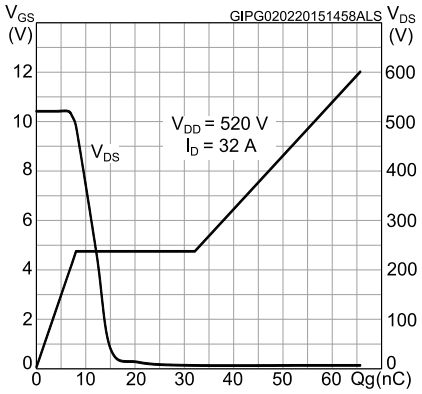


Figure 11: Capacitance variations

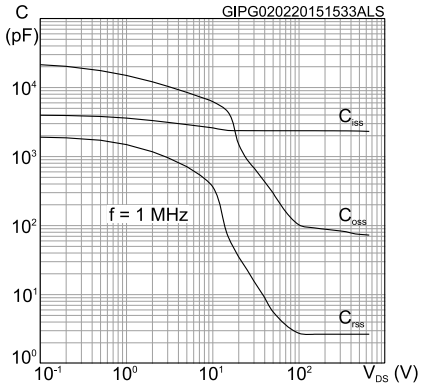


Figure 12: Output capacitance stored energy

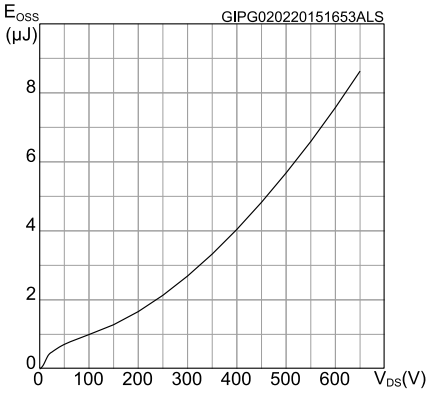
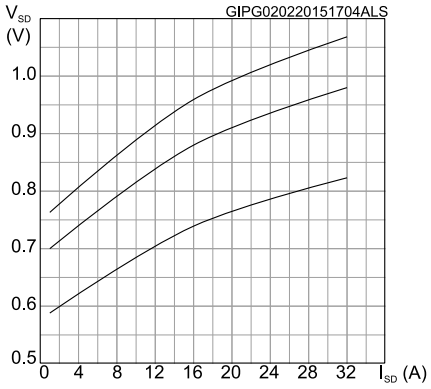


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Switching times test circuit for resistive load

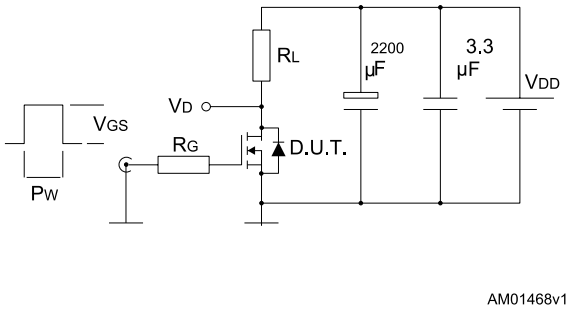


Figure 15: Gate charge test circuit

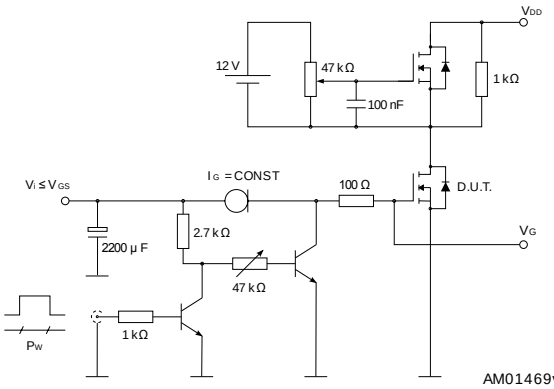


Figure 16: Test circuit for inductive load switching and diode recovery times

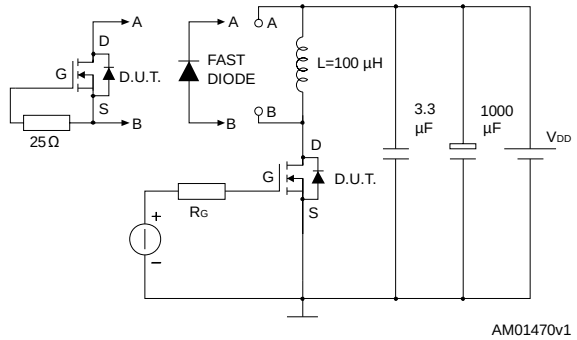


Figure 17: Unclamped inductive load test circuit

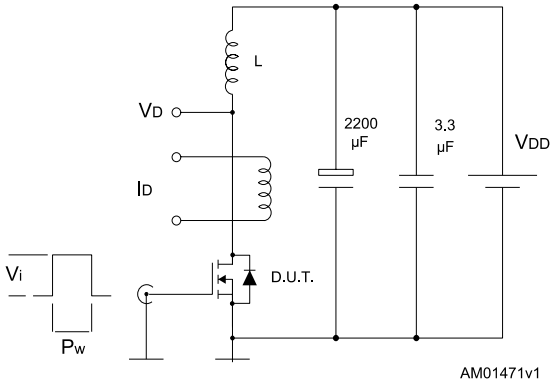


Figure 18: Unclamped inductive waveform

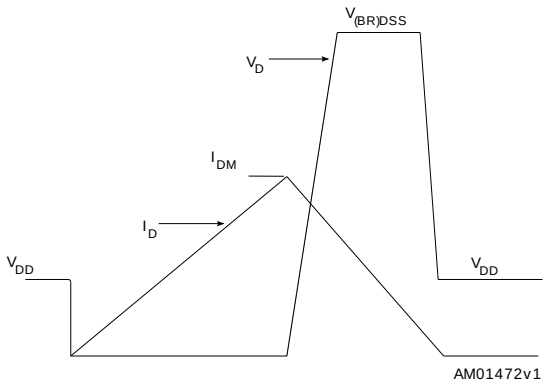
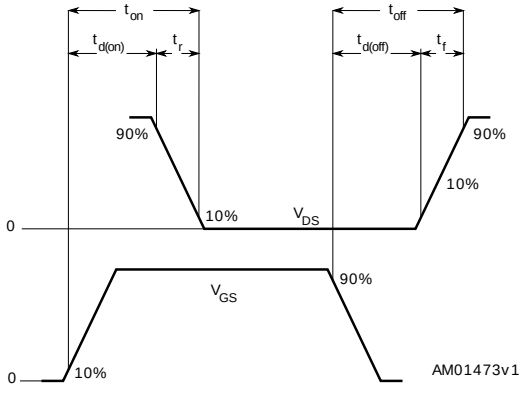


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 20: I²PAK package outline

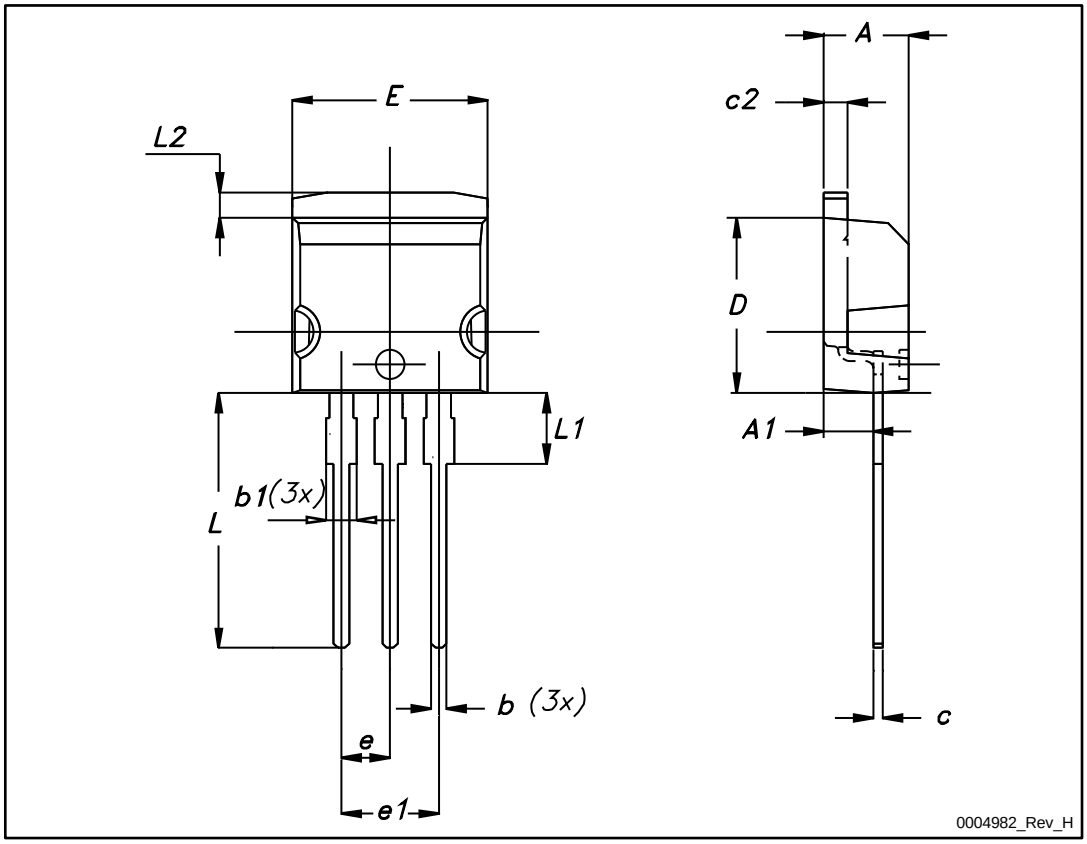


Table 9: I²PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	–	4.60
A1	2.40	–	2.72
b	0.61	–	0.88
b1	1.14	–	1.70
c	0.49	–	0.70
c2	1.23	–	1.32
D	8.95	–	9.35
e	2.40	–	2.70
e1	4.95	–	5.15
E	10	–	10.40
L	13	–	14
L1	3.50	–	3.93
L2	1.27	–	1.40

4.2 TO-220 type A package information

Figure 21: TO-220 type A package outline

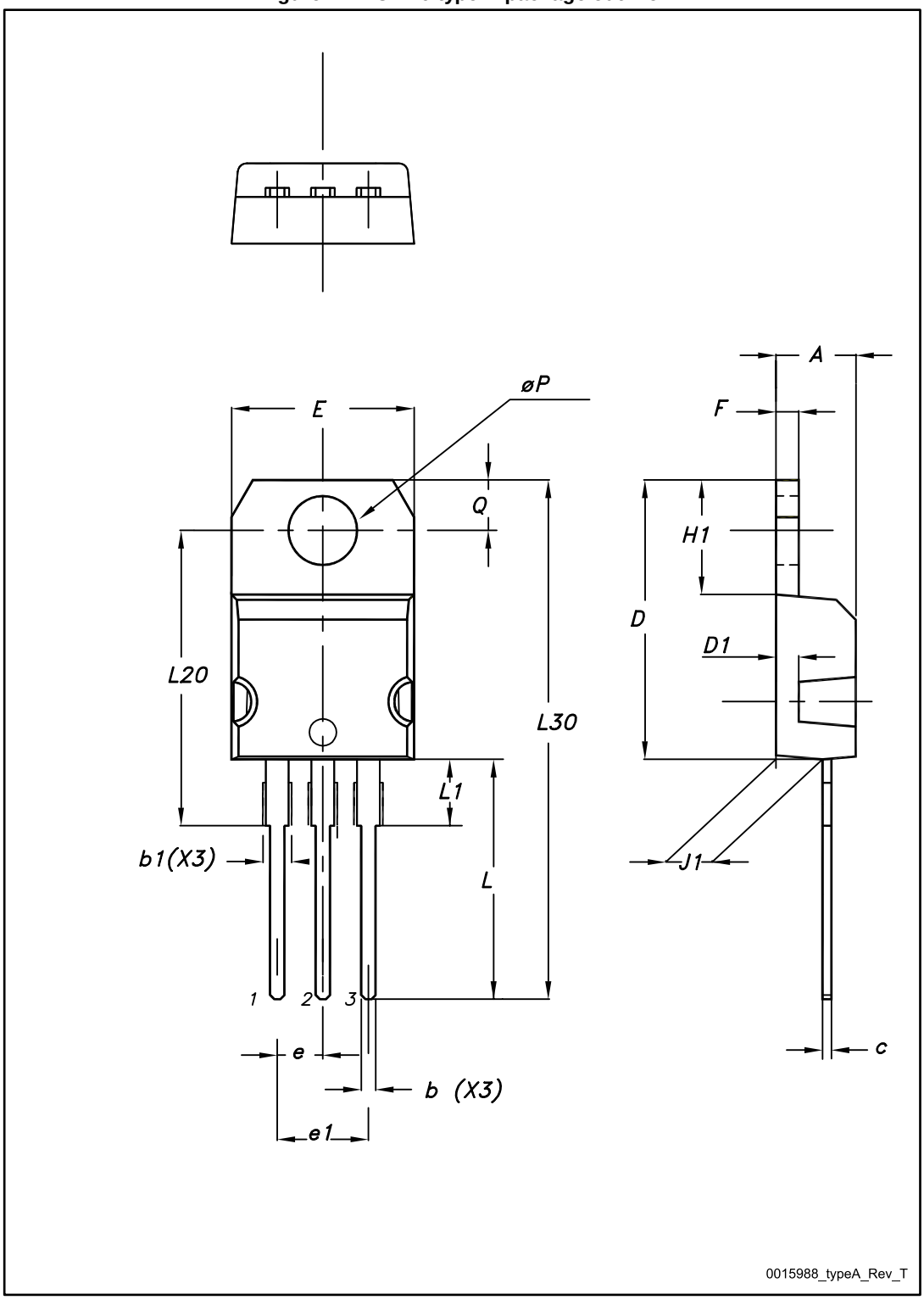


Table 10: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
09-Feb-2014	1	First release.

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