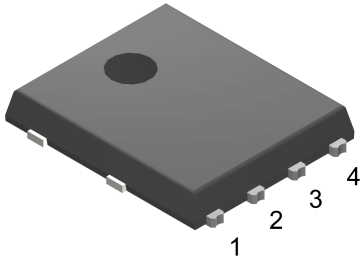
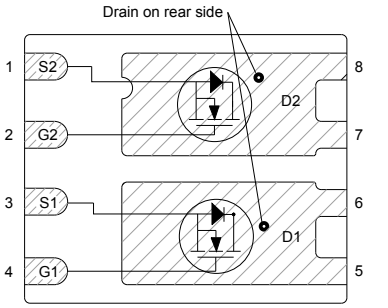
Automotive-grade dual N-channel 60 V, 22.5 mΩ typ., 7.8 A STripFET F3 Power MOSFET in a PowerFLAT 5x6 double island package



PowerFLAT 5x6 double island



NG14G22D1D2RSS13S21

STPOWER

Product status link
STL8DN6LF3

Product summary	
Order code	STL8DN6LF3
Marking	8DN6LF3
Package	PowerFLAT 5x6 double island
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL8DN6LF3	60 V	30 mΩ	7.8 A

- AEC-Q101 qualified
- Logic level $V_{GS(th)}$
- 175 °C maximum junction temperature
- 100% avalanche rated
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±20	V
V_{DS}	Drain-source voltage	60	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	20	A
I_D	Drain current (continuous) at T_C = 100 °C	20	A
I_D(2)	Drain current (continuous) at T_{pcb} = 25 °C	7.8	A
	Drain current (continuous) at T_{pcb} = 100 °C	5.5	A
I_{DM}(2)(3)	Drain current (pulsed)	31.2	A
P_{TOT}	Total power dissipation at T_C = 25 °C	65	W
P_{TOT}(2)	Total power dissipation at T_{pcb} = 25 °C	4.3	W
I_{AV}	Non-repetitive avalanche current	7.8	A
E_{AS}(4)	Single pulse avalanche energy	190	mJ
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Current is limited by bonding, with R_{thJC} = 2.3 °C/W; the chip is able to carry 30 A at 25 °C.*
2. *When mounted on an 1 inch² 2 Oz. Cu board, t < 10 s.*
3. *Pulse width is limited by safe operating area.*
4. *Starting T_J = 25 °C, I_D = I_{AS}, V_{DD} = 25 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.3	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	35	

1. *When mounted on an 1 inch² 2 Oz. Cu board, t < 10 s.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		22.5	30	mΩ
		V_{GS} = 5 V, I_D = 4 A		30	44	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	668	-	pF
C_{oss}	Output capacitance		-	144	-	pF
C_{rss}	Reverse transfer capacitance		-	14	-	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 7.8 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	13	-	nC
Q_{gs}	Gate-source charge		-	2.4	-	nC
Q_{gd}	Gate-drain charge		-	3	-	nC
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	4	-	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	9	-	ns
t_r	Rise time		-	7.7	-	ns
$t_{d(off)}$	Turn-off delay time		-	32.5	-	ns
t_f	Fall time		-	5	-	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.8	A
I_{SDM}	Source-drain current (pulsed)		-		31.2	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 7.8 A	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 7.8 A, di/dt = 100 A/µs, V_{DD} = 48 V, T_J = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	30		ns
Q_{rr}	Reverse recovery charge		-	35		nC
I_{RRM}	Reverse recovery current		-	2.35		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

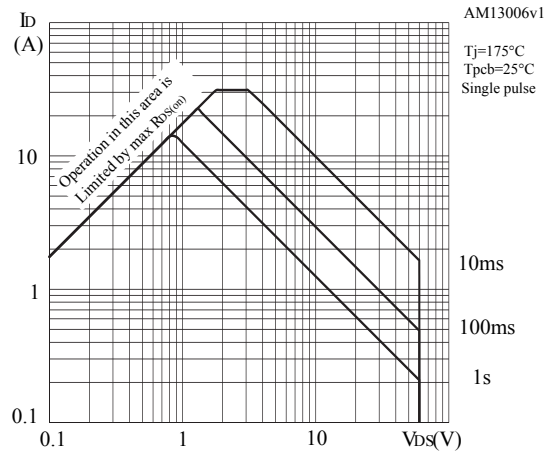


Figure 2. Thermal impedance

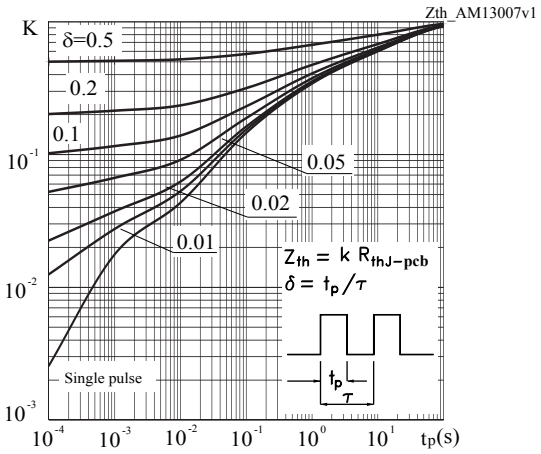


Figure 3. Output characteristics

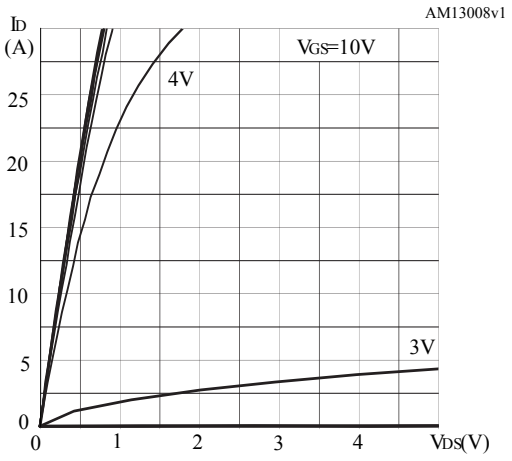


Figure 4. Transfer characteristics

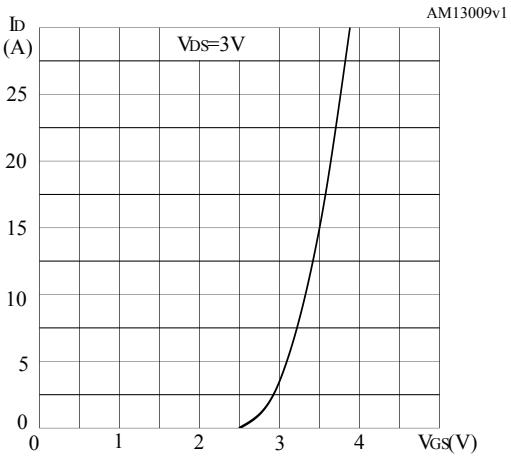


Figure 5. Normalized $V_{(BR)DSS}$ vs. temperature

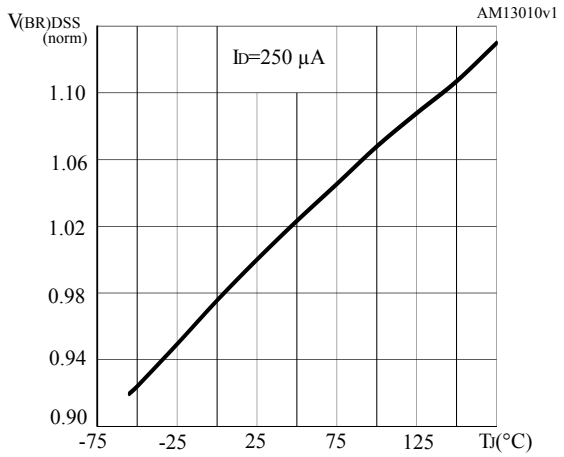


Figure 6. Static drain-source on-resistance

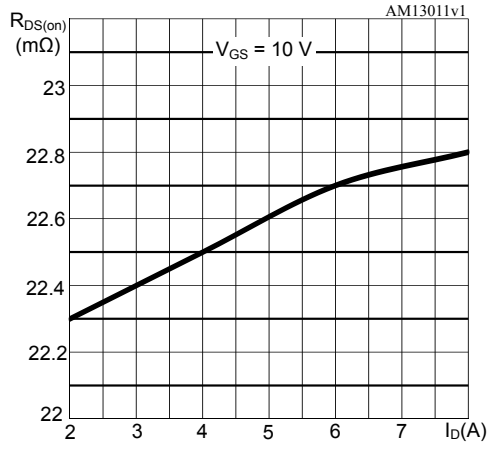


Figure 7. Gate charge vs. gate-source voltage

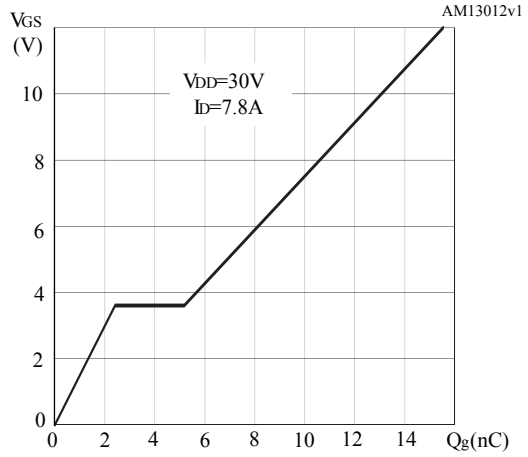


Figure 8. Capacitance variations

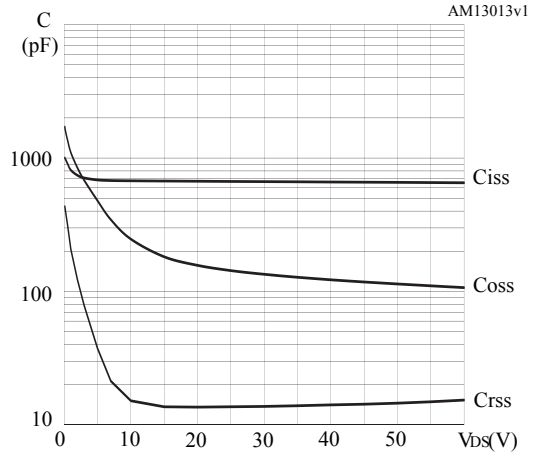


Figure 9. Normalized gate threshold voltage vs. temperature

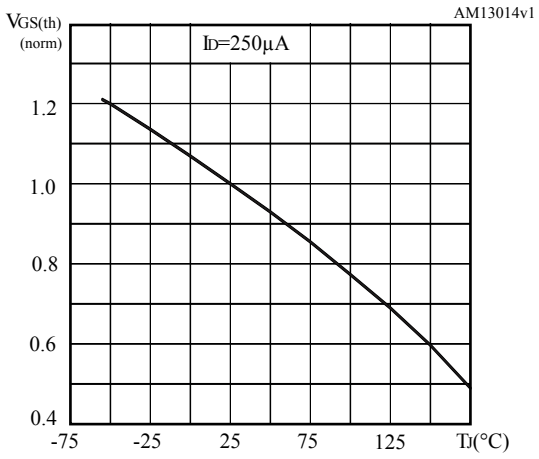


Figure 10. Normalized on-resistance vs. temperature

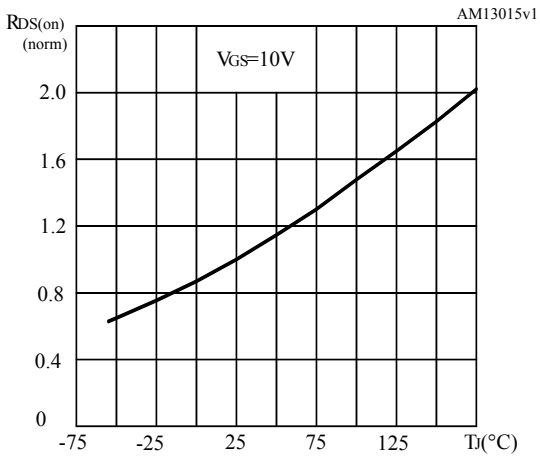
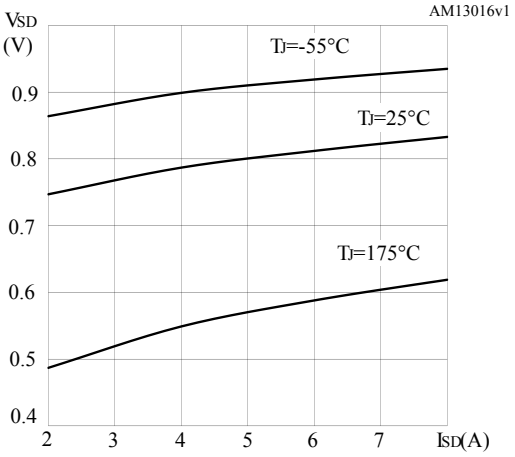


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

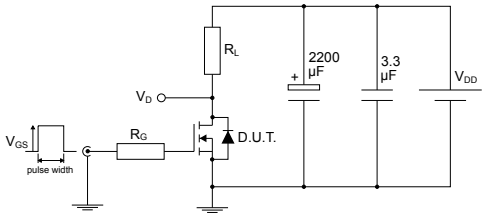


Figure 13. Test circuit for gate charge behavior

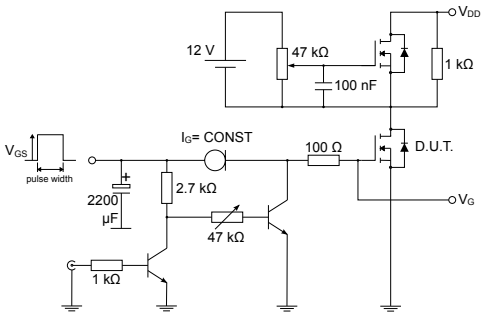


Figure 14. Test circuit for inductive load switching and diode recovery times

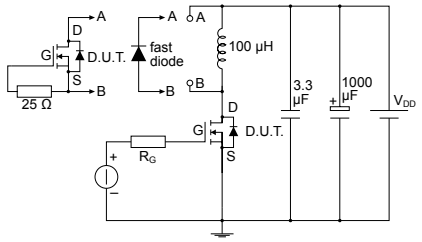


Figure 15. Unclamped inductive load test circuit

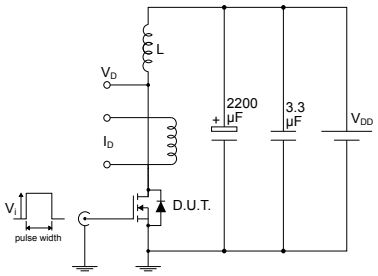


Figure 16. Unclamped inductive waveform

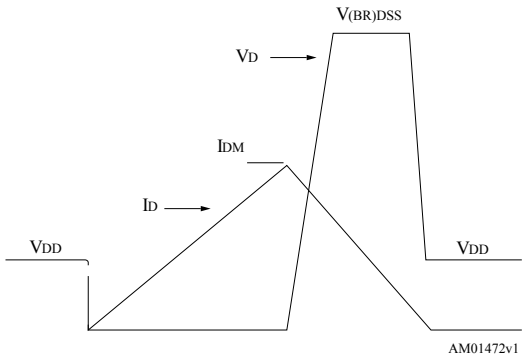
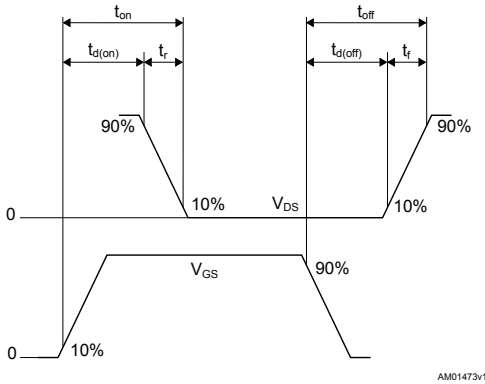


Figure 17. Switching time waveform

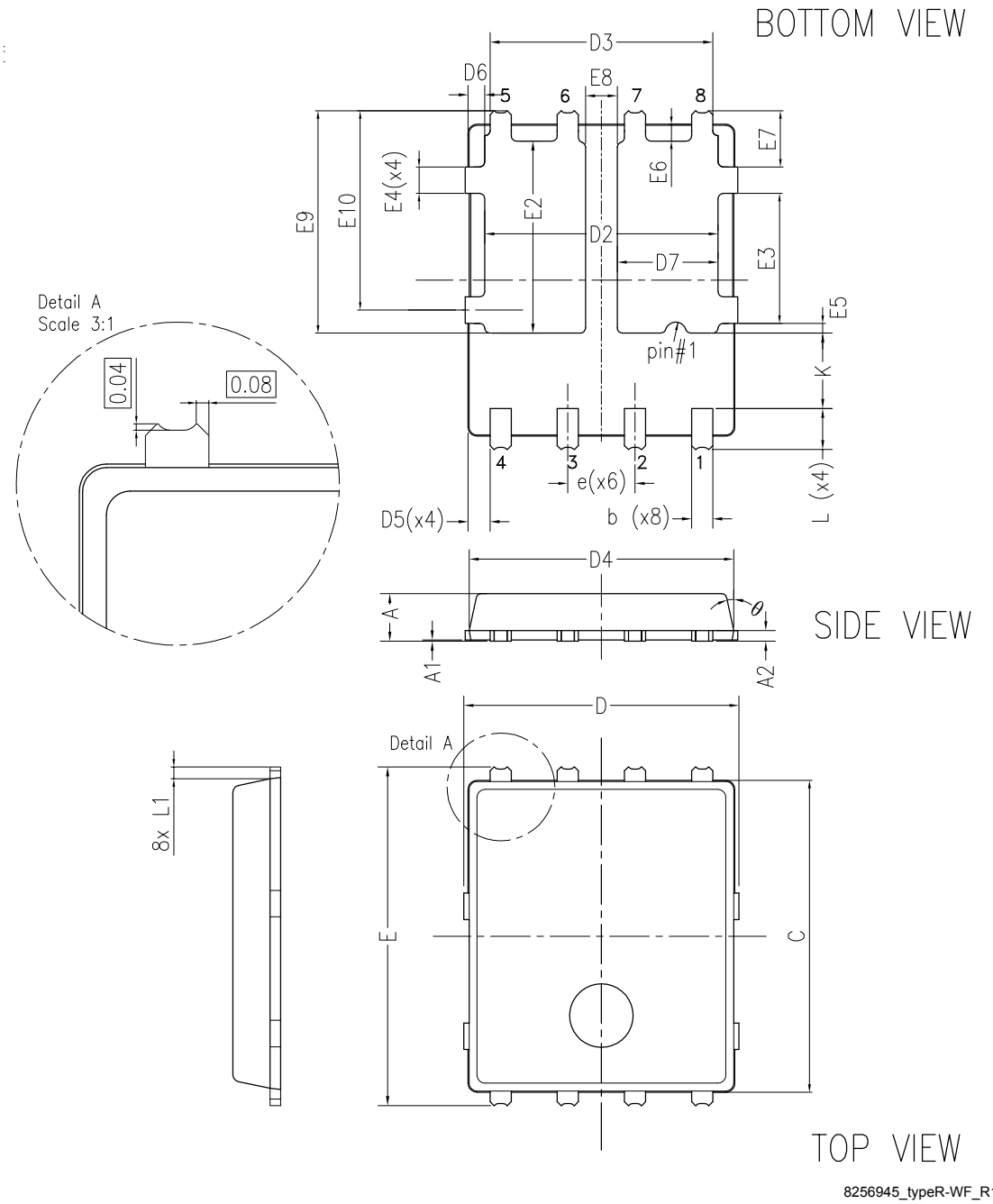


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 double island WF type R package information

Figure 18. PowerFLAT 5x6 double island WF type R package outline

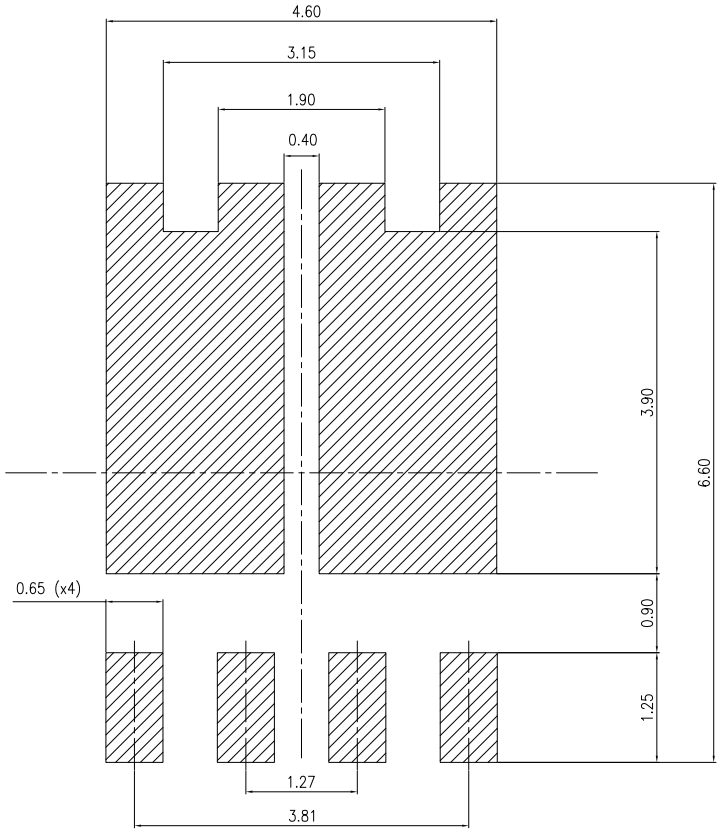


8256945_typeR-WF_R18

Table 7. PowerFLAT 5x6 double island WF type R mechanical data

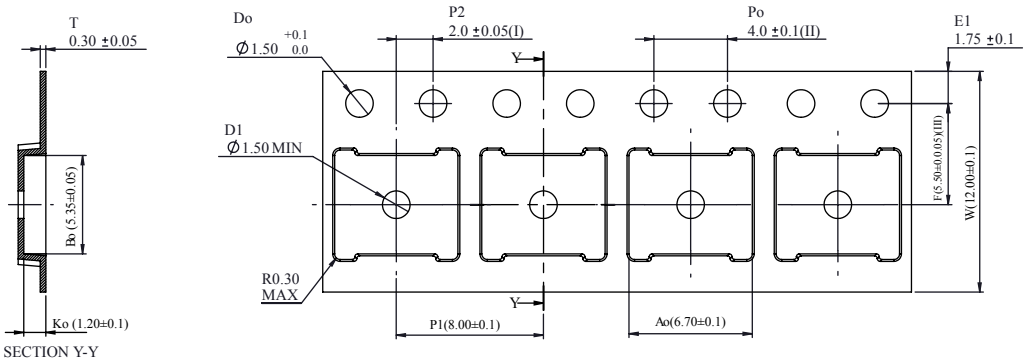
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55		0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

Figure 19. PowerFLAT 5x6 double island recommended footprint (dimensions are in mm)



4.2 PowerFLAT 5x6 WF packing information

Figure 20. PowerFLAT 5x6 WF tape (dimensions are in mm)



(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk qua ntity 3000 pcs

8234350_TapeWF_rev_C

Figure 21. PowerFLAT 5x6 package orientation in carrier tape

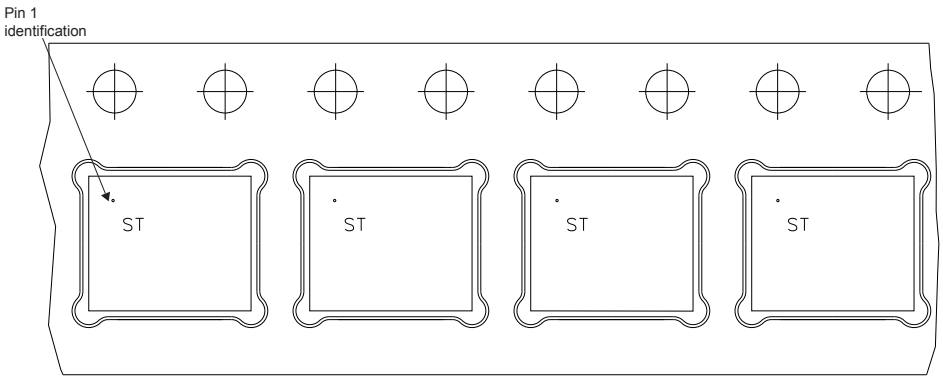
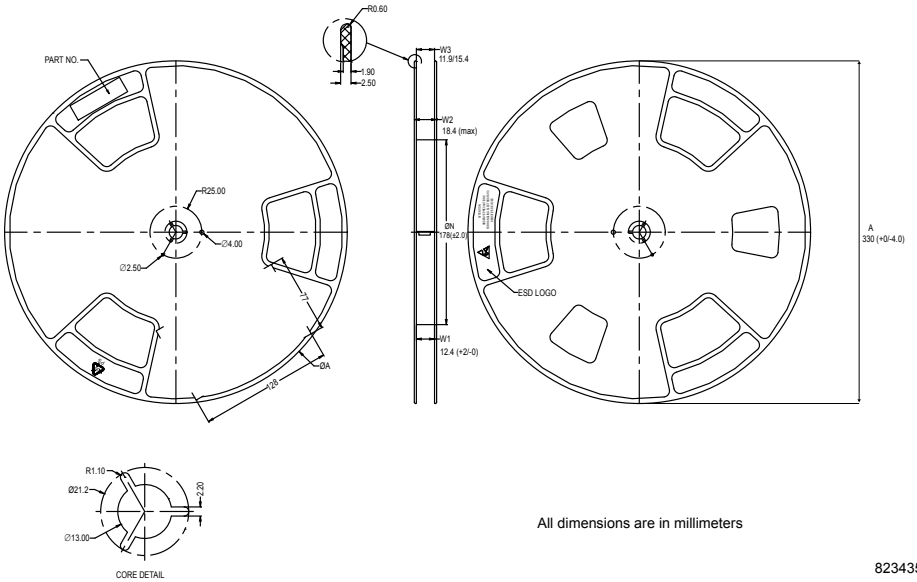


Figure 22. PowerFLAT 5x6 reel (dimensions are in mm)



All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
11-Oct-2011	1	First release.
19-Jun-2012	2	Added *Section 2.1: Electrical characteristics (curves)*. Updated *Section 4: Package mechanical data* and title on the cover page.
26-Jun-2012	3	Document status promoted from preliminary to production data.
24-Oct-2013	4	• Updated title and features in cover page • Modified: VGS(th) value in *Table 4* • Updated: *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data* • Minor text changes
20-Feb-2014	5	• Added: *Features* in cover page • Added: *note 1* in *Table 1* • Added: *Table 20* and *Table 9* • Added: *Figure 23* • Minor text changes
11-May-2017	6	Updated title and description on cover page. Updated *Figure 6: "Normalized V(BR)DSS vs. temperature"* and *Figure 11: "Normalized on-resistance vs. temperature"*. Updated *Section 4: "Package information"* Minor text changes
04-Mar-2020	7	Updated Section 4 Package information. Minor text changes.

Contents