REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE F8859. Add case outline Y. Add device type 02. Add section 1.5, radiation features. Make changes to table III, delta limits. Update the boilerplate to add radiation hardness assurance requirements, to remove classes B and S criteria, and to reflect the changes in accordance with MIL-PRF-38535 requirements. Editorial changes throughout. - jak	04-05-24	Thomas M. Hess

REV																			
SHEET																			
REV	A	A	A	A	A	A	A												
SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
93-02-23

REVISION LEVEL
A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, 16-BIT BUS DRIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-92022**

SHEET 1 OF 21

DSCC FORM 2233
APR 97

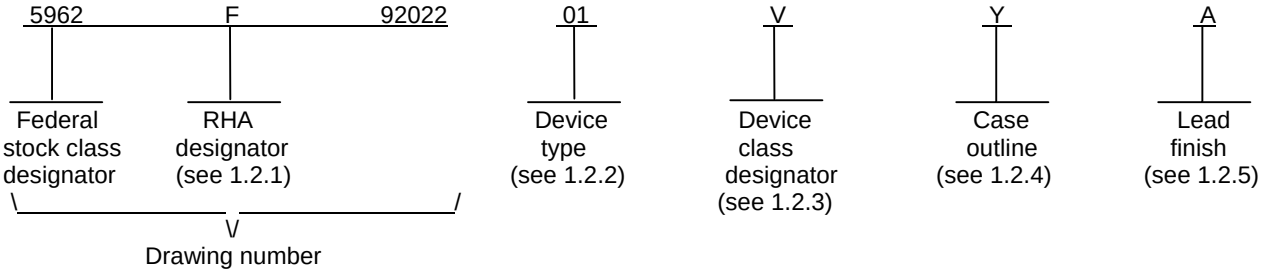
5962-E079-04

`

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example.



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT16244	16-bit bus driver with three-state outputs, TTL compatible inputs
02	54ACT16244	16-bit bus driver with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDFP1-48	48	Flat pack
Y	See figure 1	48	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
Output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Input clamp current (I_{IK}) (V_{IN} < 0 V, V_{IN} > V_{CC})	±20 mA
DC output diode current (I_{OK}) (V_{OUT} < 0 V, V_{OUT} > V_{CC})	±50 mA
DC output current (I_{OUT}) (V_{OUT} = 0 to V_{CC}) (per output pin)	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±400 mA 3/
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case outline X	See MIL-STD-1835
Case outline Y	22°C/W
Junction temperature (T_J)	+175° C
Case operating temperature range (T_C)	-55°C to +125°C

1.4 Recommended operating conditions. 2/ 4/ 5/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input rise and fall rate (t_r, t_f) maximum:	
(10% to 90% of V_{IN}, 90% to 10% of V_{IN})	10ns/V
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+24 mA

1.5 Radiation features.

Device type 02:

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	300 krads (Si)
Single Event Latchup (SEL) or Single Event Upset (SEU)	≥ 93 MeV-cm^2/mg

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with 5004 of MIL-STD-883.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ For packages with multiple V_{CC} and GND pins, this value represents the maximum total current flowing into or out of all V_{CC} and GND pins.
4/ Unless otherwise specified, the limits for parameters listed herein shall apply over the full V_{CC} and T_C recommended operating range.
5/ Unused or floating inputs should be held high or low.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA/JEDEC Standard No. 78 - IC Latch-Up Test

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices

(Copies of these documents are available online at http://www.jedec.org or from the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Positive input clamp voltage 3022	V_{IC+}	For input under test, I_{IN} = 1.0 mA	All Q, V	GND	1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -1.0 mA	All Q, V	Open	1	-0.4	-1.5	V
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -50 µA	All All	4.5 V	1, 2, 3	4.4		V
	V_{OH2}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -50 µA	All All	5.5 V	1, 2, 3	5.4		
	V_{OH3}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -24 mA	01 All	4.5 V	1	3.94		
					2, 3	3.7		
			02 All		1, 2, 3	3.7		
	V_{OH4}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -24 mA	01 All	5.5 V	1	4.94		
					2, 3	4.7		
			02 All		1, 2, 3	4.7		
	V_{OH5} 6/	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85		
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 50 µA	All All	4.5 V	1, 2, 3		0.1	V
	V_{OL2}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 50 µA	All All	5.5 V	1, 2, 3		0.1	
	V_{OL3}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 24 mA	All Q, V	4.5 V	1, 3		0.36	
					2		0.50	
			All M		1		0.36	
					2, 3		0.50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$, $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
Low level output voltage 3007	V_{OL4}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 24 mA		All Q, V	5.5 V	1, 3		0.36	V
						2		0.50	
				All M		1		0.36	
						2, 3		0.50	
	V_{OL5} 6/	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 50 mA		All All	5.5 V	1, 2, 3		1.65	
Three-state output leakage current high 3021	I_{OZH}	$\overline{mG} = V_{IH}$ or V_{IL} V_{IH} = 2.0 V V_{IL} = 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND V_{OUT} = 5.5 V		All Q, V	5.5 V	1		0.5	µA
						2		10.0	
				All M		1		0.5	
						2, 3		10.0	
			M, D, P, L, R, F	02 Q, V		1		10.0	
Three-state output leakage current low 3020	I_{OZL}	$\overline{mG} = V_{IH}$ or V_{IL} V_{IH} = 2.0 V V_{IL} = 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND V_{OUT} = GND		All Q, V	5.5 V	1		-0.5	µA
						2		-10.0	
				All M		1		-0.5	
						2, 3		-10.0	
			M, D, P, L, R, F	02 Q, V		1		-10.0	
Input current high 3010	I_{IH}	For input under test $V_{IN} = V_{CC}$ For all other inputs $V_{IN} = V_{CC}$ or GND		All Q, V	5.5 V	1		0.1	µA
						2		1.0	
				All M		1		0.1	
						2, 3		1.0	
Input current low 3009	I_{IL}	For input under test V_{IN} = GND For all other inputs $V_{IN} = V_{CC}$ or GND		All Q, V	5.5 V	1		-0.1	µA
						2		-1.0	
				All M		1		-0.1	
						2, 3		-1.0	
Input capacitance 3012	C_{IN}	See 4.4.1c T_C = +25°C		All All	GND	4		9.0	pF
Output capacitance 3012	C_{OUT}	See 4.4.1c T_C = +25°C		All All	5.0 V	4		27.0	pF
Power dissipation capacitance per buffer/driver	C_{PD} 7/	See 4.4.1c, T_C = +25°C f = 1 MHz C_L = 50 pF Any one mAn input switching	Outputs enabled	01 All	5.0 V	4		48.75	pF
			Outputs disabled	01 All	5.0 V	4		13.75	
				02 All	5.0 V	4		48.75	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$, $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 8/	For input under test, $V_{IN} = V_{CC} - 2.1\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND	01 Q, V	5.5 V	3		0.9	mA
					1, 2		1.0	
			01 M		1		0.9	
					2, 3		1.0	
			02 All	5.5 V	1, 2, 3		1.6	
Quiescent supply current, output high 3005	I_{CCH}	$\overline{mG}$ = GND For all inputs, $V_{IN} = V_{CC}$ or GND	01 Q, V	5.5 V	1		2.0	µA
					2		40.0	
			02 Q, V	5.5 V	1		4.0	µA
					2		160.0	
			All M		1		8.0	
					2, 3		160.0	
		M, D, P, L, R, F 9/	02 Q, V		1		50.0	
Quiescent supply current, output low 3005	I_{CCL}	$\overline{mG}$ = GND For all inputs, $V_{IN} = V_{CC}$ or GND	01 Q, V	5.5 V	1		2.0	µA
					2		40.0	
			02 Q, V	5.5 V	1		4.0	µA
					2		160.0	
			All M		1		8.0	
					2, 3		160.0	
		M, D, P, L, R, F 9/	02 Q, V		1		50.0	
Quiescent supply current, output three-state 3005	I_{CCZ}	$\overline{mG} = V_{CC}$ For all inputs, $V_{IN} = V_{CC}$ or GND	01 Q, V	5.5 V	1		2.0	µA
					2		40.0	
			02 Q, V	5.5 V	1		4.0	µA
					2		160.0	
			All M		1		8.0	
					2, 3		160.0	
		M, D, P, L, R, F 9/	02 Q, V		1		50.0	
Low level ground bounce noise	V_{GBL} 10/ 11/	$V_{LD} = 2.5\ V$ $I_{OL} = +24\ mA$ See figure 5	01 Q, V	4.5 V	4		2000	mV
			02 Q, V				1000	
High level ground bounce noise	V_{GBH} 10/ 11/	$V_{LD} = 2.5\ V$ $I_{OH} = -24\ mA$ See figure 5	01 Q, V	4.5 V	4		2000	mV
			02 Q, V				800	
Latch-up input/output over-voltage	I_{CC} (O/V1) 12/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCO} = 5.5\ V$, $V_{over} = 10.5\ V$	All Q, V	5.5 V	2		200	mA
Latch-up input/output positive over-current	I_{CC} (O/I1+) 12/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCO} = 5.5\ V$, $I_{trigger} = +120\ mA$	All Q, V	5.5 V	2		200	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Latch-up input/output negative over-current	I_{CC} (O/I1-) 12/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = -120\ mA$	All Q, V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 12/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$	All Q, V	5.5 V	2		100	mA
Functional tests 3014	13/	$V_{IL} = 0.8\ V$, $V_{IH} = 2.0\ V$ Verify output V_{OUT} See 4.4.1d	All All	4.5 V	7, 8	L	H	
			All M	5.5 V	7, 8	L	H	
Propagation delay time, mAn to mYn 3003	t_{PLH} 14/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 6	01 All	4.5 V and 5.5 V	9	4.0	8.5	ns
					10, 11	3.0	10.3	
			02 All	4.5 V and 5.5 V 15/	9	2.0	8.5	
					10, 11	2.0	10.3	
	t_{PHL} 14/		01 All	4.5 V and 5.5 V	9	3.4	8.7	ns
					10, 11	3.4	10.1	
			02 All	4.5 V and 5.5 V 15/	9	2.0	8.7	
					10, 11	2.0	10.1	
Propagation delay time, output enable, mG to mYn 3003	t_{PZH} 14/		01 All	4.5 V and 5.5 V	9	3.0	8.1	ns
					10, 11	3.0	10.5	
			02 All	4.5 V and 5.5 V 15/	9	2.0	8.1	
					10, 11	2.0	10.5	
	t_{PZL} 14/		01 All	4.5 V and 5.5 V	9	3.7	9.3	ns
					10, 11	3.7	11.0	
			02 All	4.5 V and 5.5 V 15/	9	2.0	9.3	
					10, 11	2.0	12.5	

See footnotes at the end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Propagation delay time, output disable, mG to mYn 3003	t_{PHZ} 14/	C_L = 50 pF minimum R_L = 500Ω See figure 6	01 All	4.5 V and 5.5 V	9	5.4	11.5	ns
					10, 11	5.4	13.0	
			02 All	4.5 V and 5.5 V 15/	9	2.0	11.5	
					10, 11	2.0	13.0	
	t_{PLZ} 14/		01 All	4.5 V and 5.5 V	9	5.0	9.5	ns
					10, 11	5.0	10.9	
			02 All	4.5 V and 5.5 V 15/	9	2.0	9.5	
					10, 11	2.0	10.9	

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.
b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.
c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 02 meet all levels M, D, P, L, R, and F of irradiation. However, these parts are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = 25°C.

4/ The word "All" in the device type and device class column, means limits for all device types and classes.

5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

6/ Transmission driving tests are performed at V_{CC} = 5.5 V with a 10 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V. For device class M, values for subgroup 1 shall be guaranteed, if not tested, to the limits specified in table I.

7/ Power dissipation capacitance (C_{PD}) determines the no load power consumption,
$P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})\, f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$ and the dynamic current consumption,
$I_S = (C_{PD} + C_L)\, V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$. For both P_D and I_S, n is the number of device inputs at TTL levels; f is the frequency of the input signal; and d is the duty cycle of the input signal.

8/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather 0 V to V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate method, the maximum limit is equal to the number of inputs at a high TTL input level times ΔI_{CC} max, and the preferred method and limits are guaranteed.

TABLE I. Electrical performance characteristics - Continued.

9/ The maximum limit for this parameter at 100 krads (Si) is 4 μA.

10/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} maximum = ±24 mA, for example) and 50 pF of load capacitance (see figure 5). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f = 3.5 \pm 1.5$ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 MΩ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (see figure 5). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

11/ When used in asynchronous TTL compatible systems, ground bounce (V_{GBL} and V_{GBH}) = 2000 mV can be a possible problem.

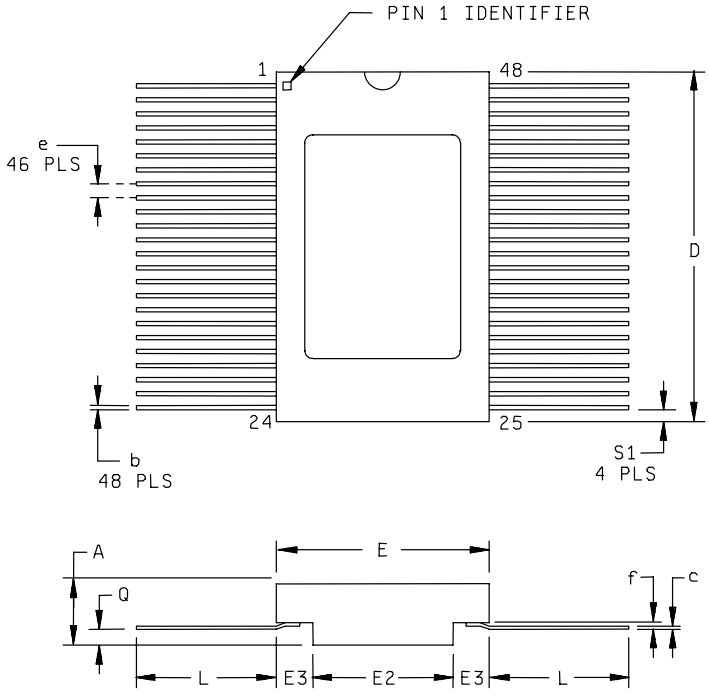
12/ See EIA/JEDEC STD. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ±5 percent (see 4.4.1b).

13/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances in accordance with MIL-STD-883 for the input voltage levels may be incorporated. For outputs, H ≥ 2.5 V, L < 2.5 V. For functional testing, the outputs shall have, at a minimum, the same loading conditions as the ac tests (see figure 6).

14/ For propagation delay tests, all paths must be tested.

15/ The AC parameter at V_{CC} = 5.5 V shall be guaranteed, if not tested, to the limits specified in table I.

Case outline Y



Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.086	.107	2.18	2.72
b	.008	.012	0.20	0.30
c	.005	.007	0.12	0.18
D	.613	.627	15.57	15.92
E	.375	.385	9.52	9.78
E2	.245	.255	6.22	6.48
E3	.060	.070	1.52	1.78
f	.008 BSC		0.20 BSC	
e	.025 BSC		0.635 BSC	
L	.270	.370	6.85	9.40
Q	.026	.036	0.66	0.92
S1	.010	.024	0.25	0.61
N	48		48	

FIGURE 1. Case outline.

Device types	01, 02		
Case outlines	X, Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{1G}$	25	$\overline{3G}$
2	1Y1	26	4A4
3	1Y2	27	4A3
4	GND	28	GND
5	1Y3	29	4A2
6	1Y4	30	4A1
7	V_{CC}	31	V_{CC}
8	2Y1	32	3A4
9	2Y2	33	3A3
10	GND	34	GND
11	2Y3	35	3A2
12	2Y4	36	3A1
13	3Y1	37	2A4
14	3Y2	38	2A3
15	GND	39	GND
16	3Y3	40	2A2
17	3Y4	41	2A1
18	V_{CC}	42	V_{CC}
19	4Y1	43	1A4
20	4Y2	44	1A3
21	GND	45	GND
22	4Y3	46	1A2
23	4Y4	47	1A1
24	$\overline{4G}$	48	$\overline{2G}$

Terminal symbol description	
Terminal Symbol	Description
mAn (m = 1 to 4, n = 1 to 4)	Data inputs
$\overline{mG}$ (m = 1 to 4)	Output enable control inputs
mYn (m = 1 to 4, n = 1 to 4)	Outputs (non-inverting)

FIGURE 2. Terminal connections.

Inputs		Output
$\overline{mG}$	mAn	mYn
L	H	H
L	L	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance

FIGURE 3. Truth table.

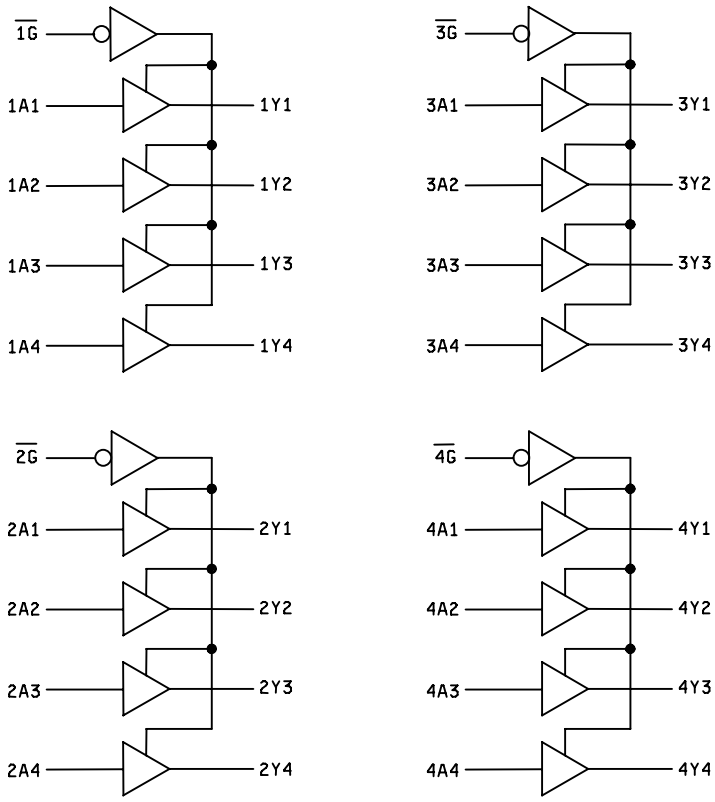
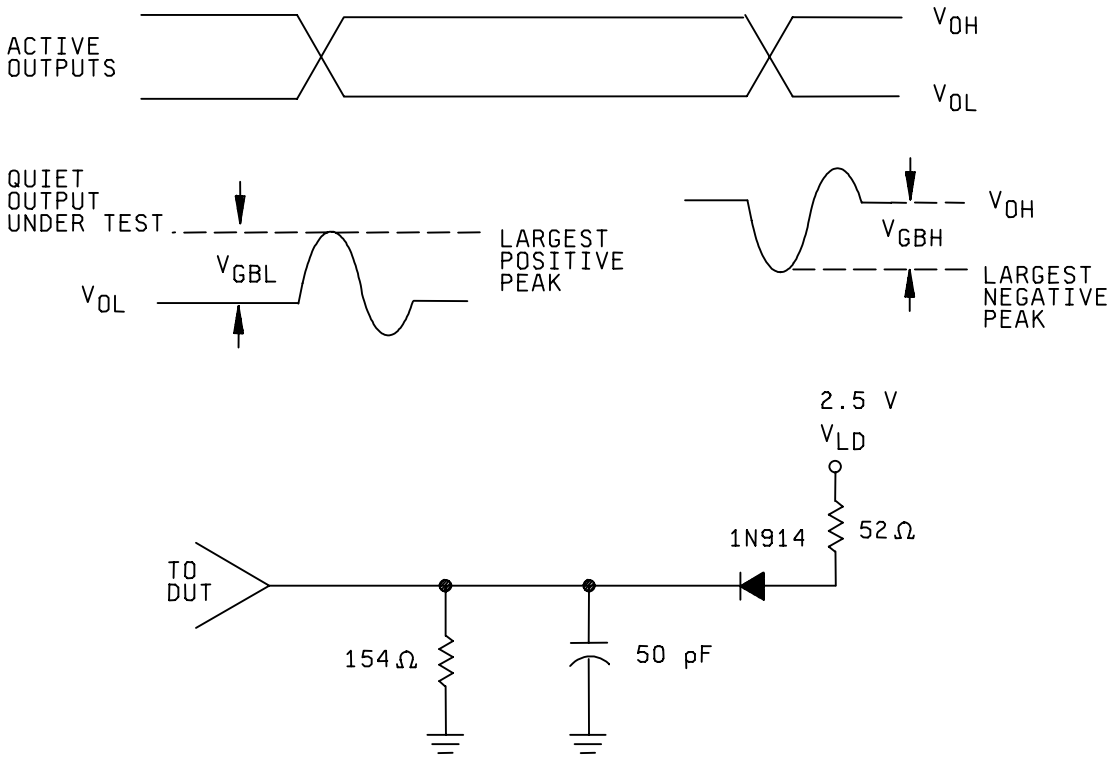


FIGURE 4. Logic diagram.



NOTE: Resistor and capacitor tolerances = ±10%.

FIGURE 5. Ground bounce waveforms and test circuit.

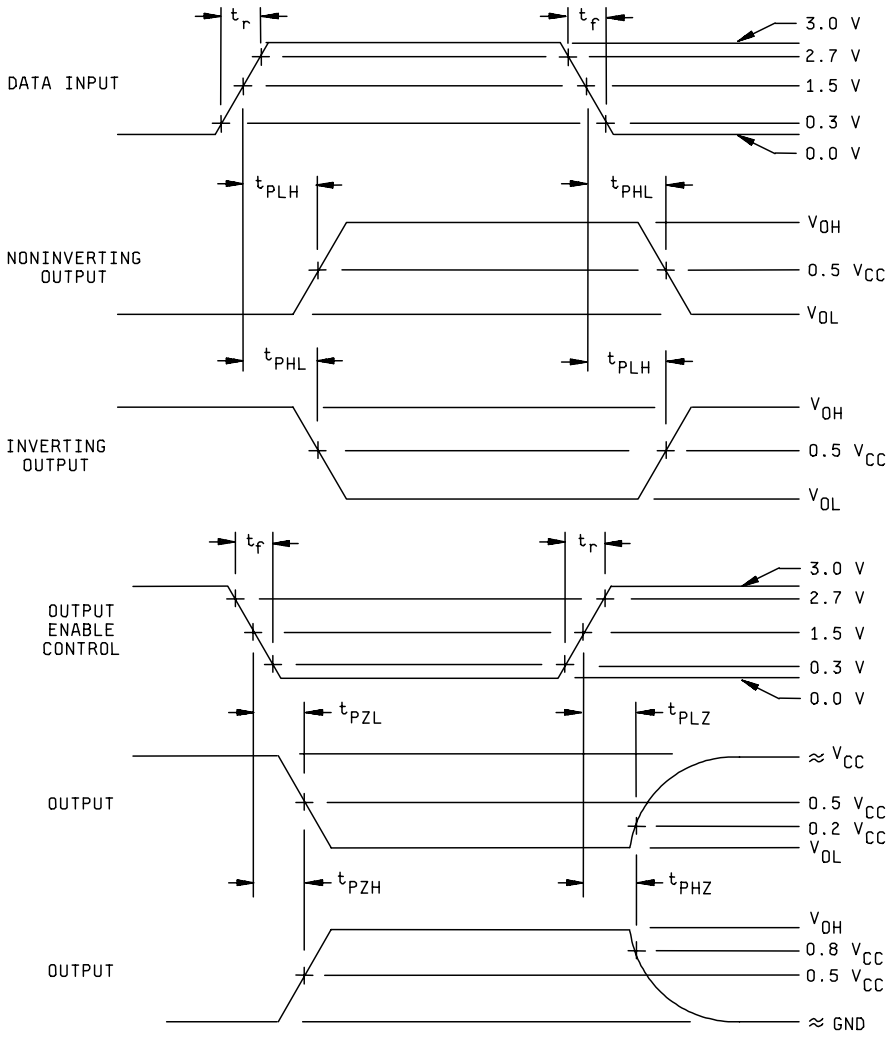
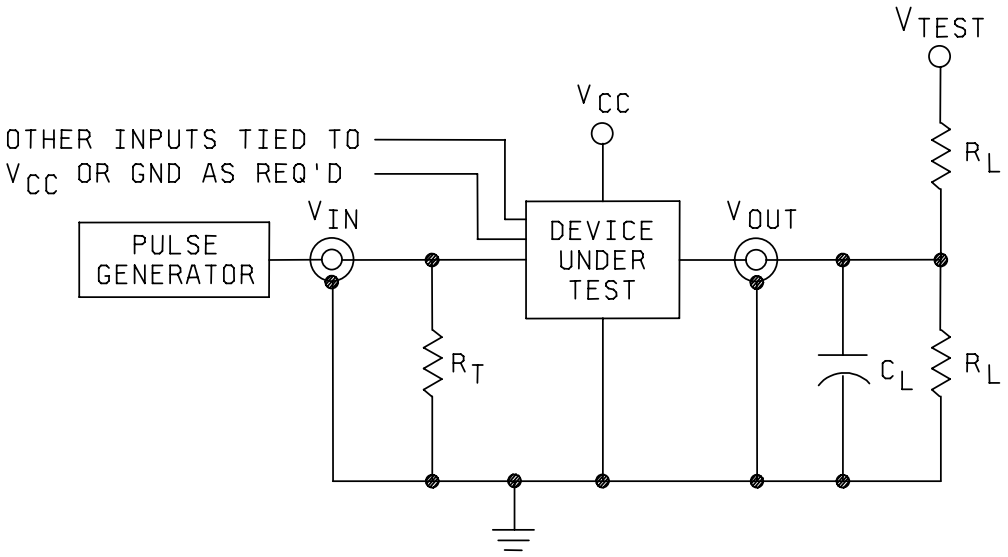


FIGURE 6. Switching waveforms and test circuit .



NOTES:

1. When measuring t_{PHZ} and t_{PZH}: V_{TEST}= GND.
2. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X $V_{CC.}$
3. When measuring t_{PLH} and t_{PHL}: V_{TEST} = open.
4. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
5. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
6. R_T = 50Ω or equivalent. R_L = 500Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. Outputs are measured one at a time with one output per measurement.

FIGURE 6. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Latch-up and ground bounce tests are required for device classes Q and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground-bounce tests, test all applicable pins on five devices with zero failures.

c. C_{IN}, C_{OUT}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	3/ 1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table III, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device types	Delta limits
Supply current	I_{CCH}, I_{CCL}, I_{CCZ}	01	±100 nA 2/
		02	±300 nA
Supply current delta	ΔI_{CC}	02	±0.4 mA
Input current low level	I_{IL}	02	±20 nA
Input current high level	I_{IH}	02	±20 nA
Output voltage low level (V_{CC} = 5.5 V, I_{OL} = 24 mA)	V_{OL}	02	±0.04 V
Output voltage high level (V_{CC} = 5.5 V, I_{OH} = -24 mA)	V_{OH}	02	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ This limit may not be production tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. RHA tests for device classes M, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

b. Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on classes M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE

DATE: 04-05-24

Approved sources of supply for SMD 5962-92022 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9202201MXA	01295	SNJ54ACT16244WD
5962-9202202QYC	F8859	54ACT16244K01Q
5962-9202202QYA	F8859	54ACT16244K02Q
5962-9202202VYC	F8859	54ACT16244K01V
5962-9202202VYA	F8859	54ACT16244K02V
5962F9202202QYC	F8859	RHFACT16244K01Q
5962F9202202QYA	F8859	RHFACT16244K02Q
5962F9202202VYC	F8859	RHFACT16244K01V
5962F9202202VYA	F8859	RHFACT16244K02V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84 M/S 853 Sherman, TX 75090-9493
F8859	ST Microelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2 - France

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