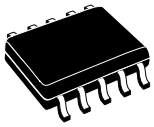
HVLED001

Offline controller for LED lighting with constant voltage primary-sensing and high power factor

Datasheet - production data



SSOP10

Features

- Quasi-resonant (QR) topology
- Primary side regulation of output voltage
- Direct optocoupler connection for current loop regulation with feedback disconnection detection and disable
- 800 V high voltage start-up
- High power factor and low THD in universal range
- High efficiency and output stability in wide voltage and current range
- Low start-up and quiescent current
- Programmable minimum off time
- Integrated input voltage detection for high power factor capability and protection triggering
- Latch free device guarantee by smart autoreload timer (ART)
- 0 - 10 and PWM dimming compatible
- Remote control pin

Applications

- Single stage LED drivers with high power factor up to 75 W
- Two stages LED drivers up to 150 W

Description

The HVLED001 is an enhanced peak current mode controller capable of controlling mainly high power factor (HPF) flyback or buck-boost topologies in LED drivers having an output power up to 150 W. Some other topologies, like buck, boost and SEPIC can also be implemented.

ST's innovative high voltage technology allows direct connection of the HVLED001 to the input voltage in order to both start up the device and monitor the input voltage without the need for external components.

Advanced features are embedded to control either the output voltage or output current precisely and reliably using a reduced number of components, mainly passive. Startup and light-load conditions are managed by dedicated operating schemes to improve the quality of output variable regulation in the final application. Abnormal conditions such as open circuit, output short-circuit, input overvoltage/undervoltage, and circuit failures such as open loop and overcurrent of the main switch are effectively controlled.

A smart auto-recover timer (ART) function is built in to guarantee automatic application recovery, without loss of reliability.

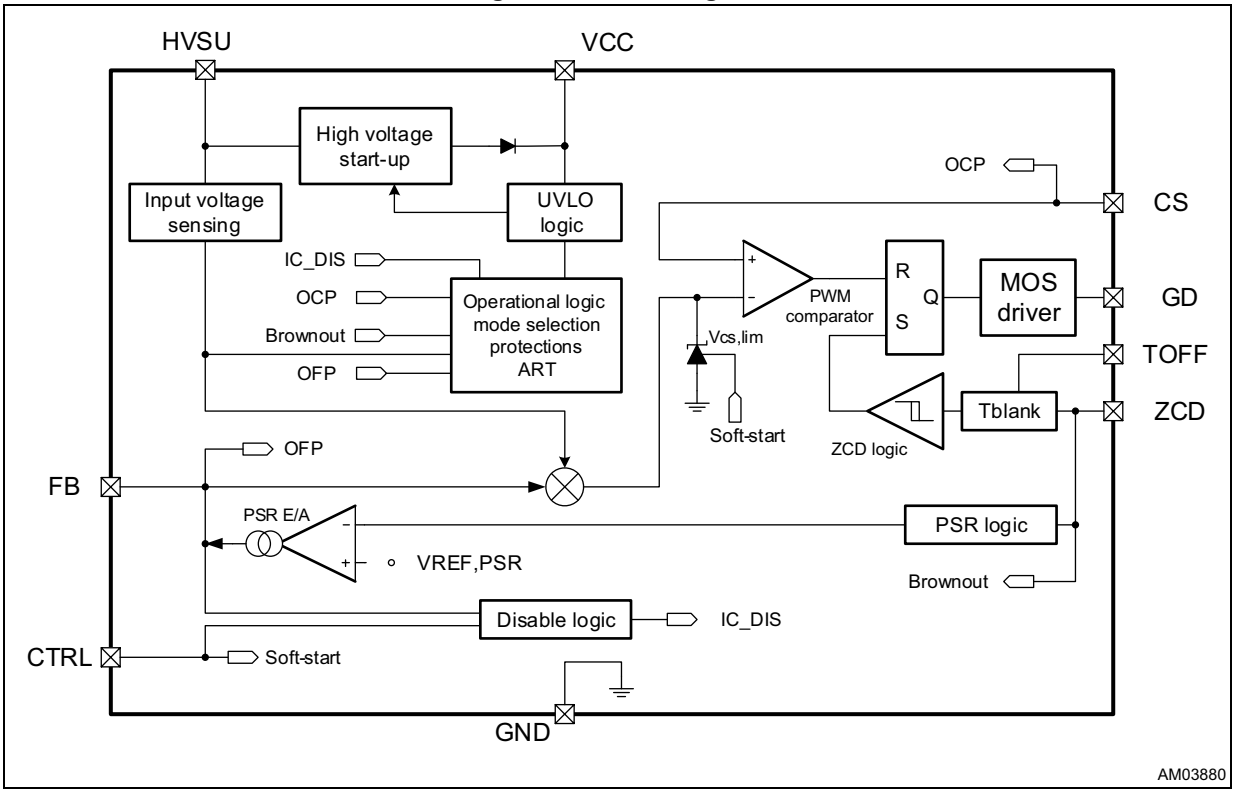
Table 1. Device summary

Order code	Package	Packaging
HVLED001	SSOP10	Tube
HVLED001TR		Tape and reel

Contents

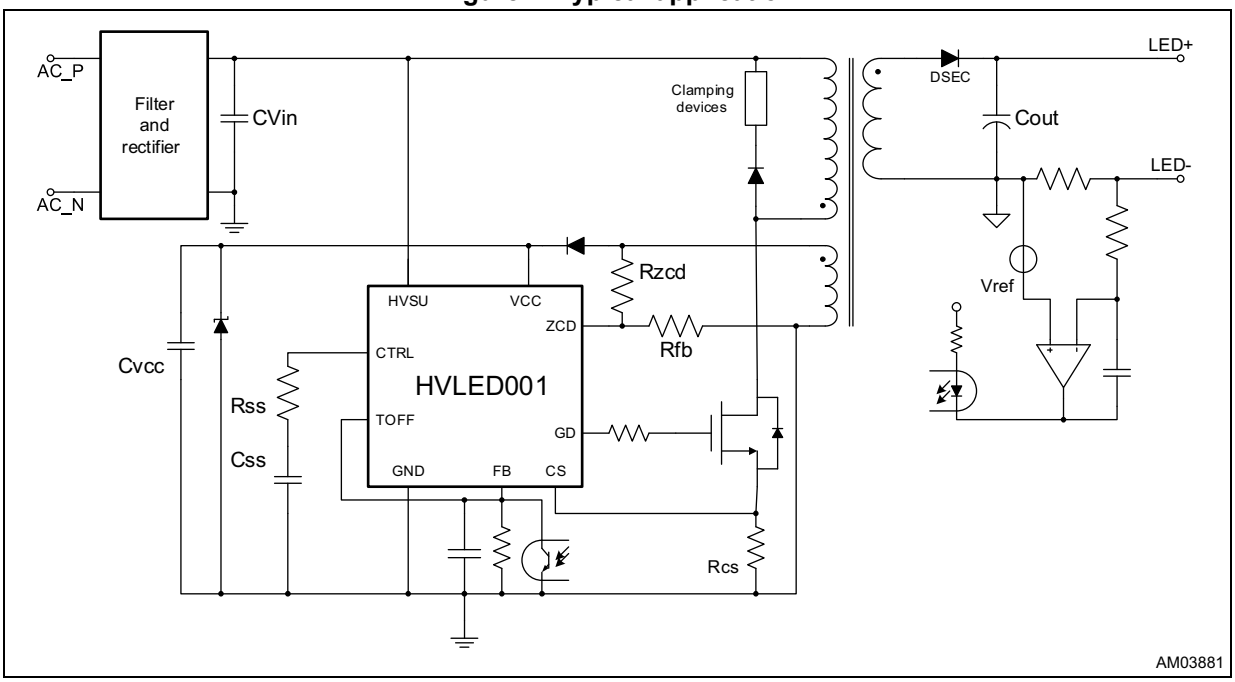
1 Block diagram

Figure 1. Block diagram



2 Typical application - HPF flyback

Figure 2. Typical application



3 Pin settings

Figure 3. Pin connection

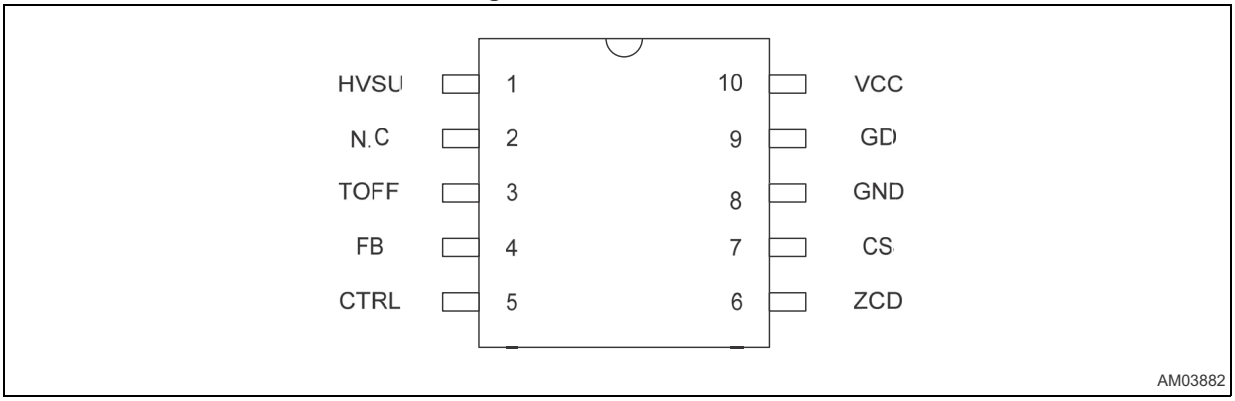


Table 2. Pin description

Symbol	Pin	Description
HVSU	1	High voltage start-up and input voltage detection. The pin, able to withstand 800 V, is to be tied to the input voltage using a low value resistor (1 kΩ typ.). It embeds the internal start-up unit that charges the capacitor connected between the V_{CC} pin and GND pin during the start-up and low consumption. During the operational mode, the voltage at this pin is used to both measure the input voltage and detect input overvoltages.
N.C.	2	Not connected pin.
TOFF	3	A blanking time for zero voltage detection can be set applying a voltage to this pin. A minimum blanking time is obtained leaving the pin unconnected.
FB	4	Input for loop regulation. The pin is intended to be directly driven by the phototransistor (emitter-grounded) of an optocoupler and / or to the compensation network related to the output voltage primary side regulation loop. An upper threshold VOFP detects a failure of the optocoupler. The burst-mode and disable conditions are also related to the voltage applied to this pin.
CTRL	5	This pin is used to disable the IC and generate the soft-start ramp. External active circuitry can be used to turn off the application.
ZCD	6	Multiple function pin able to detect the zero current instant, to sense the output voltage for primary side regulation and the input voltage for brownout detection. A negative-going edge triggers the MOSFET's turn on, while an internal starter unit is active to generate the triggering signal when not externally available (e.g.: start-up).
CS	7	Input to the current sense comparator for the power regulation. A second level overcurrent (OCP) threshold detects abnormal currents (e.g.: due to transformer's saturation) and, on this occurrence, activates the second level overcurrent protection procedure.
GND	8	Reference pin.

Table 2. Pin description (continued)

Symbol	Pin	Description
GD	9	Gate driver output. The output stage is able to drive the power MOSFET's and IGBT's gate.
VCC	10	Supply voltage of the IC. Internal UVLO logic prevents the operation at voltages that are insufficient for an efficient gate driving or signal processing. Both a bulk capacitor (typically around 10 µF) and a high frequency filter capacitor (100 nF ceramic, mounted as close as possible to the device) are connected between this pin and GND. Internal clamp structure prevents accidental low energy spikes damaging the device.

4 Electrical data

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
VHVSU,bd	HVSU	HVSU breakdown voltage	IHVSU < 100 µA, DC VCC = 15 V	800		V
VHVSU,neg	HVSU	HVSU negative voltage	IHVSU source < 2 mA	- 0.3		V
VGD	GD	Maximum swing voltage		- 0.3	V_{CC}	V
VCS	CS	Current sense applied voltage		- 0.3	7	V
VZCD	ZCD	ZCD pin voltage			7	V
			Negative, Isource < 1 mA	- 0.3		V
VFB	FB	FB voltage		- 0.3	3.6	V
VCTRL	CTRL	CTRL voltage		- 0.3	V_{CC}	V
VCC,MAX	VCC	IC supply voltage			18	V
VTOFF	TOFF	Maximum applied voltage		- 0.3	7	V

Note: Where not otherwise indicated the AMR are intended when $V_{CC} > V_{CC,on}$. When $V_{CC} < V_{CC,on}$ the minimum between the indicated value and V_{CC} + 0.3 V has to be considered.

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	120	°C/W
T_J	Junction temperature operating range	-40 to 125	°C
T_{stg}	Storage temperature range	-55 to 150	°C

5 Electrical characteristics

$T_j = T_a$ = 25 °C production tested, V_{CC} = 15 V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage							
V_{CC}	VCC	Operating range	After turn on(1)	9.7		18	V
$V_{CC,on}$	VCC	Turn on threshold	(2)	12	13	14	V
$V_{CC,su}$	VCC	Low consumption mode activation	Low consumption mode(2)	8.8	9.2	9.7	V
			Start-up	2.2	3	3.8	V
$V_{CC,shd}$	VCC	V_{CC} for IC reset	Low consumption(2)	7.8	8.5	9.2	V
Supply current							
Istart-up	VCC	Start-up current	Start-up, $V_{CC} < V_{CC,on}$		125	250	µA
ICC	VCC	Operating supply current	Stop mode, FB < VFB,dis		2.6	4	mA
			See *Figure 4: Graph 1: V_{CC} current consumption on page 13*				
Iq	VCC	Quiescent current	Low consumption mode, CTRL < VCTRL,dis		330	480	µA
High voltage start-up generator							
VHV	HVSU	Breakdown voltage	IHV < 100 µA	800			V
VHV,op	HVSU	Operating voltage range	(1)			VHV	V
VHVstart	HVSU	Start voltage	IV_{CC} < 100 µA	40	46	55	V
Icharge,su	VCC	Initial charging current	VHVSU > VHvstart, V_{CC} < 2 V	0.15	0.5	0.9	mA
Icharge	VCC	V_{CC} charge current	VHVSU > VHvstart, start-up, $V_{CC} < V_{CC,on}$	2	3.4	5	mA
IHV, ON	HVSU	ON-state current	VHVSU > VHvstart, V_{CC} < 2 V	0.2	0.7	1.1	mA
			VHVSU > VHvstart, start-up, $V_{CC} < V_{CC,on}$	2.3	4	6	
IHV, OFF	HVSU	OFF-state leakage current	VHVSU = 400 V, active mode		18	35	µA
Input voltage sensing							
Vsurge	HVSU	Surge protection threshold	(3)		540		V
Tsurge	HVSU	Max. stop state duration after surge	VHVSU > Vsurge(4)	9	10	11	ms
Feedback input							
VFB	FB	FB pin regulation voltage range	Active mode(1)	1.085		2.8	V
VFB,ref	FB	FB reference voltage	Active mode(5), (6)		1		V

Table 5. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
kp	FB	Multiplier gain	Active mode, VFB = 2.8 V, VHVSU = 300 V[6]	0.355	0.4	0.445	
VFB,dis	FB	IC disabling threshold from FB	Falling edge	0.35	0.5	0.75	V
IFBsrc	FB	FB pin pull-up current	Active mode, VZCD,off = 2.0 V, VFB = 1.65 V		1		mA
			Low consumption VFB = 0.7 V[3]	40	75	120	µA
IFBsnk	FB	FB pull down current	Active mode, VZCD,off = 2.7 V, VFB = 1.65 V[3]	90	230	350	µA
VBm	FB	Burst-mode threshold	Active mode[5]	0.97	1.054	1.11	V
Tbm	FB	Burst-mode repetition rate	VFB = 0.8 V[4]	0.94	1.04	1.16	ms
VOFP	FB	Optocoupler failure protection threshold	Active mode[5]	2.75	2.95	3.5	V
TOFP	FB	Max. active mode duration after FB clamping	VFB > VFB,max[4]	90	100	110	ms
PSR function							
VREF,PSR	FB	PSR loop reference	Tamb = 25 °C[7]	2.55	2.6	2.65	V
			Over all temperature range[3], [7]	2.5	2.6	2.7	
gm	FB	Transconductance	ΔIFB = ±10 µA, VFB = 1.65 V[3]	1.3	2.3	3.2	mS
Current sense input[8]							
VCS,lim	CS	Current sense reference clamp	VHVSU = DC voltage, VFB = 3.3 V, 1.9 V < VCTRL < 2.4 V		746		mV
VCS,min	CS	Current sense minimum level	VHVSU,pk = 400 V[3]		60		mV
			VHVSU,pk = 130 V[3]		20		
ICS	CS	Current sense pin bias current	VCS = 500 mV[3]		2.5	5	µA
TLEB	CS	Leading edge blanking		130	200	340	ns
VOCP	CS	Saturation protection threshold	During Ton	1	1.1	1.2	V
TOCP	CS	Max. stop state duration after OCP	tpulse = 1 µs, amplitude 2 V[4]	0.94	1.04	1.16	ms
VCS_SS	CS	VCS during SS	VCTRL = 0.7 V	280	348	450	mV
			VCTRL = Vctrl,bias		VCS,lim		
ZCD input							
VZCD,arm	ZCD	ZCD arming threshold	Positive-going edge[7]	0.42	0.5	0.6	V
VZCD,trig	ZCD	ZCD triggering threshold	Negative-going edge[7]	0.24	0.3	0.38	V
TBLANK	ZCD	ZCD blanking time	VTOFF > VTOFF,fix[3], [9]		3.2		µs
			VTOFF = 0 V[9]	120	200	290	µs

Table 5. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
VZCD,cl_I	ZCD	ZCD negative clamping voltage	IZCD src = 1 mA	-230	-135		mV
IZCDb	ZCD	ZCD pin biasing current	VZCD = 0.1 to 2.6 V(3)			1	µA
IBO	ZCD	Brownout detection level	Sourcing during on time(3)		100		µA
TBO	ZCD	Brownout detection time	IZCD < IBO(4)	90	100	110	ms
Td,ZCD	ZCD	ZCD propagation delay	Measured from last VZCD,trig crossing and GD rising edge(3)		300		ns
Timing							
Trec		Recovery time after opto failure, analogue disable or brownout	(4)	2.2	2.5	2.8	s
Gate driver							
VGDH	GD	Output high voltage	IGD,source = 5 mA	14.5			V
VGDL	GD	Output low voltage	IGD,sink = 5 mA			0.1	V
Isource	GD	Output source peak current	VGD = 7.5 V(3)	0.3			A
Isink	GD	Output sink peak current	VGD = 7.5 V(3)	0.6			A
Tf	GD	Fall time	CGD = 1 nF, from 13.5 V to 1.5 V		15		ns
Tr	GD	Rise time	CGD = 1 nF, from 1.5 V to 13.5 V		30		ns
VGD,shd	GD	Maximum voltage during shutdown	Vcc < $V_{CC,shd}$, IGD = 2 mA		1	2	V
CTRL input							
VCTRL,dis	CTRL	Disabling threshold	Negative-going edge(10)	0.4	0.5	0.6	V
Vadis	CTRL	Timed disabling threshold	(10)	2.4	2.6	2.85	V
TADIS	CTRL	Max. operating interval after analog disable feature triggering	VCTRL > Vadis(4)	90	100	110	ms
Vctrl,bias	CTRL	CTRL biasing voltage	Tamb = 25 °C(10)	1.85	2.05	2.25	V
			Over whole temp. range(3)	1.75		2.35	
Ictrl,bias	CTRL	CTRL biasing current	VCTRL = 0 V	5	10	15	µA
Rctrl	CTRL	Internal parallel resistor	(11)		205		kΩ
Vctrl,pd	CTRL	Pin voltage during low consumption (power good)	Low consumption, ICTRL = 0.2 mA			0.2	V
Veoss	CTRL	End of soft-start level	(10)	1.7	1.8	1.9	V
TOFF characteristics							
VTOFF	TOFF	Operating range	(1)	GND		3.3	V
VTOFF,fix	TOFF	Minimum fixed TBLANK voltage	(3)		2		V

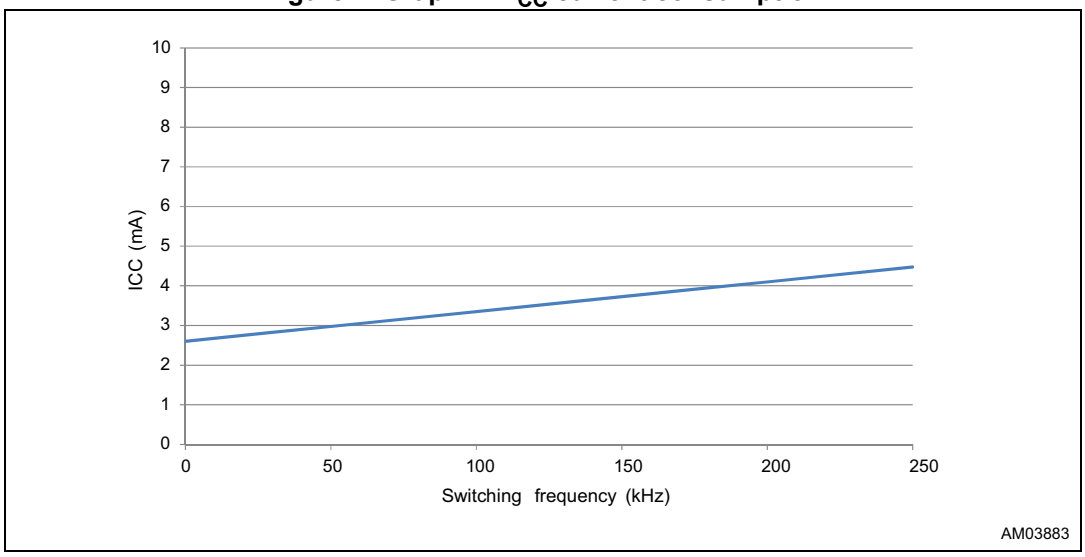
Table 5. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
koff	TOFF	TOFF characteristic slope	(3)		100		µs / V
ITOFFpu	TOFF	Pull-up current		5	12	20	µA
VTOFF,bias	TOFF	Internal bias voltage	(3)		2.4		V

1. Operating conditions not associated with specific production test.
2. Parameters in tracking group 1.
3. Parameters not tested in production.
4. Parameter calculated.
5. Parameters in tracking group 2.
6. kp parameter includes the overall tolerances of the multiplier block defined as per note *8.*
7. Parameters in tracking group 3.
8. $VCS = kp \frac{VHVSU}{VHVSU,pk}(VFB - VFB,ref) OR\ VCS,min,$ VHVSU,pk indicates the maximum value of VHVSU.
9. TBLANK = MAX {koff • (VTOFF,fix - VTOFF)}.
10. Parameters in tracking group 4.
11. VCTRL,bias/ICTRL,bias.

6 Typical electrical characteristics

Figure 4. Graph 1: V_{CC} current consumption



7 Application information

7.1 Operating modes

The HVLED001 QR flyback controller is able to operate either as a single stage high power factor (HPF) flyback controller or as a DC/DC flyback controller in dual stages topologies. Its enhanced features are mainly intended to simplify the design and the management of constant current applications (LED drivers).

Application schematics of the two main topologies are reported in *Figure 5* and *Figure 6*.

Figure 5. High power factor flyback - constant output current

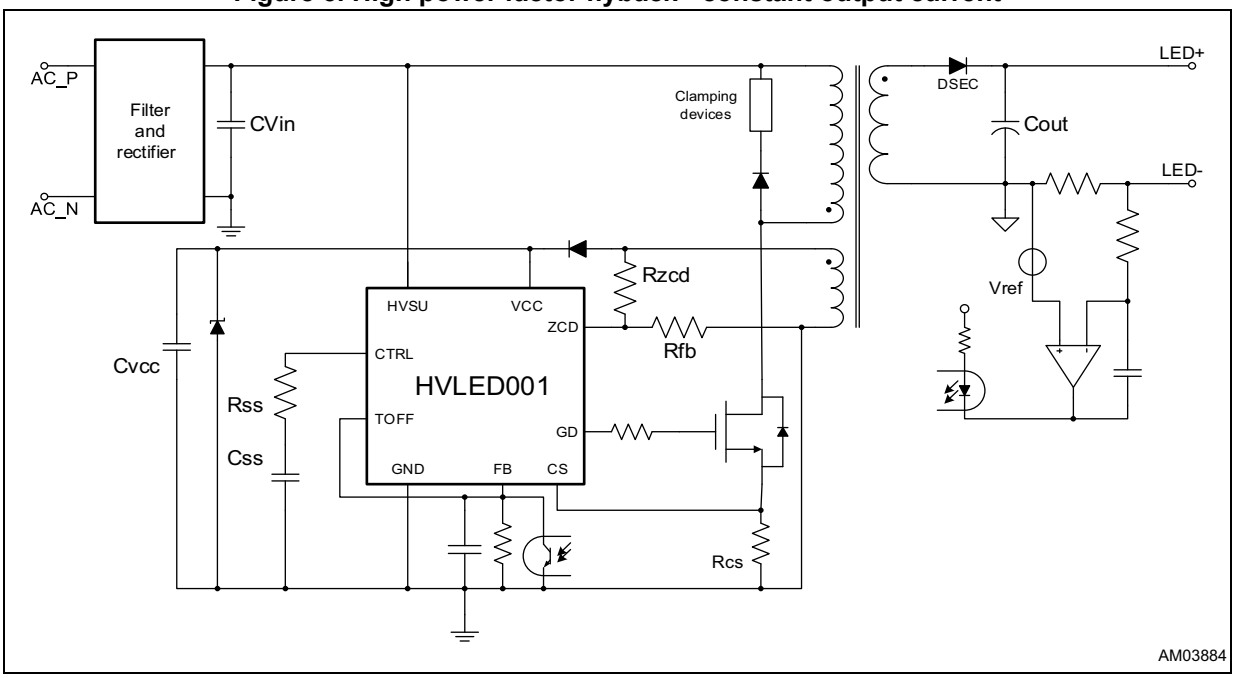
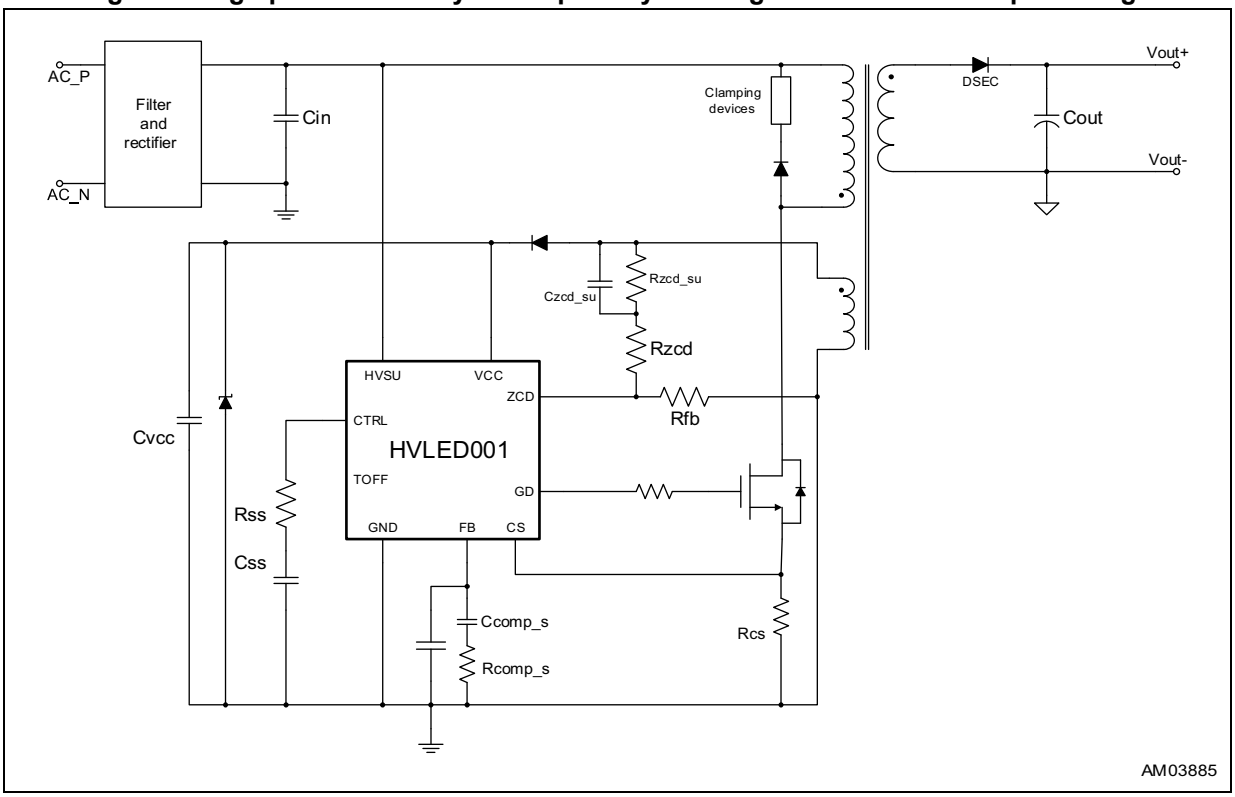


Figure 6. High power factor flyback – primary side regulated constant output voltage



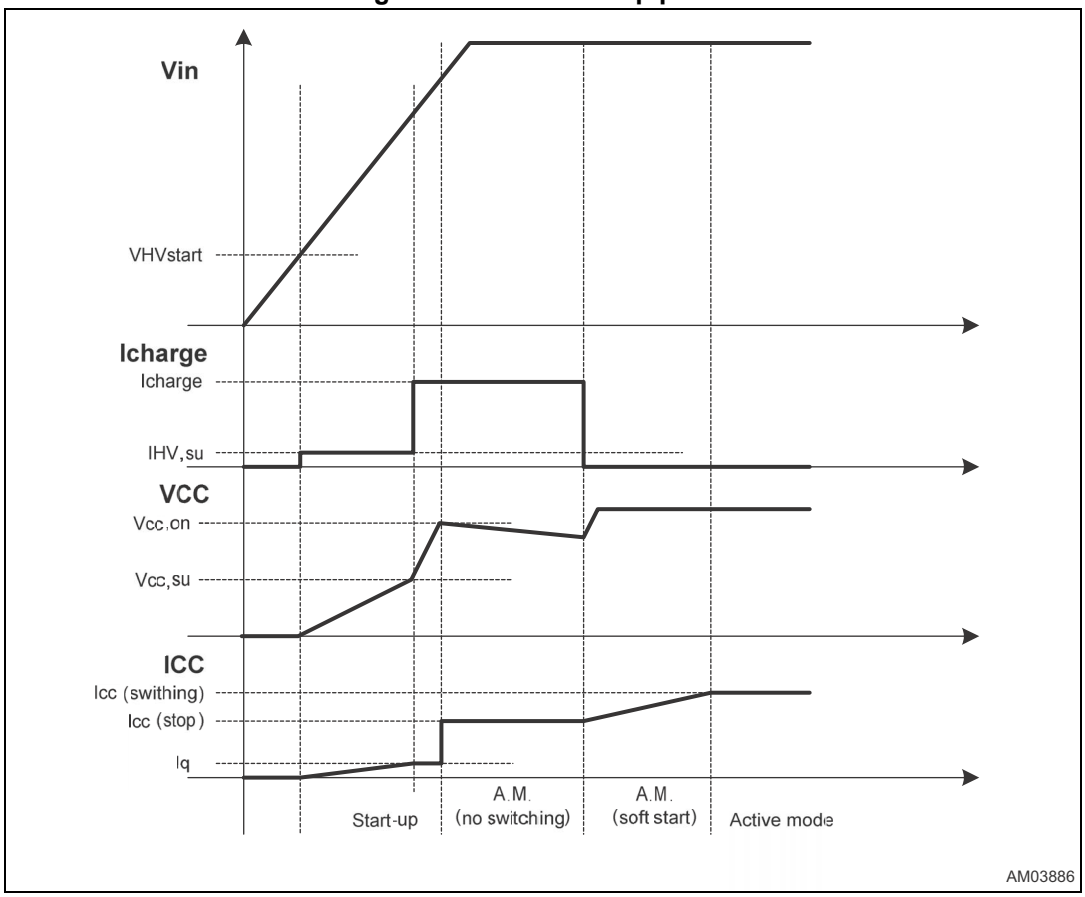
The HVLED001 has four main operating modes: the start-up mode, active mode, stop mode and low consumption mode.

7.1.1 Start-up mode

This state is entered to begin the switching activity (during application's turn on or exiting from low consumption state). The HVSU is involved into the mechanism of VCC charging; all other peripherals, except the UVLO and logic supply, are turned off to minimize the start-up time.

During this state the CTLR pin is internally pulled to ground.

Figure 7. Initial start-up phase



7.1.2 Active mode

It is the normal operational mode. During this state the external MOSFET is driven accordingly to signals coming from the application in order to regulate the desired output parameter in the closed loop (peak current control method).

The active mode is exited when abnormal conditions are present or the V_{CC} drops below the $V_{CC,su}$ threshold. The HVSU is inactive during the active mode.

7.1.3 Stop mode

This state is intended to stop the switching activity without turning off the entire function set, to quickly restart when abnormal or disabling conditions end. During this state the power consumption is not minimized and the soft-start procedure is not enabled.

7.1.4 Low consumption mode

This state is intended to stop the switching activity reducing the power consumption to a minimum level. The soft-start procedure is set to be performed when abnormal or disabling condition is removed.

During this state the VCC is kept between VCC,su and VCC,on by the high voltage start-up unit (HVSU) delivering Icharge to the output capacitor.

Note: Important: HVSU charges VCC so any other external voltage (including auxiliary winding) must be decoupled using a 1N4148 diode.

7.1.5 Soft-start

The soft-start phase is entered after the start-up and every time the IC exits from low consumption mode. This phase lasts until the voltage at the CTRL pin reaches the “end of soft-start” level (Veoss).

The current sense maximum limit is derived from this voltage, therefore the charging time of a capacitor placed between the CTRL pin and GND defines the soft-start time.

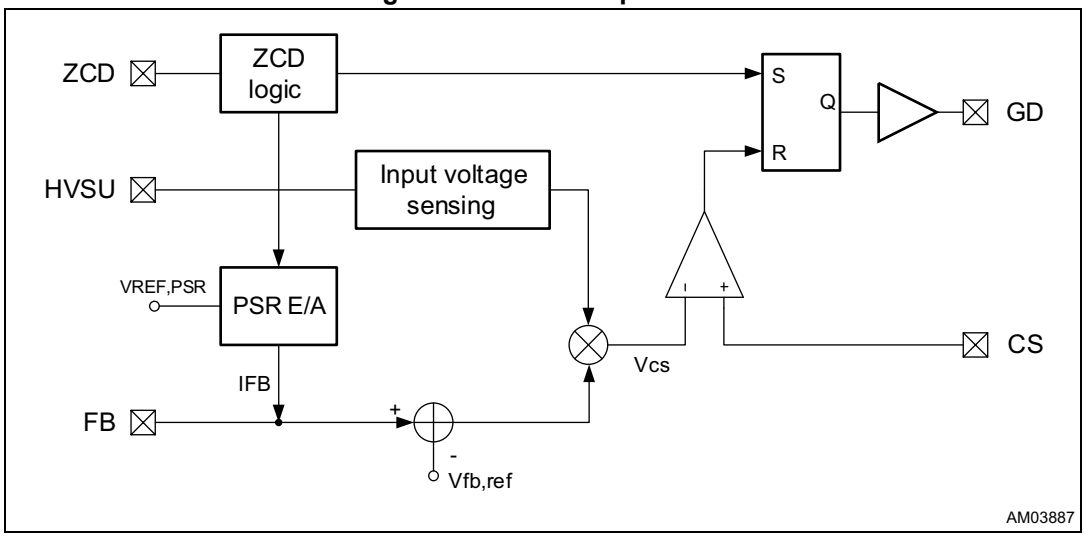
During this phase some protections (optocoupler failure protection (OFP), brownout (BO) and analog disable (AN_DIS) are ignored.

7.2 Control loop

The control loop is based on the current mode quasi-resonant flyback control scheme and is therefore performed turning off the MOSFET when the peak of its source current reaches the threshold set by the control loop, and turning the MOSFET on in correspondence of the resonant valley following the primary side demagnetization input.

A detail of the block involved into this scheme is shown in *Figure 8*.

Figure 8. Control loop blocks



7.2.1 Current sense input

The peak of the primary current is read across a shunt resistor placed between the MOSFET's source and compared with a threshold equal to:

Equation 1

$$V_{CS} + k_p \bullet \frac{V_{HVSU}}{V_{HVSU,\,pk}} \bullet (V_{FB} - V_{FB,\,ref})$$

Where the term *VHVSU,pk* is the maximum value of the HVSU voltage within around 20 ms and is used to compensate the dependency on the input voltage of the open loop gain transfer function. The gain k_p collects all the proportional terms between the HVSU voltage and CS threshold.

A leading edge blanking time (LEB) is applied after MOSFET's turn on.

The Vcs signal is upper limited to a value that depends on the CTRL voltage and is lower limited to a level defined as:

Equation 2

$$V_{CS,min} = V_{HVSU} \bullet 0.15$$

A second level OCP threshold is present to temporarily stop the switching activity in case of inductor saturation.

7.2.2 Feedback input

The FB pin is intended to be connected directly to the collector of the optocoupler that provides the galvanic insulation to the control loop as well as to act as compensation output for the primary side control (PSR) loop of the output voltage (see *Section 7.2.4*). A suitable RC network can be placed between FB and ground to compensate the control loop.

In case of constant output voltage applications, the PSR loop can be used to regulate the output voltage saving the secondary side error amplifier.

The FB voltage is also used as an input parameter for the burst-mode operation described in *Section 7.2.5*.

The pin embeds protection to prevent from the operation with the failed optocoupler and can be pulled to ground to interrupt the switching activity (stop mode).

7.2.3 Zero current detection

The zero level detection is performed by a trigger logic that, once armed by a rising voltage, is sensitive to falling edges. The advanced ZCD logic is able to discriminate between the normal operation, output short-circuit or start-up condition.

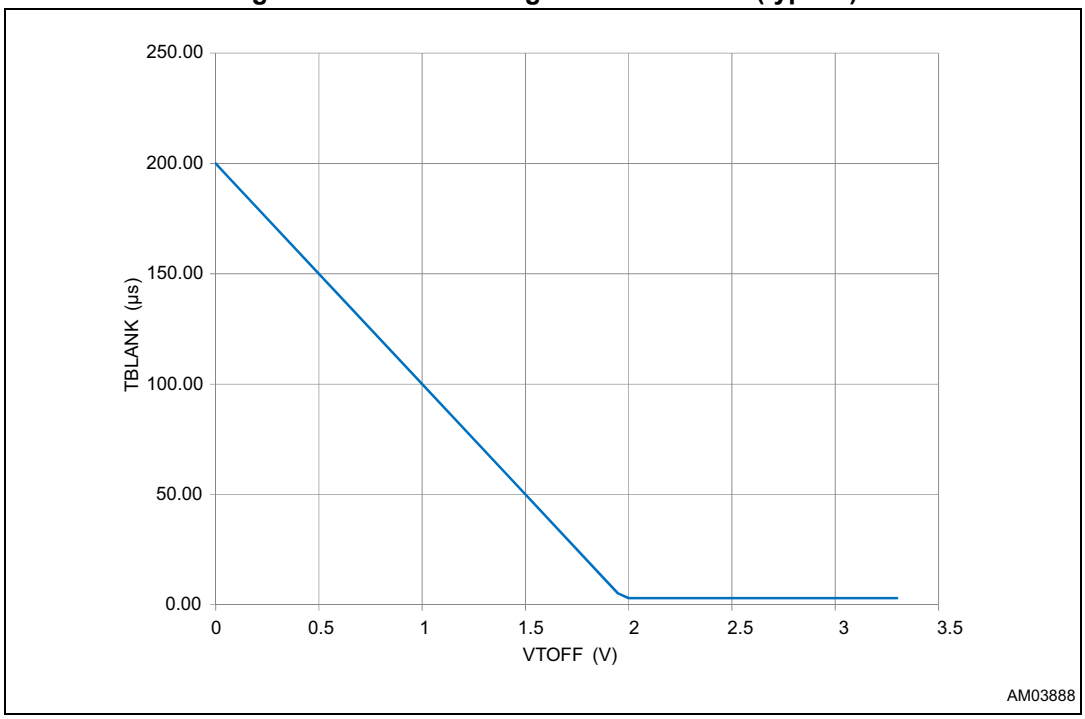
An internal blanking time prevents any triggering signal to activate the MOSFET's at the very beginning of the off time, where spurious resonances could be present. As a result, the first falling edge occurring after the blanking time turns on the MOSFET.

To ensure a proper operation, the transformer has to be designed to guarantee that the inductor's demagnetization time is longer than TBLANK (at VTOFF > VTOFF,fix) when the V_{CS} value (*Equation 1:*) is higher than 0.3 V (typ.).

The TOFF pin is intended to select the blanking time duration. If the pin is left unconnected a fixed blanking time is provided.

The TBLANK value depends on Toff voltage (*Figure 9*).

Figure 9. TBLANK voltage vs Tblank time (typical)



An internal starter provides the triggering signal whenever a valid arming signal is not detected.

The ZCD pin embeds a negative clamp to limit the negative-going current.

7.2.4 Primary side regulation feature

The ZCD pin is also is used as input of the PSR error amplifier (E/A). The reference voltage of this loop is internally fixed to VREF,PSR and applied to the non-inverting input of the E/A. The output of such error amplifier is connected to the FB pin where the relevant compensation network has to be connected.

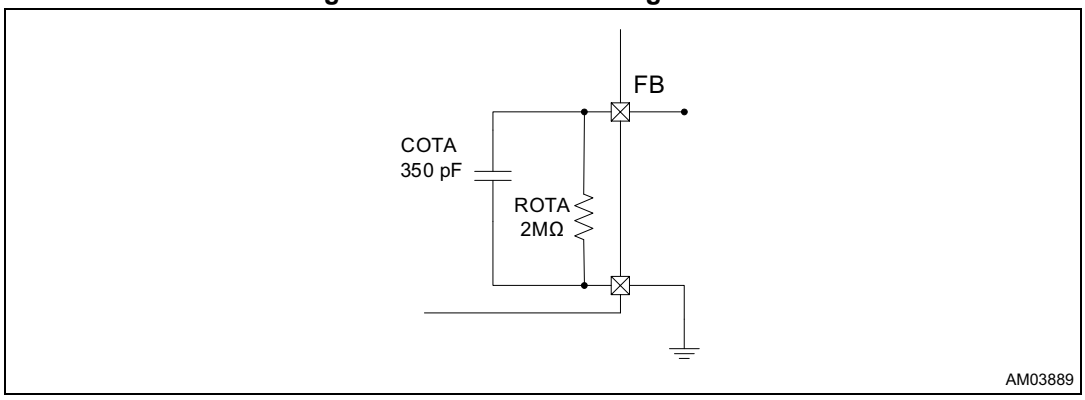
In a flyback or buck-boost topology the output voltage can be read from the primary side using an auxiliary winding: in this case the output voltage is obtained using the following equation:

Equation 3

$$Vout = VREF,PSR \bullet \frac{N_{SEC}}{N_{AUX}} \bullet \left(1 + \frac{Rzcd}{Rfb}\right)$$

The internal small signal model of the PSR E/A is obtained considering the voltage gain (G_V = 73 dB) and the gain bandwidth product (GBWP = 1 MHz) and is illustrated in *Figure 10*.

Figure 10. PSR E/A small signal model



7.2.5 Burst-mode operation

As soon as the FB pin drops below Vbm, the burst-mode operating mode is entered. The switching activity is temporarily interrupted until the FB voltage returns above the Vbm value. An internal hysteresis improves the noise rejection of this feature. The FB biasing current follows the same rules as in the normal operation; therefore the burst-mode operation is either defined by the secondary side error amplifier when an optocoupler is used or by the internal error amplifier if the PSR operation is on.

An internal biasing mean prevents the FB voltage to drop below disabling thresholds during the inactive state.

7.3 Gate driver

The output stage, connected to VCC potential and capable of the 300 mA source and the 600 mA sink current, is suitable to drive high current MOSFETs. The resulting managed power can be greater than 150 W.

7.4 IC supply management

The IC's voltage supply is managed by the UVLO circuitry together with the high voltage start-up unit and reference generators. These logics define also supply currents during different operating conditions.

7.4.1 VCC supply management

The IC is designed to operate with a range of supply voltage to ensure an optimum gate driving. An active limiting device is embedded to prevent low energy fluctuations to bring the VCC voltage above the technological constraints.

Both the active mode and the low consumption mode exhibits very low supply currents in order to meet energy saving regulation.

The VCC pin can be driven independently from the HVSU pin's connection, for example when auxiliary supply voltage is present. In this case the HVSU pin will be used solely to monitor input voltage.

A bulk capacitor, having a capacitance of around 10 µF, followed by a ceramic capacitor, having a typical capacitance of 100 nF and connected very tight to the V_{CC} pin, are necessary to properly sustain the Vcc voltage during all operating phases.

7.4.2 High voltage start-up

High voltage start-up (HVSU) circuitry is primarily intended to provide the start-up current to the VCC pin and maintain the IC responsive during low consumption modes.

This structure is able to sustain at least 800 V to avoid any damage in case of a surge or a burst on the stage's input.

The overall structure is off until input voltage reaches the VHVSU, start threshold, after that it sources a minimum current (Icharge,su) to charge the VCC pin up to Vcc,su threshold. This condition prevents the IC from severe damaging effects in case of a short-circuit on the V_{CC} pin.

At this V_{CC} voltage a higher current (Icharge) is provided to VCC to reach the VCC,on threshold. At this occurrence the active mode is invoked and the HVSU is turned off.

During other active mode's phases and the stop mode the HVSU is off.

If the low consumption mode is entered, the HVSU unit is turned on.

Table 6 summarizes the HVSU behavior in all IC conditions.

Table 6. HVSU operating modes

Operating condition (see *Figure 7*)	VCC range	OFF	Icharge,su	Icharge
All states if VIN < VHVSU,ON	-	X		
Start-up (logic start-up)	0 V... Vcc,su		X	
Start-up (IC start-up)	Vcc,su ... Vcc,on			X
Active mode (no switching period)	Vcc,su ... VCC,MAX			X
Active mode (switching period)	Vcc,su ... VCC,MAX	X		
Stop mode	Vcc,su ... VCC,MAX	X		
Low consumption mode	Vcc,su Vcc,on (rising)			X
Low consumption mode (after the end of entering conditions)	Vcc,su ... Vcc,on			X

7.5 Autorestart timer (ART)

The autorestart timer unit is responsible for the generation of the protection's intervals and of the restart times after the low consumption mode. A summary of all possible combination of times is described in each protection paragraph.

7.6 Protections

A comprehensive set of protections is embedded to ensure a high level of reliability of the final application using a limited number of components.

7.6.1 Overcurrent protection (OCP)

To prevent any damage to active components in case of inductor's saturation the MOSFET is immediately turned off by the fast OCP protection. At this occurrence the IC temporarily enters the stop state for a time equal to TOCP.

7.6.2 Input overvoltage protection (I-OVP)

Disturbances of the input voltage like surges or bursts may increase the voltage applied to the transformer primary side. Worst, an excessive input voltage could be applied to the application. These occurrences may result into MOSFET damage during the off-state when the drain voltage rises to Vin plus reflected voltage, eventually above the maximum absolute rating of the MOSFET itself.

An input voltage higher than VSurge, measured by HVSU structure, immediately stops the IC. If the extra voltage diminishes before Tsurge the device restarts immediately without activating the start-up procedure, otherwise the low consumption mode is entered until the input voltage returns below the safety threshold. An internal hysteresis improves the noise rejection of this feature. In the latter case the ART activates the start-up procedure.

7.6.3 Brownout protection (BO)

The current sourced by the ZCD pin's negative clamp during on time is compared to a minimum value to determine whether the input voltage is lower than the input range specification (brownout protection). If a value lower than IBO for a time longer than TBO, managed by the ART, is detected, the IC is stopped for Trec and then restarted.

When the protection is triggered, the ART performs the autorelaoding procedure after Trec. The brownout protection is active during the active mode, but blanked during the soft-start.

7.6.4 Optocoupler failure protection (OFP)

This protection detects either the absence of the optocoupler control (no pull-down) or the overload condition for more than a time equal to TOFP and switches off the application putting the device in the low consumption mode. This prevents the output power from rising above excessive values due to the loss of control.

The ART manages the TOFP interval and performs the auto-reloading procedure after Trec. The OFP is active during the active mode, but blanked during the soft-start.

7.7 Disable and monitor feature

Several disabling means are available to externally disable the IC:

1. **Driving FB pin low (FB_DIS):** this occurrence immediately stops the switching activity until the FB voltage returns above the threshold.
2. **Driving CTRL pin low (CTRL_DIS):** this occurrence immediately puts the device in the low consumption mode; when the CTLR pin is left free, the internal biasing mean pulls-up the voltage above the threshold entering the soft-start procedure.
3. **Driving CTRL pin high (AN_DIS):** a CTRL voltage higher than the threshold for a time longer than Tdis causes the device to enter the low consumption mode. The ART timer performs an auto-recover procedure after Trec.

Anytime the HVLED001 device enters low consumption, an internal pull-down discharges the soft-start capacitor and resets the soft-start time.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 11. SSOP10 package outline

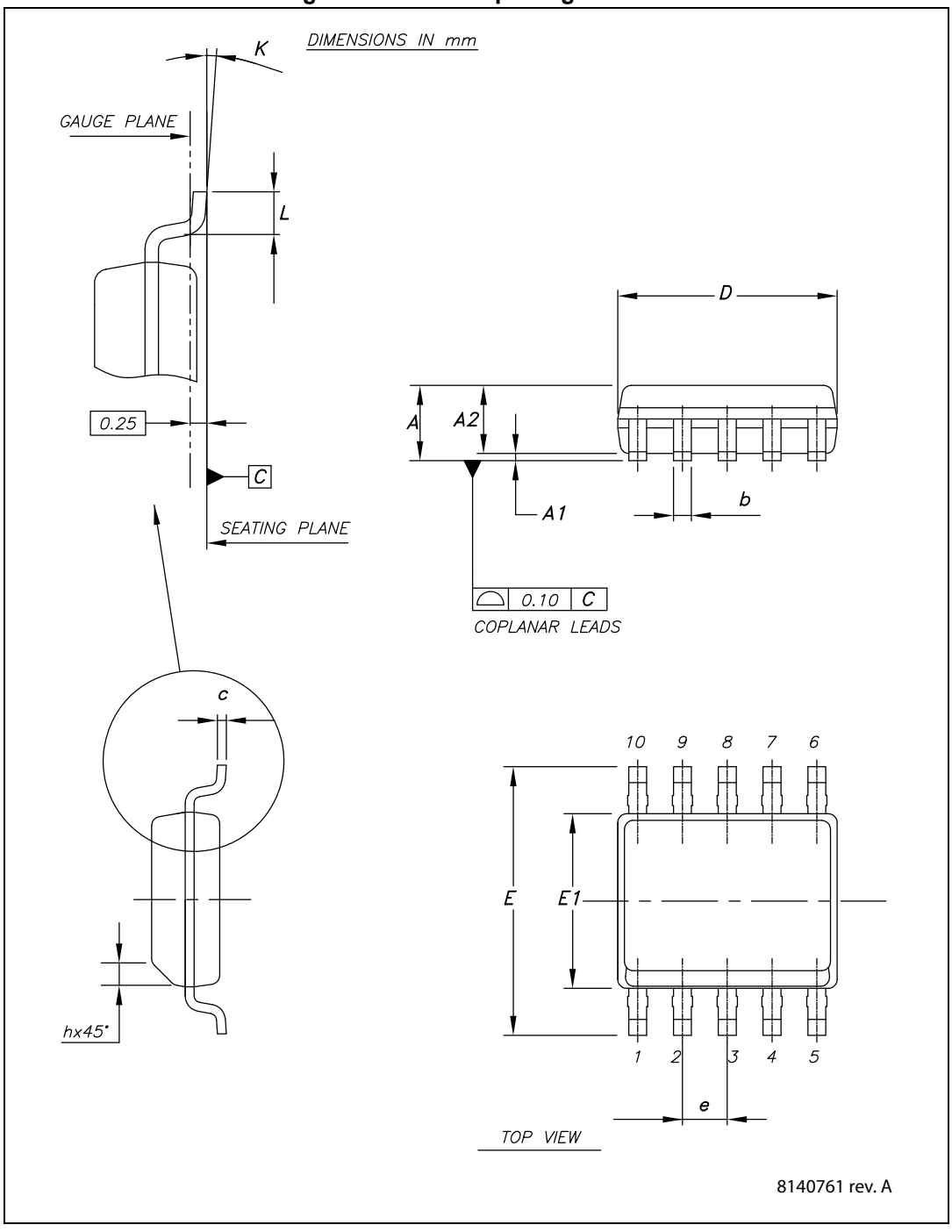


Table 7. SSOP10 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e		1	
h	0.25		0.50
L	0.40		0.90
K	0°		8°

9 Revision history

Table 8. Document revision history

Date	Revision	Changes
13-Jan-2015	1	Initial release.