

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete Vendor CAGE 18714. Add vendor CAGE 27014. Editorial changes throughout.	91-08-28	M. A. Frye
B	Add vendor CAGE 01295 for device type 01. Change boilerplate to add device class V criteria.	97-08-04	Monica L. Poelking
C	Add vendor CAGE F8859. Add case outline X. Add device type 03. Add delta limits, table III. Update boilerplate to MIL-PRF-38535 requirements. - LTG	02-06-24	Thomas M. Hess
D	Change lead temperature for case outline X in section 1.3. Add section 1.5, radiation features. Update boilerplate to include radiation hardness assured requirements. Add notes to figure 4, switching waveforms and test circuit. Editorial changes throughout. - LTG	04-12-01	Thomas M. Hess
E	Add appendix A, microcircuit die. Update the boilerplate to MIL-PRF-38535 requirements and to include radiation hardness assurance requirements. Editorial changes throughout. - jak	07-03-19	Thomas M. Hess

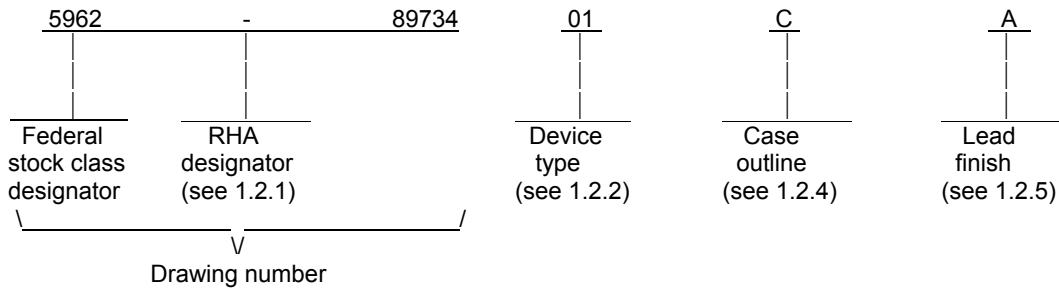
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SHEET																							
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REV STATUS OF SHEETS				REV				E	E	E	E	E	E	E	E	E	E	E	E	E			
				SHEET				1	2	3	4	5	6	7	8	9	10	11	12	13	14		
PMIC N/A				PREPARED BY Marcia B. Kelleher				DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dscc.dla.mil															
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Thomas J. Ricciuti																			
				APPROVED BY Michael A. Frye				MICROCIRCUIT, DIGITAL, ADVANCED CMOS, HEX INVERTER, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON															
				DRAWING APPROVAL DATE 91-08-28																			
				REVISION LEVEL E				SIZE A	CAGE CODE 67268	5962-89734													
				SHEET				1	OF	21													

1. SCOPE

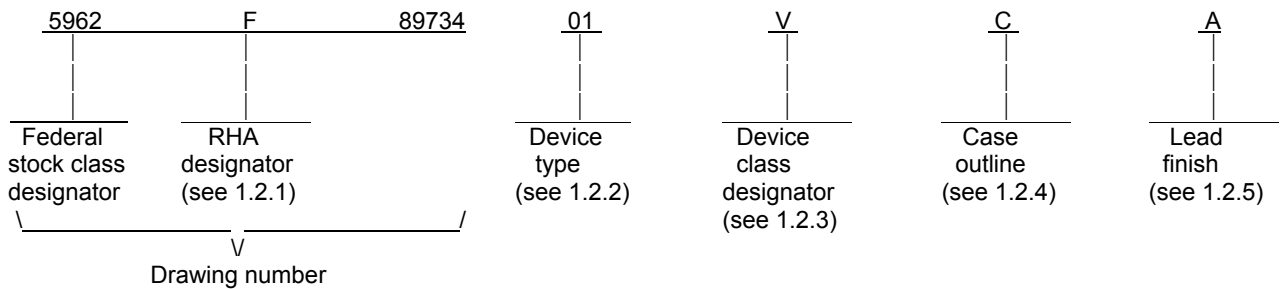
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ACT04	Hex inverter, TTL compatible inputs
02	54ACT11004	Hex inverter, TTL compatible inputs
03	54ACT04	Hex inverter, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.
Q or V	Certification and qualification to MIL-PRF-38535.

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1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
X	CDFP3-F14	14	Flat pack
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC input diode current	± 20 mA
DC output diode current (per pin)	± 50 mA
DC output source or sink current	± 50 mA
DC V_{CC} or GND current	± 150 mA
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds):	
Case outline X	+260°C
Other case outlines except case X	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C 4/

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range (V_{CC})	4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum input rise or fall rate ($\Delta t/\Delta V$)	0 to 8 ns/V
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features.

Device type 03:

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	300 krad (Si)
Single Event Latch-up (SEL)	≥ 93 MeV-cm ² /mg 6/

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
- 4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
- 5/ Unused inputs must be held high or low to prevent them from floating.
- 6/ Limits are guaranteed by design or process but not production tested unless specified by the customer through the purchase order or contract.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

JESD 78 - IC Latch-up Test

(Copies of this document is available online at www.eia.org/ or from the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-PRF-38535, appendix A).

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TABLE IA. Electrical performance characteristics

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified		Device type and device class	V _{CC}	Group A subgroups	Limits <u>4/</u>		Unit		
							Min	Max			
Positive input clamp voltage 3022	V _{IC+}	For input under test, I _{IN} = 18 mA		01, 02 V	4.5 V	1, 2, 3		5.7	V		
		For input under test, I _{IN} = 1 mA		03 V	GND		0.4	1.5			
Negative input clamp voltage 3022	V _{IC-}	For input under test, I _{IN} = -18 mA		01, 02 V	4.5 V	1, 2, 3		-1.2	V		
		For input under test, I _{IN} = -1 mA		03 V	Open		-0.4	-1.5			
High level output voltage 3006	V _{OH} <u>5/</u>	For all inputs affecting output under test V _{IN} = 2.0 V or 0.8 V For all other inputs V _{IN} = V _{CC} or GND	I _{OH} = -50 μA	All All	4.5 V	1, 2, 3	4.4		V		
					5.5 V		5.4				
					4.5 V		3.7				
					5.5 V		4.7				
Low level output voltage 3007	V _{OL} <u>5/</u>	For all inputs affecting output under test V _{IN} = 2.0 V or 0.8 V For all other inputs V _{IN} = V _{CC} or GND	I _{OL} = 50 μA	All All	4.5 V	1, 2, 3		0.1	V		
					5.5 V			0.1			
					4.5 V			0.5			
					5.5 V			0.5			
Input leakage current high 3010	I _{IH}	V _{IN} = 5.5 V		All All	5.5 V	1, 2, 3		1.0	μA		
Input leakage current low 3009	I _{IL}	V _{IN} = 0.0 V		All All	5.5 V	1, 2, 3		-1.0			
Quiescent supply current delta, TTL input levels 3005	ΔI _{CC} <u>6/</u>	V _{IL} = 0.0 V, V _{IH} = V _{CC} - 2.1 V		All All	5.5 V	1, 2, 3		1.6	mA		
Quiescent supply current 3005	I _{CC}	V _{IN} = V _{CC} or GND I _{OUT} = 0.0 μA		01, 02 All	5.5 V	1, 2, 3		80	μA		
				03 All				1		2	
								2, 3		80	
				M, D, P, L, R, F <u>7/</u>				03 Q, V		1	50

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class	V _{CC}	Group A subgroups	Limits <u>4/</u>		Unit
						Min	Max	
Input capacitance 3012	C _{IN}	See 4.4.1c T _C = +25°C	All All	GND	4		10.0	pF
Power dissipation capacitance	C _{PD} <u>8/</u>	See 4.4.1c T _C = +25°C f = 1 MHz	01, 03 All	5.0 V	4		80	pF
			02 All				40	
Latch-up input/output over-voltage	I _{CC} (O/V1) <u>9/</u>	t _w ≥ 100 μs, t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V V _{over} = 10.5 V See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up input/output positive over-current	I _{CC} (O/I1+) <u>9/</u>	t _w ≥ 100 μs, t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V I _{trigger} = +120 mA See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up input/output negative over-current	I _{CC} (O/I1-) <u>9/</u>	t _w ≥ 100 μs, t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V I _{trigger} = -120 mA See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up supply over-voltage	I _{CC} (O/V2) <u>9/</u>	t _w ≥ 100 μs, t _{cool} ≥ t _w 5 μs ≤ t _r ≤ 5 ms 5 μs ≤ t _f ≤ 5 ms V _{test} = 6.0 V, V _{CCQ} = 5.5 V V _{over} = 9.0 V See 4.4.1d	All V	5.5 V	2		100	mA
Functional tests 3014	<u>10/</u>	Verify output V _{OUT} See 4.4.1b V _{IH} = 2.0 V, V _{IL} = 0.8 V	All All	4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
Propagation delay time, input to output 3003	t _{PLH} <u>11/</u>	C _L = 50 pF R _L = 500Ω See figure 4	01, 03 All	4.5 V	9	1.0	9.0	ns
					10, 11	1.0	10.0	
			02 All		9	1.0	9.0	
					10, 11	1.0	10.2	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/ 3/</u> -55°C ≤ T _C ≤ +125°C +4.5 V ≤ V _{CC} ≤ +5.5 V unless otherwise specified	Device type and device class	V _{CC}	Group A subgroups	Limits <u>4/</u>		Unit
						Min	Max	
Propagation delay time, input to output 3003	t _{PHL} <u>11/</u>	C _L = 50 pF R _L = 500Ω See figure 4	01, 03 All	4.5 V	9	1.0	8.5	ns
						10, 11	1.0	
			02 All		9	1.0	8.7	
					10, 11	1.0	10.3	

- 1/ For tests not listed in the referenced MIL-STD-883, (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table IA herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.
- 3/ RHA parts for device type 03 supplied to this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, this device is only tested at the 'F' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
- 4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table IA, as applicable, at 4.5 V ≤ V_{CC} ≤ 5.5 V.
- 5/ The V_{OH} and V_{OL} tests shall be tested at V_{CC} = 4.5 V. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for V_{CC} = 5.5 V. Limits shown apply to operation at V_{CC} = 5.0 V ± 0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum. Transmission driving tests may be performed using V_{IN} = V_{CC} or GND. When V_{IN} = V_{CC} or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.
- 6/ ΔI_{CC}(max)/pin ≤ 1.6 mA (preferred method), or ΔI_{CC}/package ≤ 1.6 mA x the number of input pins/package where ΔI_{CC}(max)/data pin ≤ 1.6 mA and ΔI_{CC}(max)/control pin ≤ 3.0 mA (alternate method).
- 7/ The maximum limit for this parameter at 100 krads (Si) is 2 μA.
- 8/ Power dissipation capacitance (C_{PD}) determines both the load dynamic power consumption (P_D) and current consumption (I_S) where:

$$P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$$

$$I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$$
 For both C_{PD} and I_S, n is the number of device inputs at TTL levels, f is the frequency of the input signal, d is the duty cycle of the input signal, and C_L is the output load capacitance.
- 9/ See EIA/JEDEC STD. No. 78 for electrically induced latch-up test methods and procedures. The values listed for I_{trigger} and V_{over} are to be accurate within ±5 percent.
- 10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs L ≤ 0.8 V, H ≥ 2.0 V.
- 11/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum AC limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

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TABLE IB. SEP test limits. 1/ 2/

Device type	SEP	T _C = temperature ±10°C	V _{CC}	Effective LET
03	SEL	+25°C	5.5 V	≥ 93 MeV-cm ² /mg

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

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Device types	01, 03		02	
Case outlines	C, D, X	2	R	2
Terminal number	Terminal symbol			
1	1A	NC	1Y	V _{CC}
2	1Y	1A	2Y	NC
3	2A	1Y	3Y	3A
4	2Y	2A	GND	2A
5	3A	NC	GND	1A
6	3Y	2Y	GND	1Y
7	GND	NC	GND	2Y
8	4Y	3A	4Y	3Y
9	4A	3Y	5Y	GND
10	5Y	GND	6Y	GND
11	5A	NC	6A	GND
12	6Y	6Y	5A	GND
13	6A	6A	4A	4Y
14	V _{CC}	5Y	NC	5Y
15	---	NC	V _{CC}	6Y
16	---	5A	V _{CC}	6A
17	---	NC	NC	5A
18	---	4Y	3A	4A
19	---	4A	2A	NC
20	---	V _{CC}	1A	V _{CC}

NC = No connection.

Pin description	
Terminal symbol	Description
mA (m = 1 to 6)	Data inputs
mY (m = 1 to 6)	Data outputs

FIGURE 1. Terminal connections.

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Inputs	Outputs
H	L
L	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

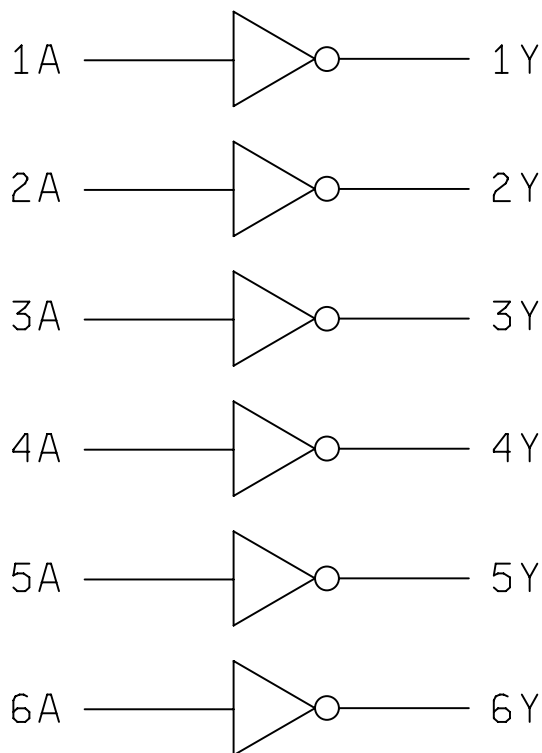
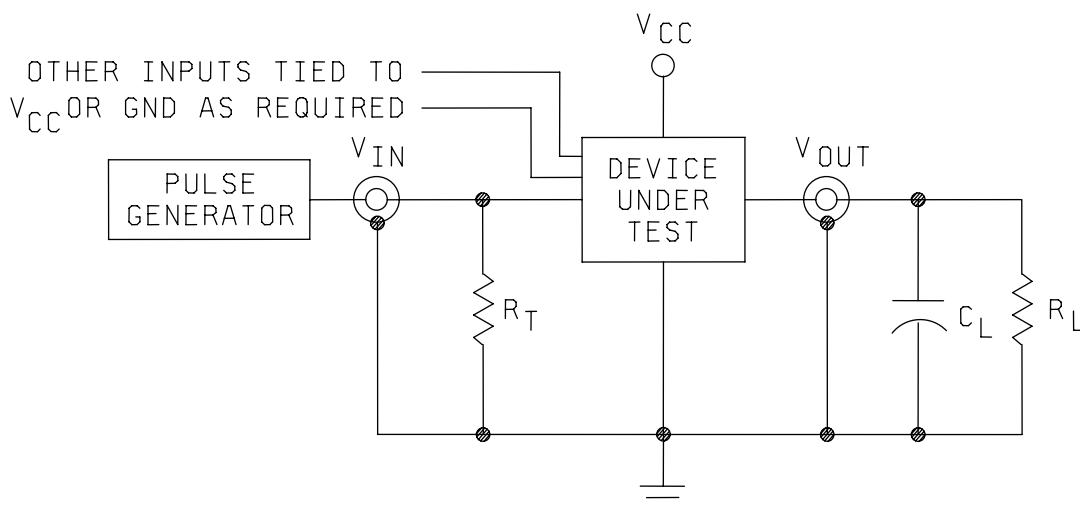
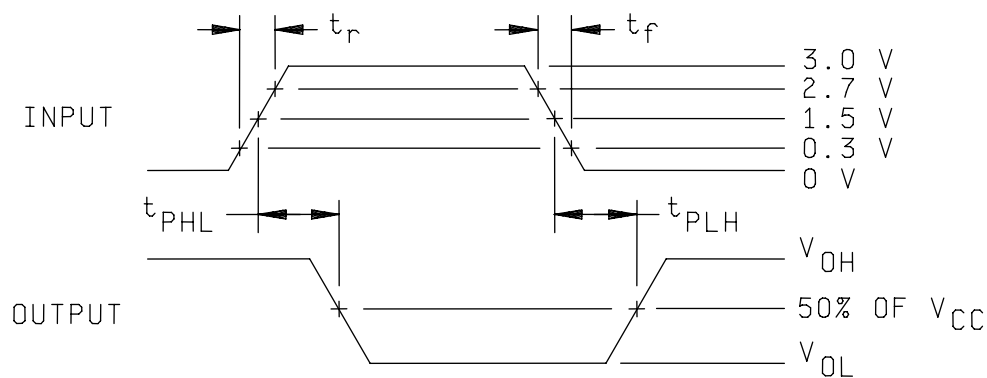


FIGURE 3. Logic diagram.

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Device types 01, 02, and 03



NOTES:

1. $C_L = 50 \text{ pF}$ per table I (includes test jig and probe capacitance).
2. $R_T = 50\Omega$, $R_L = 500\Omega$ or equivalent.
3. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $\text{PRR} \leq 10 \text{ MHz}$; $t_r \leq 3.0 \text{ ns}$; $t_f \leq 3.0 \text{ ns}$; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V , respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1MHz .
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JDEC Standard No. 20 and table IA herein. For C_{IN} and C_{PD} , test all applicable pins on five devices with zero failures.
- d. Latch-up tests are required for device class V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up tests, test all applicable pins on five devices with zero failures.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	^{1/} 1, 2, 3, 7, 8, 9	^{1/} 1, 2, 3, 7, 8, 9, 10, 11	^{2/} ^{3/} 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	^{3/} 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

^{1/} PDA applies to subgroup 1.

^{2/} PDA applies to subgroups 1, 7, and deltas.

^{3/} Delta limits, as specified in table IIB, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter ^{1/}	Symbol	Device type	Delta limits
Supply current	I_{CC}	01 ^{2/}	± 100 nA
		03	± 150 nA
Supply current delta	ΔI_{CC}	03	± 0.4 mA
Input current low level	I_{IL}	03	± 20 nA
Input current high level	I_{IH}	03	± 20 nA
Output voltage low level $V_{CC} = 5.5$ V, $I_{OL} = 24$ mA	V_{OL}	03	± 0.04 V
Output voltage high level $V_{CC} = 5.5$ V, $I_{OH} = -24$ mA	V_{OH}	03	± 0.20 V

^{1/} These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

^{2/} Guaranteed, if not tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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b. $T_A = +125^{\circ}\text{C}$, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} + 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Inputs tested high, $V_{CC} = 5.5 \text{ V dc } \pm 5\%$, $V_{IN} = 5.0 \text{ V dc } + 10\%$, $R_{IN} = 1\text{k}\Omega \pm 20\%$, and all outputs are open.

b. Inputs tested low, $V_{CC} = 5.5 \text{ V dc } \pm 5\%$, $V_{IN} = 0.0 \text{ V dc}$, $R_{IN} = 1\text{k}\Omega \pm 20\%$, and all outputs are open.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².

c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be $+25^{\circ}\text{C}$ and the latchup test temperature is maximum rated operating temperature $\pm 10^{\circ}\text{C}$.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

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4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, P.O. Box 3990 Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of upsets (SEP).
- d. Number of transients (SEP).
- e. Occurrence of latch-up (SEP).

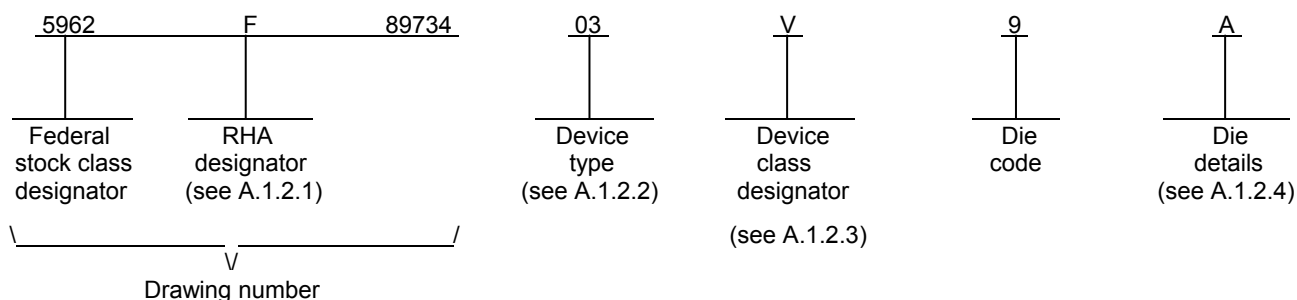
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
03	54ACT04	Hex inverter, TTL compatible inputs

A.1.2.3 Device class designator. Device class Q designator will not be included in the PIN and will not be marked on the device since the device class designator has been added after the original issuance of this drawing.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2. APPLICABLE DOCUMENTS

A.2.1 Government specification, standards, and handbooks. The following specification, standard, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

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A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0547.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

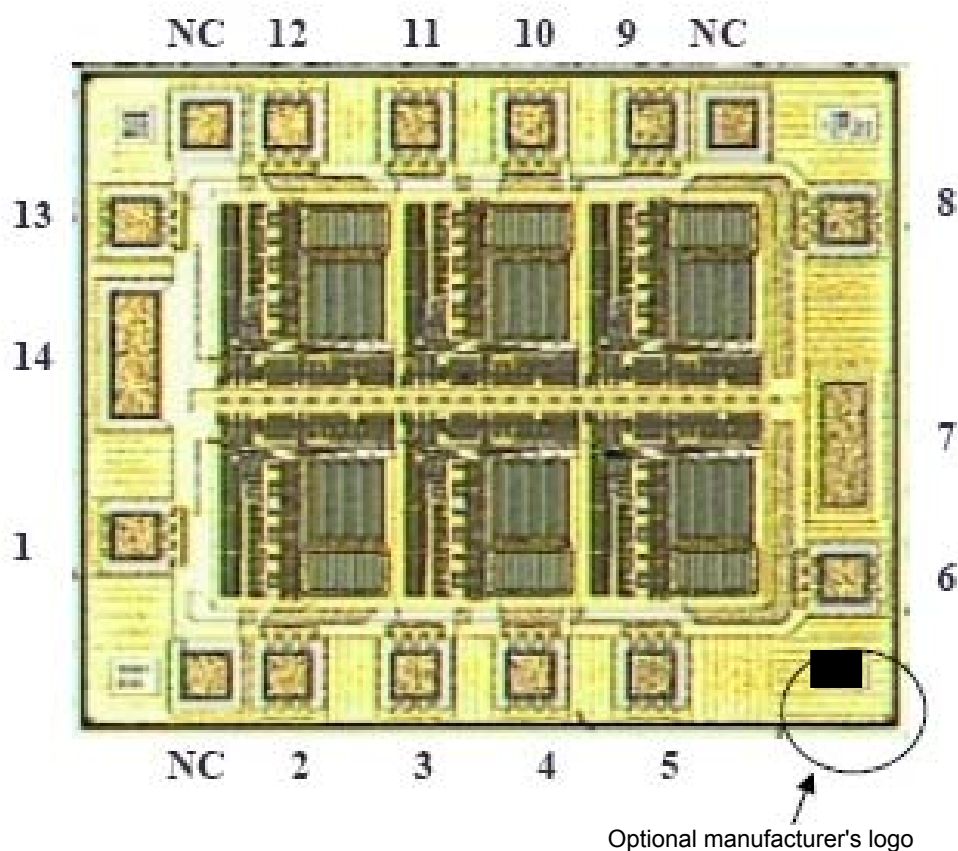
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Die physical dimensions.

Die size: 1941.2 x 1577.2 μm
Die thickness: 285 \pm 25 μm

Die bonding pad locations and electrical functions.



Pad size: Pad numbers 1 to 6 and 8 to 13: 100 x 100 μm
Pad numbers 7 (GND) and 14 (V_{CC}): 100 x 280 μm

NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1

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Interface materials.

Top metallization: Al Si Cu 0.85 μm

Backside metallization: None

Glassivation.

 Type: P. Vapox + Nitride
 Thickness: 5000Å – 7000Å

Substrate: Silicon

Assembly related information.

Substrate potential: Floating or tied to GND

Special assembly instructions: Bond pad #14 (V_{CC}) first

FIGURE A-1 – Continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-03-19

Approved sources of supply for SMD 5962-89734 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/SMCR/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8973401CA	27014 01295 0C7V7	54ACTQ04DMQB SNJ54ACT04J 54ACTQ04DMQB
5962-8973401DA	27014 01295 0C7V7	54ACTQ04FMQB SNJ54ACT04W 54ACTQ04FMQB
5962-89734012A	27014 01295 0C7V7	54ACTQ04LMQB SNJ54ACT04FK 54ACTQ04LMQB
5962-8973401VCA	27014 01295	54ACTQ04J-QMLV SNV54ACT04J
5962-8973401VDA	27014 01295	54ACTQ04W-QMLV SNV54ACT04W
5962-8973401V2A	27014	54ACTQ04E-QMLV
5962-8973402RA	3V146	54ACT11004/BRA
5962-89734022A	3V146	54ACT11004/B2A
5962-8973403XA	<u>3/</u>	54ACT04K02Q
5962-8973403VXA	<u>3/</u>	54ACT04K02V
5962-8973403XC	<u>3/</u>	54ACT04K01Q
5962-8973403VXC	<u>3/</u>	54ACT04K01V
5962F8973403CA	F8859	RHFACT04D04Q
5962F8973403CC	F8859	RHFACT04D03Q
5962F8973403XA	F8859	RHFACT04K02Q
5962F8973403XC	F8859	RHFACT04K01Q
5962F8973403VCA	F8859	RHFACT04D04V
5962F8973403VCC	F8859	RHFACT04D03V
5962F8973403VXA	F8859	RHFACT04K02V
5962F8973403VXC	F8859	RHFACT04K01V
5962F8973403V9A	F8859	ACT04DIE2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
27014	National Semiconductor 2900 Semiconductor Drive P. O. Box 58090 Santa Clara, CA 95052-8090
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Ln. P. O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P. O. Box 84, M/S 853 Sherman, TX 75090-9493
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE
3V146	Rochester Electronics 10 Malcolm Hoyt Drive Newburyport, MA 01950
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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