- **Drive Capability and Output Counts**
  - **80 mA (Current Sink) x 16 Bits**
- **Constant Current Output Range**
  - **5 to 80 mA (Current Value Setting for All Output Terminals Using External Resistor and Internal Brightness Control Register)**
- **Constant Current Accuracy**
  - **±4% (Maximum Error Between Bits)**
- **Voltage Applied to Constant Current Output Terminals**
  - **Minimum 0.4 V (Output Current 5 to 40 mA)**
  - **Minimum 0.7 V (Output Current 40 to 80 mA)**
- **1024 Gray Scale Display**
  - **Pulse Width Control 1024 Steps**
- **Brightness Adjustment†**
  - **All Output Current Adjustment for 64 Steps (Adjustment for Brightness Deviation Between LED Modules)**
  - **Output Current Adjustment by Output (OUT0 to OUT15) for 64 Steps (Adjustment for Brightness Deviation Between Dots)**
  - **Brightness Control by 16 Steps Frequency Division Gray Scale Control Clock (Brightness Adjustment for Panel)**
- **Gray Scale Clock Generation**
  - **Gray Scale Control Clock Generation by Internal PLL or External Input Selectable**
- **Clock Invert/Noninvert Selectable**
  - **Clock Invert Selectable to Reduce Changes in Duty Ratio at Cascade Operation**
- **Protection**
  - **WDT (Watchdog Timer) Function (Turn Output Off When Scan Signal Stopped)**
  - **TSD (Thermal Shutdown) Function (Turn Output Off When Junction Temperature Exceeds Limit)**
- **LOD**
  - **LED Open Detection (Detection for LED Disconnection)**
- **Data Input/Output‡**
  - **Port A (for Data Display)**
    - **Clock Synchronized 10 Bit Parallel Input (Schmitt Triggered Input)**
    - **Clock Synchronized 10 Bit Parallel Output (3-State Output)**
  - **Port B (for Dot Correction Data)**
    - **Clock Synchronized 6 Bit Parallel Input (Schmitt-Triggered Input)**
    - **Clock Synchronized 6 Bit Parallel Output**
- **Input/Output Signal Level**
  - **CMOS Level**
- **Power Supply Voltage**
  - **4.5 V to 5.5 V (Logic, Analog and Constant Current)**
  - **3 V to 5.5 V (Interface)**
- **Maximum Output Voltage . . . 15 V (Max)**
- **Data Transfer Rate . . . 20 MHz (Max)**
- **Gray Scale Clock Frequency**
  - **16 MHz (Max) Using Internal PLL**
  - **8 MHz (Max) Using External Clock**
- **Operating Free-Air Temperature Range –20°C to 85°C**
- **100-Pin HTQFP Package (P_D=4.7 W, T_A = 25°C)**

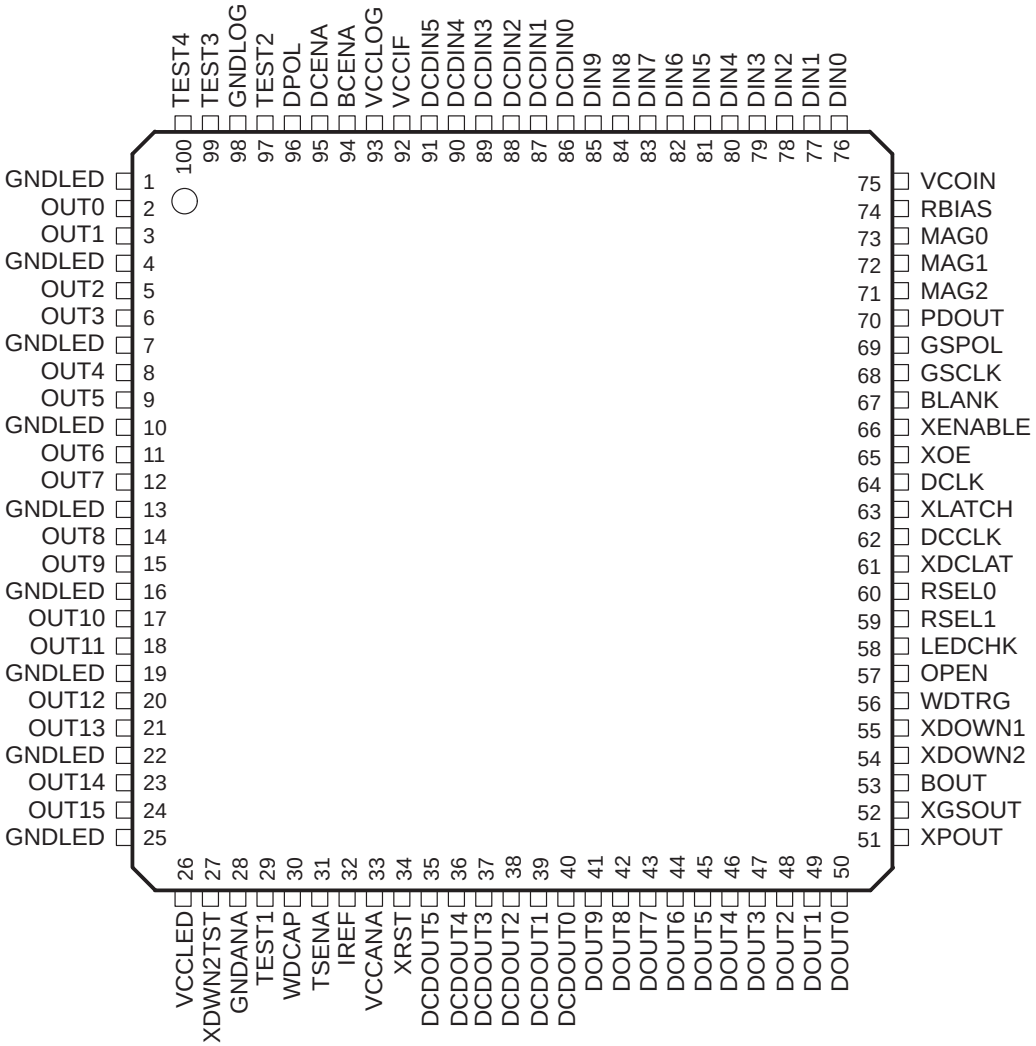
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† These functions are adjustable independently.
‡ Allows the writting of all the data at port A by setting the logic to 1.

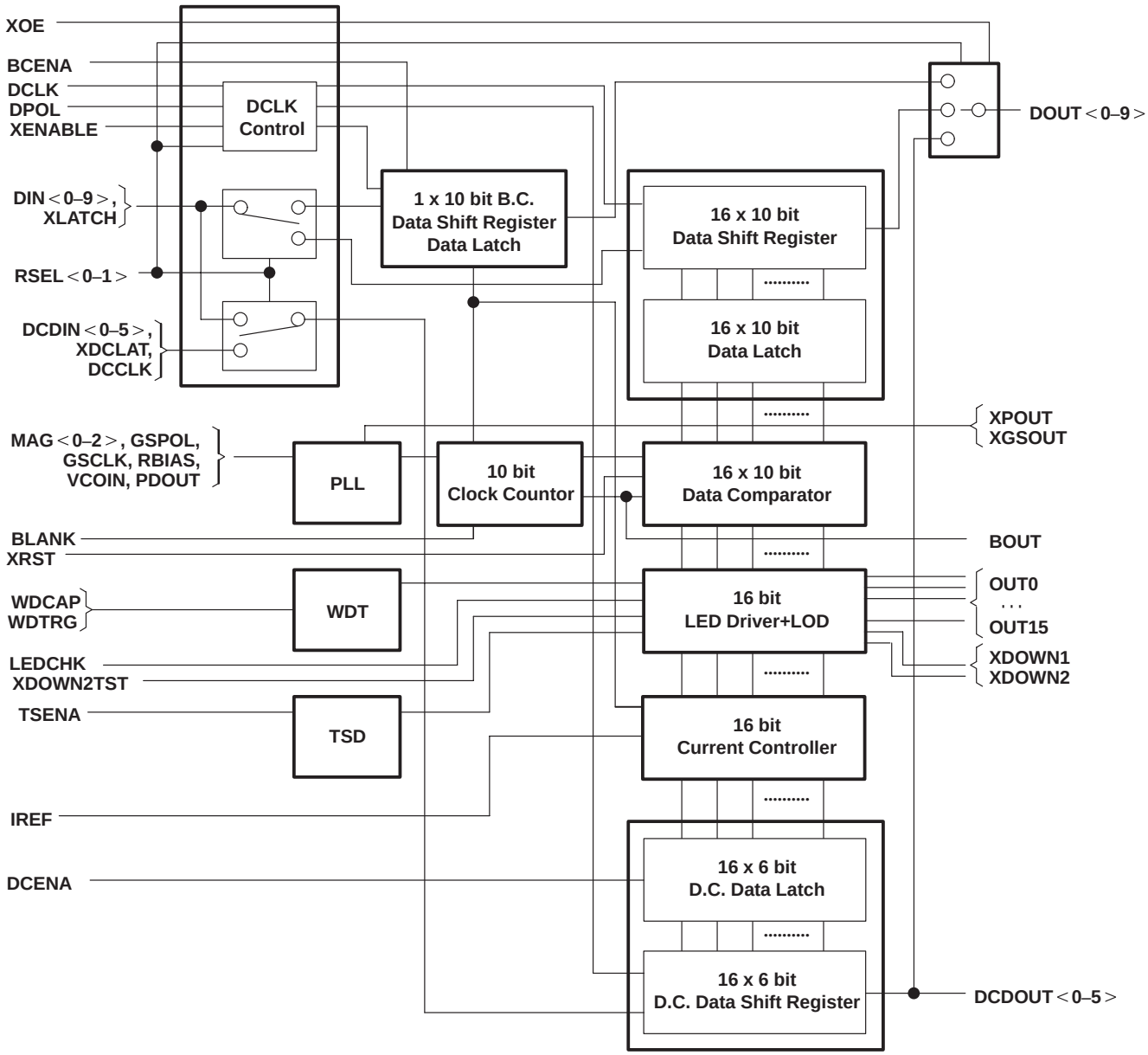
description

The TLC5910 is a constant current driver, incorporating a shift register, data latch, and constant current circuitry with current value adjustable, PLL circuitry for gray scale control clock generation, and 1024 gray scale display using pulse width control. The output current is a maximum of 80 mA with 16 bits, and the current value of constant current output can be set by one external resistor. The device has two channel I/O ports. The brightness deviation between LED modules (ICs) can be adjusted by external data input from a display data port. The brightness control for the panel can be accomplished by the brightness adjustment circuitry. Independently of these functions, the device incorporates the shift register and data latch to correct the deviation between LEDs adjusting output current using data from a dot correction data port. Moreover, the device incorporates watchdog timer (WDT) circuitry, which turns the constant current output off when a scan signal is stopped at the dynamic scanning operation. It incorporates thermal shutdown (TSD) circuitry, which turns constant current output off when the junction temperature exceeds the limit. It also incorporates LOD (LED open detection) circuitry, which creates an error signal output when LED disconnection occurs and test mode functions detect LED open or short conditions.

PZP PACKAGE
(TOP VIEW)



functional block diagram

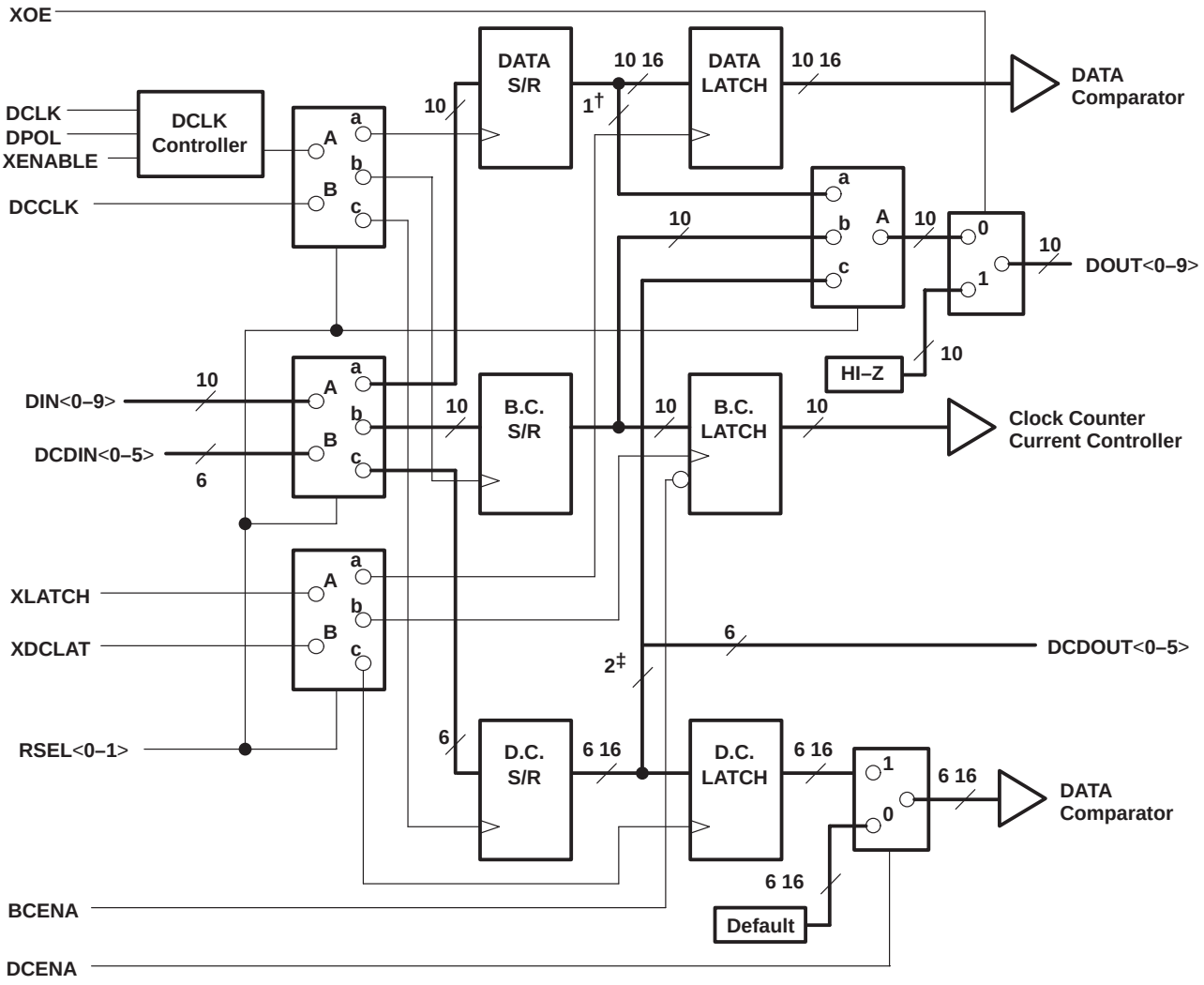


B.C. (brightness control) : Adjustment for brightness deviation between LED modules, and between panels.

D.C (Dot Control) : Adjustment for brightness deviation between dots.

NOTE: All the input terminals are with Schmitt-triggered inverters except RBIAS, VCOIN, PDOUT, IREF, and WDCAP.

functional block diagram for shift register and data latch



† 1 : Connect to 16th 10 bit bus
‡ 2 : Connect to 16th 6 bit bus

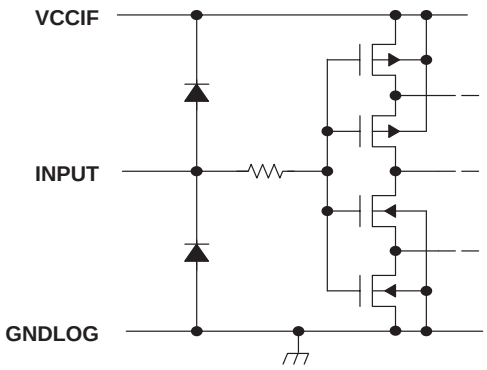
B.C. (brightness control) : Adjustment for brightness deviation between LED modules, and between panels.

D.C. (dot control) : Adjustment for brightness deviation between dots.

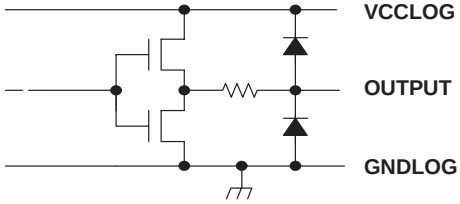
RSEL		CONNECTION
RSEL1	RSEL0	
0	0	A – a, B – c
0	1	A – b, B – c
1	0	A – c
1	1	INHIBIT

schematic

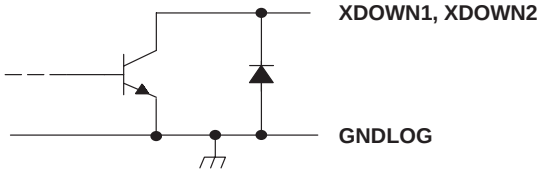
Input



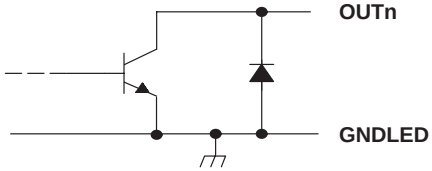
DOUT0–9, DCDOUT0–5, XGSOUT, XPOUT, BOUT



XDOWN1, XDOWN2



OUTn



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BCENA	94	I	Brightness control enable. When BCENA is low, brightness control latch is set to the default value. The output current value in this status is 100% of setting the value by an external resistor. The frequency division ratio of GSCLK is 1/1. When BCENA is high, writing to brightness control latch is enabled.
BLANK	67	I	Blank(light off). When BLANK is high, all outputs of the constant current driver are turned off. When GSPOL is high, the output is turned on (LED on), synchronizing to the falling edge of GSCLK after the next rising edge of GSCLK, when BLANK goes from high to low. When GSPOL is low, the output is turned on (LED on), synchronizing to the rising edge of GSCLK after the next falling edge of GSCLK, when BLANK goes from high to low.
BOUT	53	O	BLANK buffered output
DCCLK	62	I	Clock input for data transfer. The input data is from DCDIN (port B) , output data at DCDOUT, and all data on the shift register for dot correction data, from DCDIN, is shifted by 1 bit synchronizing to the rising edge of DCCLK.
DCDIN0 – DCDIN5	86,87,88, 89,90,91	I	Input for 6 bit parallel data (port B). These terminals are used as a shift register input for dot correction data.
DCDOUT0 – DCDOUT5	40,39,38, 37,36,35	O	Output for 6 bit parallel data (port B). These terminals are used as a shift register output for dot correction data.
DCENA	95	I	Latch enable for dot correction data. When DCENA is low, the latch is set to the default value. At this time, the output current value is 100% of the value set by an external resistor.
DCLK	64	I	Clock input for data transfer. The input data is from DIN (port A) , all data on the shift register selected by RSEL, 1 and output data at DOUT is shifted by 1 bit synchronizing to DCLK. Note that synchronizing to either the rising or falling edge of DCLK depends on the value of DPOL.
DIN0 – DIN9	76,77,78,79,80, 81,82,83,84,85	I	Input for 10 bit parallel data (port A). These terminals are inputs to the shift register for gray scale data, brightness control, and dot correction data. The register selected is determined by RSEL0, 1.
DOUT0 – DOUT9	50,49,48,47,46, 45,44,43,42,41	O	Output for 10 bit parallel data (port A). These terminals are outputs to the shift register for gray scale data, brightness control, and dot correction data. The register selected is determined by RSEL0, 1.
DPOL	96	I	Select the valid edge of DCLK. When DPOL is high, the rising edge of DCLK is valid. When DPOL is low, the falling edge of DCLK is valid.
GNDANA	28		Analog ground (internally connected to GNDLOG and GNDLED)
GNDLOG	98		Logic ground (internally connected to GNDANA and GNDLED)
GNDLED	1,4,7,10,13, 16,19,22,25		LED driver ground (internally connected to GNDANA and GNDLED)
GSCLK	68	I	Clock input for gray scale. When MAG0 to MAG2 are all low, GSCLK is used for pulse width control, and GSCLK is used for PLL timing control when either MAG is not low. The gray scale display is accomplished by lighting LEDs on until the number of GSCLK or PLL clocks counted is equal to data latched.
GSPOL	69	I	Select the valid edge of GSCLK. When GSPOL is high, the rising edge of GSCLK is valid. When GSPOL is low, the falling edge of GSCLK is valid.
IREF	32	I/O	Constant current value setting. LED current is set to the desired value by connecting an external resistor between IREF and GND. The 38 times current compares current across the external resistor sink on the output terminal.
LEDCHK	58	I	LED disconnection detection enable. When LEDCHK is high, LED disconnection detection is enabled and XDOWN2 is valid. When LEDCHK is low, LED disconnection detection is disabled.
MAG0 – MAG2	73,72,71	I	PLL multiple ratio setting. The clock frequency generated by PLL referenced to GSCLK is set.
OPEN	57		TEST. Factory test terminal. OPEN should be opened.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
OUT0–DOUT15	2,3,5,6,8,9,11,12, 14,15,17,18,20,21, 23,24	O	Constant current output
PDOUT	70	I/O	Resistor connection for PLL feedback adjustment
RBIAS	74	I/O	Resistor connection for PLL oscillation frequency setting
RSEL0 RSEL1	60 59	I	Input/output port selection and shift register data latch switching. When RSEL1 is low and RSEL0 is low, the gray scale data shift register latch is selected to port A and the dot correction register latch is selected to port B. When RSEL1 is low and RSEL0 is high, the brightness control register latch is selected to port A and the dot correction register latch is selected to port B. When RSEL1 is high and RSEL0 is low, the dot correction register latch is selected to port A and no register latch is selected to port B.
TEST1–TEST4	29,97,99,100	I	TEST. Factory test terminal. These terminals should be connected to GND.
THERMAL PAD	package bottom		Heat sink pad. This pad is connected to the lowest potential IC or thermal layer.
TSENA	31	I	TSD(thermal shutdown) enable. When TSENA is high, TSD is enabled. When TSENA is low, TSD is disabled.
VCOIN	75	I/O	Capacitance connection for PLL feedback adjustment
VCCANA	33		Analog power supply voltage
VCCLOG	93		Logic power supply voltage
VCCIF	92		Interface power supply voltage
VCCLED	26		LED driver power supply voltage
WDTRG	56	I	WDT (watchdog timer) trigger input. By applying a scan signal to this terminal, the scan signal can be monitored by turning the constant current output off and protecting the LED from damage when the scan signal stopped during the constant period designed.
WDCAP	30	I/O	WDT detection time adjustment. WDT detection time is adjusted by connecting a capacitor between WDCAP and GND. When WDCAP is directly connected to GND, WDT function is disabled. In this case, WDTRG should be tied to a high or low level.
XDCLAT	61	I	Data latch for dot correction. When XDCLAT is high, data on the shift register for dot correction data from DCDIN (port B) goes through latch. When XDCLAT is low, data is latched. Accordingly, if data on the shift register is changed during XDCLAT high, this new value is latched (level latch).
XDOWN1	55	O	Shutdown. XDOWN1 is configured as an open collector. It goes low when constant current output is shut down by WDT or TSD function.
XDOWN2	54	O	LED disconnection detection output. XDOWN2 is configured as an open collector. XDOWN2 goes low when an LED disconnection is detected.
XDWN2TST	27	I	Test for XDOWN2. When XDWN2TST is low, XDOWN2 goes low. (This terminal is internally pulled up with 50 kΩ)
XENABLE	66	I	DCLK enable. When XENABLE is low, data transfer is enabled. Data transfer starts on the valid edge of DCLK after XENABLE goes low. During XENABLE high, no data is transferred.
XGSOUT	52	O	Clock output for gray scale. When MAG0 to MAG2 are all low, the clock with GSCLK inverted appears on this terminal. When either MAG is not low, PLLCLK appears on this terminal.
XLATCH	63	I	Latch. When XLATCH is high, data on the shift register from DIN (port A) goes through latch. When XLATCH is low, data is latched. Accordingly, if data on the shift register is changed during XLATCH high, this new value is latched (level latch).
XOE	65	I	Data output enable. When XOE is low, DOUT0–9 terminals are driven. When XOE is high, DOUT0–9 terminals go to a high-impedance state.
XPOUT	51	O	GSPOL output inverted
XRST	34	I	Blank (Light off). When XRST is low, all the output of the constant current driver is turned off. (This terminal is internally pulled up with 50 kΩ)

absolute maximum ratings (see Note 1)†

Logic supply voltage, VCCLOG . . . . . – 0.3 V to 7 V
Supply voltage for interface circuit, VCCIF . . . . . – 0.3 V to 7 V
Supply voltage for constant current circuit, VCCLED . . . . . – 0.3 V to 7 V
Analog supply voltage, VCCANA . . . . . – 0.3 V to 7 V
Output current (dc), $I_{O(LC)}$ . . . . . 85 mA
Input voltage range, V_I . . . . . – 0.3 V to VCCLOG + 0.3 V
Output voltage range, $V_{O(DOUT)}$, $V_{O(DCDOUT)}$, V_{BOUT}, V_{XPOUT} and V_{XGSOUT} . . . . . – 0.3 V to VCCLOG + 0.3 V
Output voltage range, $V_{O(OUT)}$ and $V_{O(XDOWNn)}$ . . . . . – 0.3 V to 16 V
Storage temperature range, T_{str} . . . . . –40°C to 150°C
Continuous total power dissipation at (or below) T_A = 25°C . . . . . 4.7 W
Power dissipation rating at (or above) T_A = 25°C . . . . . 38.2 mW/°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GNDLOG terminal.

recommended operating conditions

dc characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Logic supply voltage, VCCLOG		4.5	5	5.5	V
Supply voltage for interface circuit, VCCIF		3.0	5	5.5	V
Supply voltage for constant current circuit, VCCLED		4.5	5	5.5	V
Analog power supply, VCCANA		4.5	5	5.5	V
Voltage between VCC, V_{DIFF1}	V_{DIFF1} = VCCLOG – VCCANA VCCLOG – VCCLED VCCANA – VCCLED	– 0.3	0	0.3	V
Voltage between GND, V_{DIFF2}	V_{DIFF2} = GNDLOG – GNDANA GNDLOG – GNDLED GNDANA – GNDLED	– 0.3	0	0.3	V
Voltage applied to constant current output, V_{OUT}	OUT0 to OUT15 off			15	V
High-level input voltage, V_{IH}		0.8 VCCLOG		VCCLOG	V
Low-level input voltage, V_{IL}		GNDLOG		0.2 VCCLOG	V
High–level output current, I_{OH}	VCCLOG = 4.5 V, DOUT0 to DOUT9, DCDOUT0 to DCDOUT5, BOUT, XGSOUT, XPOUT			– 1.0	mA
Low–level output current, I_{OL}	VCCLOG = 4.5V, DOUT0 to DOUT9, DCDOUT0 to DCDOUT5, BOUT, XGSOUT, XPOUT			1.0	
	VCCLOG = 4.5 V, XDOWN1, XDOWN2			5	mA
Constant output current, I_{OLC}	OUT0 to OUT15	5		80	mA
Operating free-air temperature range, T_A		– 20		85	°C
PLL capacitance, C_{VCO}			1		µF
PLL resistor, R_{BIAS}	At 16 MHz oscillation		22		kΩ
PLL resistor, R_{PD}			30		kΩ

ac characteristics, VCCLOG= VCCANA = VCCLED = 4.5 V to 5.5 V, T_A = – 20 to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCLK, DCCLK clock frequency, f_{DCLK}, f_{DCCLK}	At single operation			20	MHz
	At cascade operation			15	
DCLK, DCCLK pulse duration (high or low level), t_{wh}/t_{wl}		20			ns
GSCLK clock frequency, f_{GSCLK}				8	MHz
GSCLK pulse duration (high or low level), t_{wh}/t_{wl}		40			ns
WDT clock frequency, f_{WDT}				8	MHz
WDT pulse duration (high or low level), t_{wh}/t_{wl}		40			ns
XLATCH, XDCLAT pulse duration (high level), t_{wh}		30			ns
Rise / fall time, t_r/t_f				100	ns
Setup time, t_{su}	DINn – DCLK	5			ns
	DCDINn – DCCLK	5			
	BLANK – GSCLK	10			
	XENABLE – DCLK	15			
	XLATCH – DCLK	10			
	XLATCH – GSCLK	10			
	XDCLAT – DCCLK	10			
	RSEL – DCLK	10			
	RSEL – DCCLK	15			
	RSEL – XLATCH	30			
	RSEL – XDCLAT	15			
Hold time, t_h	DINn – DCLK	15			ns
	DCDINn – DCCLK	15			
	XENABLE – DCLK	20			
	XLATCH – DCLK	30			
	XDCLAT – DCCLK	20			
	RSEL – DCLK	20			
	RSEL – DCCLK	20			
	RSEL – XLATCH	20			
	RSEL – XDCLAT	10			

electrical characteristics, LEDCHK = L, MIN/MAX: VCCLOG = VCCANA = VCCLED = 4.5 V to 5.5 V, T_A = – 20 to 85°C TYP: VCCLOG = VCCANA = VCCLED = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DOUTn, DCOUTn, XGSOUT, XPOUT, BOUT I_{OH} = –1 mA	VCCLOG –0.5			V
V_{OL}	Low-level output voltage	DOUTn, DCOUTn, XGSOUT, XPOUT, BOUT I_{OL} = 1 mA			0.5	V
		XDOWN1, XDOWN2 I_{OL} = 5 mA			0.5	
I_I	Input current	V_{IN} = VCCLOG or GNDLOG			± 1	µA
I_{LOG}	Supply current (logic)	Input signal is static, TSENA = H, WDCAP = OPEN, No PLL is used			0.1	mA
		Input signal is static, TSENA = H, WDCAP = OPEN, PLL multiple ratio = 1042			1	mA
		Data transfer, DCLK = 20 MHz, GSCLK = 8 MHz No PLL is used		35	45	
		Data transfer, DCLK = 20 MHz, GSCLK = 15 kHz PLL multiple ratio = 1042		39	49	mA
I_{ANA}	Supply current (analog)	BLANK = L, R_{IREF} = 1200 Ω		6.5	8	mA
		BLANK = L, R_{IREF} = 600 Ω		13	15	
I_{LED}	Supply current (constant current driver)	LED turn off, R_{IREF} = 1200 Ω		12	20	mA
		LED turn off, R_{IREF} =600 Ω		20	35	
		V_{OUT} = 1V, R_{IREF} = 1200Ω All output bits turn on		12	20	
		V_{OUT} = 1V, R_{IREF} = 600 Ω All output bits turn on		20	35	
I_{OLC1}	Constant output current (includes error between bits)	V_{OUT} = 1V, V_{IREF} = 1.21 V, R_{IREF} = 1200Ω	35	40	45	mA
I_{OLC2}	Constant output current (includes error between bits)	V_{OUT} = 0.7 V, V_{IREF} = 1.21 V, R_{IREF} = 600 Ω	70	80	90	mA
I_{OLK}	Constant output leakage current	OUT0 to OUT15 (V_{OUTn} = 15 V)			0.1	µA
		XDOWN1,2 (V_{XDOWNn} = 15 V)			1	µA
		DOUTn, DCDOUTn (V_{OUTn} = VCCLOG or GND)			1	µA
ΔI_{OLC}	Constant output current error between bit	VCCLOG=VCCANA=VCCLED= 5 V, V_{OUT} = 1 V, R_{IREF} = 600 Ω All output bits turn on		± 1%	± 4%	
$I_{\Delta OLC1}$	Changes in constant output current depend on supply voltage	V_{OUT} = 1V, R_{IREF} = 600 Ω, V_{IREF} = 1.21 V		± 1	± 4	%/V
$I_{\Delta OLC2}$	Changes in constant output current depend on output voltage	V_{OUT} = 1 V to 3 V, R_{IREF} = 600 Ω, V_{IREF} = 1.21 V, 1 bit output turn on		± 1	± 3	%/V
T_{tsd}	TSD detection temperature	Junction temperature	150	160	170	°C
T_{wdt}	WDT detection temperature	No external capacitor	5	10	15	ms
V_{IREF}	Voltage reference	BCENA = L, R_{IREF} = 590 Ω,		1.21		V
V_{LEDDET}	Voltage applied to LED disconnection detection		0.2	0.3	0.4	V
$P_{LLJITTER}$	PLL jitter	R_{BIAS} = 22 kΩ, R_{PD} = 30 kΩ, C_{VCO} = 0.1 µF		0.4%	2%	

switching characteristics, C_L = 15pF,
MIN/MAX: VCCLOG= VCCANA = VCCLED = 4.5 V to 5.5 V, T_A = – 20 to 85°C,
TYP: VCCLOG = VCCANA = VCCLED = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	DOUTn, DCDOUTn		12	30	ns
		XGSOUT, BOUT, XPOUT		12	30	
		OUTn (see Figure 1)		110		
t_f	Fall time	DOUTn, DCDOUTn		10	30	ns
		XGSOUT, BOUT, XPOUT		10	30	
		OUTn (see Figure 1)		130		
t_d	Propagation delay time	OUTn+1 – OUTn		30	45	ns
		BLANK↑ – OUT0	40	50	105	
		BLANK – BOUT	10	20	40	
		GSCLK – OUT0 (see Note 2)		7		
		GSCLK – XGSOUT	10	20	40	
		DCLK – DOUTn	15	30	45	
		DCLK – DCDOUTn	15	30	45	
		DCCLK – DCDOUTn	15	30	45	
		XOE↓ – DOUTn (see Note 3)	10	20	35	
		XOE↑ – DOUTn (see Note 3)	10	15	25	
		RSEL – DOUTn	10	20	40	
		LEDCHK – XDOWN2			1000	

NOTES: 2. MAG0 to MAG2 are all low level.
3. Until DOUT will be turned on (drive) or turned off (Hi-Z).

PARAMETER MEASUREMENT INFORMATION

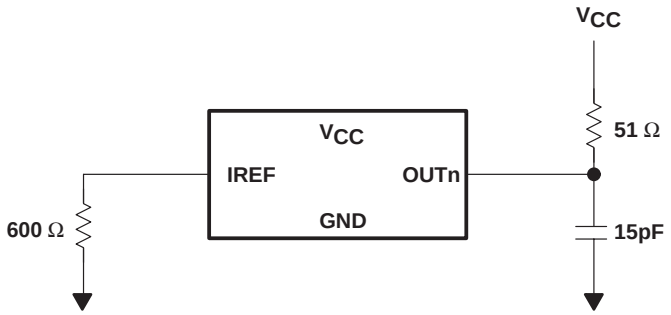


Figure 1. Rise Time and Fall Time Test Circuit for OUTn

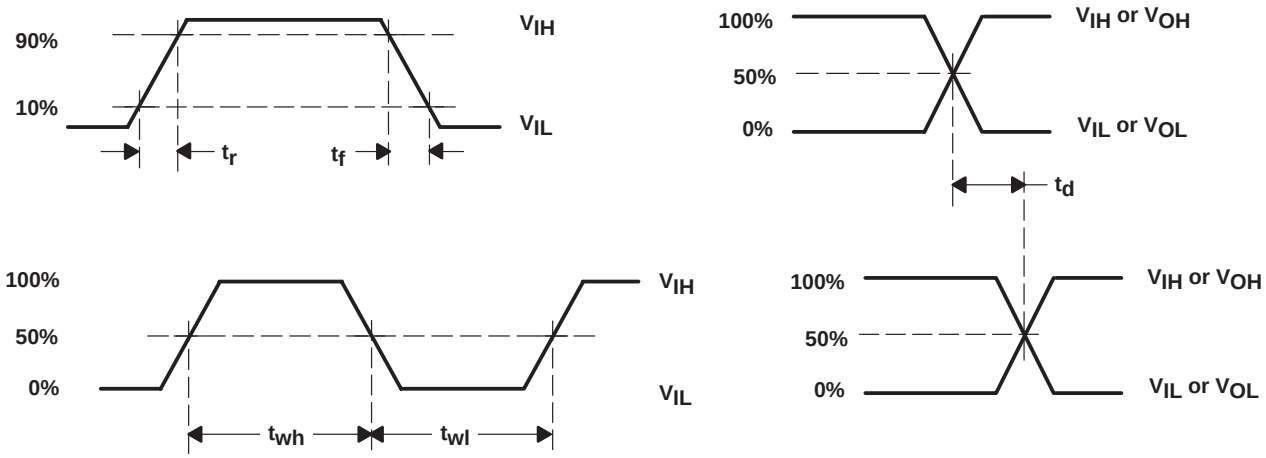


Figure 2. Timing Requirements

PRINCIPLES OF OPERATION

setting for output constant current value

On the constant current output terminals (OUT0–15), approximately 38 times the current which flows through external resistor, R_{IREF} (connected between IREF and GND), can flow. The external resistor value is calculated using the following equation:

$R_{IREF}\ (\Omega) \cong 38 \times 1.21\ (V)/I_{O(LC)}(A)$ where both BCENA and DCENA are low.

Note that more current flows if IREF is connected to GND directly.

constant output current operation

If GSPOL is high, the constant current output turns on the sink constant current if all the gray scale data in the gray scale latch is not zero on the falling edge of the gray scale clock after the next rising edge of the gray scale clock when BLANK goes from high to low. After that, the number of the falling edge is counted by the 10 bit gray scale counter. Then, the output counted corresponding to the gray scale data is turned off (stop to sink constant current). The gray scale clock can be selected from GSCLK or that generated by internal PLL circuitry. If the shift register for gray scale is updated during XLATCH high, data on the gray scale data latch is also updated affecting the constant current output number of the gray scale. Accordingly, during the on-state of the constant current output, keep the XLATCH to a low level and hold the gray scale data latch.

input/output port and shift register selection

The TLC5910 supplies two parallel input ports such as DIN (10 bits) and DCDIN (6 bits). The DIN and DCDIN ports also supply DCLK and DCCLK for shift clock, XLATCH and XDCLAT for latch, and DOUT and DCDOUT for output, respectively. The device has three types of shift register latches, gray scale data, brightness control, and dot correction. The port and shift register can be selected by RSEL0 and RSEL1. Table 1 shows the selection using RESL0 and RSEL1. Note that the RSELn setting should be done at DCLK low, (when DPOL is high, and at DCLK high when DPOL is low). When only port A is used, DCDIN, DCDOUT, DCCLK, and XDCLAT should be connected to GND.

Table 1. Shift Register Latch Selection

SELECTED SHIFT REGISTER LATCH				
RSEL1	RSEL0	PORT A	PORT B	
		DIN, DCLK, XLATCH, DOUT	DCDIN, DCCLK, XDCLATCH	DCDOUT
L	L	Gray scale data displayed	Dot correction	Dot correction
L	H	Brightness control	Dot correction	Dot correction
H	L	Dot correction (see Note)	Not connected	Dot correction
H	H	N/A (inhibit)	N/A (inhibit)	N/A (inhibit)

NOTE: Zero is output to DOUT6 to DOUT9.

shift register latch for gray scale data

The shift register latch for gray scale data is configured with 16 x 10 bits. The gray scale data, configured with 10 bits, represents the time when constant current output is being turned on, and the data range is 0 to 1023 (00h to 3FFh). When the gray scale data is 0, the time is shortest, and the output is not turned on(light off). When the gray scale data is 1023, the time is longest, and it turns on during time of 1023 clocks from the gray scale clock. The configuration of the shift register and latch for gray scale data is shown in Figure 3.

PRINCIPLES OF OPERATION

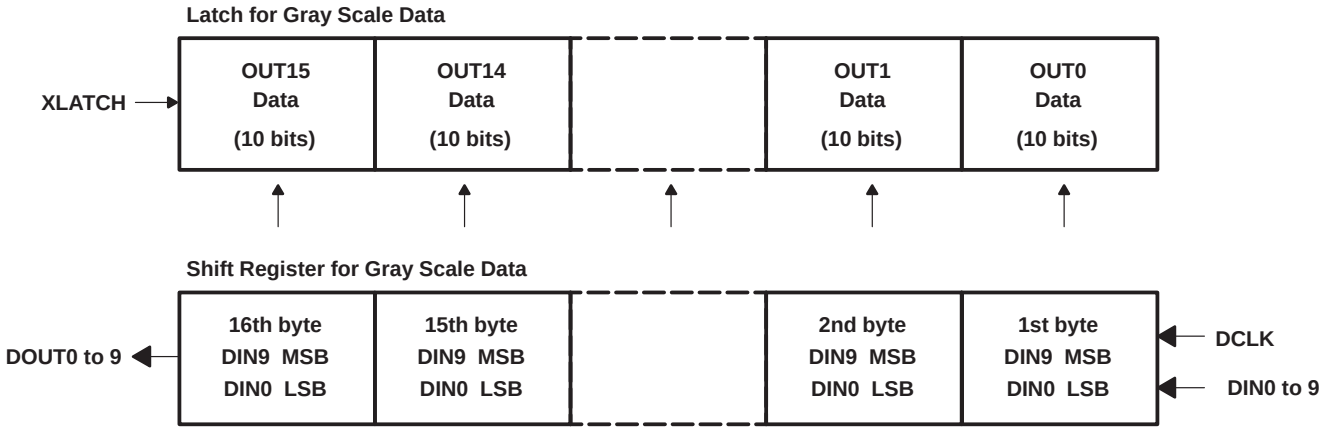
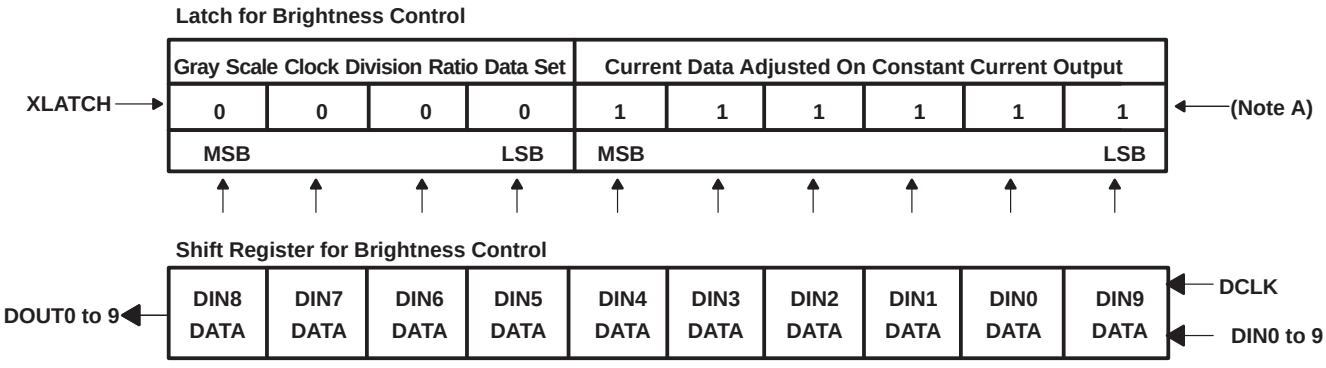


Figure 3. Relationship Between Shift Register and Latch for Gray Scale Data

shift register latch for brightness control

The shift register latch for brightness control is configured with 1 × 10 bits. Using the shift register latch for brightness control, the division ratio of the gray scale clock can be set and the output current value on constant current output can be adjusted. When powered up, the latch data is indeterminate and the shift register is not initialized. Data should be written to the shift register latch prior to lighting-on (BLANK=L) when these functions are used. Also, the latch value for brightness control cannot be rewritten when the constant current output is turned on. When these functions are not used, the latch value can be set to the default value setting BCENA to low level (connect to GND). Also, DIN9 is assigned to the LSB of the reference current control to maintain the compatibility with TLC5901/02/03 family. The configuration of the shift register and the latch for brightness control is shown below.



Note A: Indicates default value at BCENA low.

Figure 4. Relationship Between Shift Register and Latch for Brightness Control

shift register latch for dot correction

The shift register latch for dot correction is configured with 16 × 6 bits. Using the shift register latch for dot correction, the current value on the constant current output can be set individually. When powered up, the latch data is indeterminate and the shift register is not initialized. Data should be written to the shift register latch prior to lighting-on (BLANK=L) when these functions are used. Also, the latch value for dot correction cannot be rewritten when the constant current output is turned on. When these functions are not used, the latch value can be set to the default value setting of DCENA to low level (connect to GND). The configuration of the shift register and the latch for dot correction is shown in Figure 5.

PRINCIPLES OF OPERATION

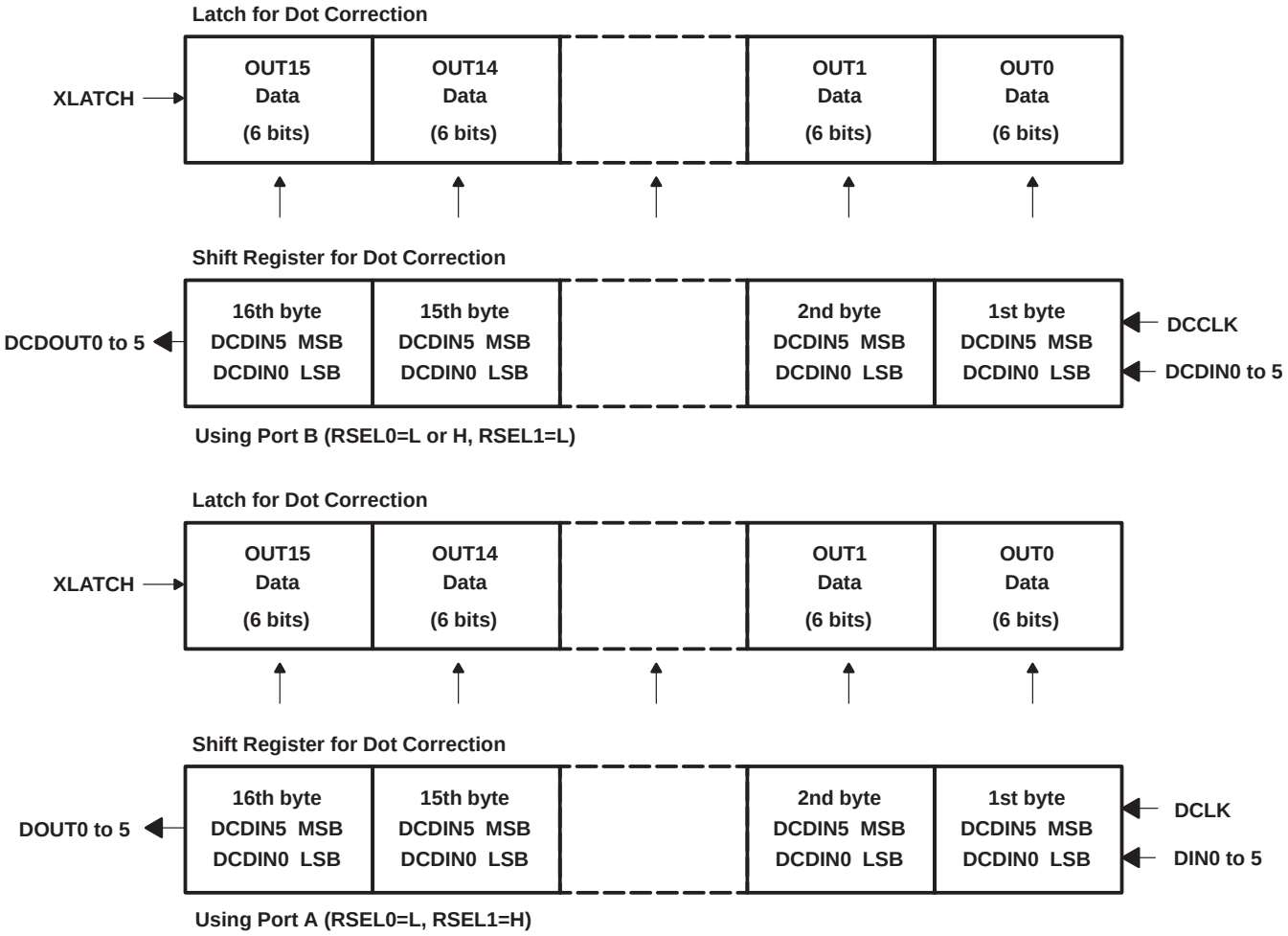


Figure 5. Relationship Between Shift Register and Latch for Dot Correction

write data to shift register latch

The shift register latch written to is selected using the RSEL0 and RSEL1 terminals. At port A, the data is applied to the DIN data input terminal and clocked into the shift register synchronizing to the rising edge of DCLK after XENABLE is pulled low. At port B, the data is applied to the DCDIN data input terminal and clocked into the shift register synchronizing to the rising edge of DCCLK. The shift register for the gray scale data is configured with 16 × 10 bits and the shift register for dot correction is configured with 16 x 6 bits resulting in sixteen times DCLK, and the shift register for brightness control is configured with 1 x 10 bits resulting in one times DCLK. At number of DCLK input for each case, data can be written into the shift register. In this condition, when XLATCH at port A or XDCLAT at port B is pulled high, data in the shift register is clocked into latch (data through), and when XLATCH at port A or XDCLAT at port B is pulled low, data is held (latch).

PRINCIPLES OF OPERATION

brightness control function

By writting data into the brightness control latch, the current on all constant current outputs can be adjusted to control the variation of brightness between ICs and the division ratio for the gray scale clock can be set to control the variation of brigtness for the total panel system. Furthermore, by writing data into the dot correction latch, the current on each constant current output can be adjusted.

output current adjustment on all constant current outputs – brightness adjustment between ICs

By using the lower 6 bits of the brightness control latch, the output current can be adjusted to 64 steps. 1 step of 0.8% current ratio between 100% and 50.8% when the set output current is 100% by an external resistor (note that the current value is lower if the constant current output is corrected using the dot correction function). By using this function, the brightness control between modules (ICs) can be adjusted sending the desired data externally even if the ICs are mounted on a print-circuit board. When BCENA is pulled low, output current is set to 100%.

Table 2. Relative Current Ratio For Total Constant Current Output

CODE	CURRENT RATIO (%)	20 (mA)	80 (mA)	V_{IREF} (TYP)
MSB 000000 LSB	50.8	10.2	40.6	0.61
. . . .	. . . .	. . . .	. . . .	. . . .
111110	99.2	19.8	79.7	1.20
111111†	100	20.0	80.0	1.21

† BCENA is low.

frequency division ratio setting for gray scale clock – panel brightness adjustment

By using the upper 4 bits of the brightness control latch, the gray scale clock can be divided into 1/1 to 1/16. If the gray scale clock is set to 16 times the speed (1024×16=16384) of frequency during horizontal scanning time, the brightness can be adjusted to 16 steps selecting the frequency division ratio. By using this function, the total panel brightness can be adjusted at once, and it applies to the brightness of day or night circumstances. When BCENA is pulled low, the gray scale clock is not divided. When BCENA is pulled high, the brightness can be adjusted (see Table 3).

Table 3. Relative Brightness Ratio For Total Constant Current Output

CODE	FREQUENCY DIVISION RATIO	RELATIVE BRIGHTNESS RATIO (%)
MSB 0000 LSB†	1/1	6.3
. . . .	. . . .	. . . .
1110	1/15	93.8
1111	1/16	100

† BCENA is low.

PRINCIPLES OF OPERATION

output current adjustment on each constant current output – LED brightness adjustment

By using the 6 bits of the dot correction latch, the output current on each constant current output can be adjusted to 64 steps. 1 step of 0.8% current ratio between 100% and 50.8% when the set output current is 100% by an external resistor at 111111h of the latched value and the lower 6 bits of the brightness control register. By using this function, the brightness deviation due to LED brightness variation can be minimized. When DCENA is pulled low, the output current is set to 100% without dot correction.

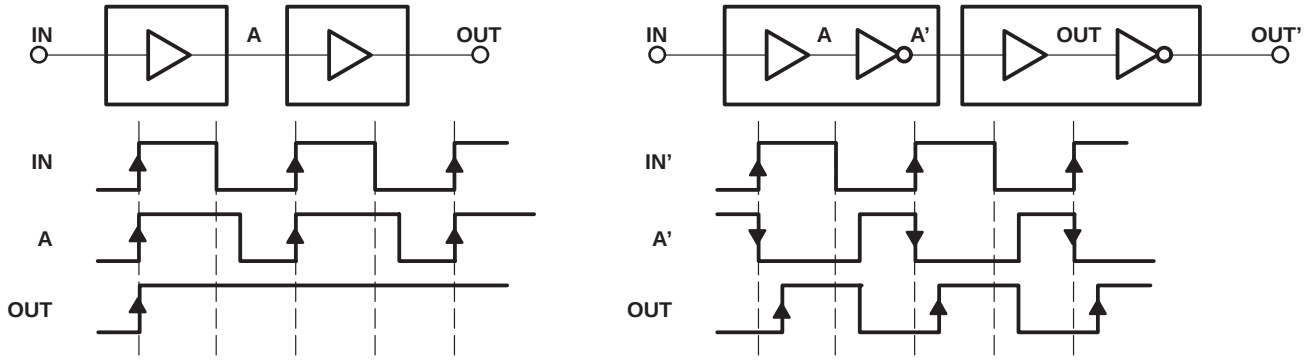
Table 4. Relative Current Ratio By Constant Current Output

CODE	CURRENT RATIO (%)	I_{OLC}=40 (mA)
MSB 000000 LSB	50.8	20.3
. . . .	. . . .	. . . .
111110	99.2	39.7
111111†	100	40

† DCENA is low.

clock edge selection

The high speed clock signal is delayed due to the duty ratio change through multiple stages of an IC or through the module stages shown in Figure 6.



a) Propagate through multiple stages buffer with slow falling edge

b) Insert inverter between buffers

Figure 6. Clock Edge Selection

As shown in Figure 6 a), if the falling at the internal buffer is behind the rising, the clock will disappear as multiple cascade connections are made. To resolve this problem, the duty ratio can be held unchanged using the connection as shown in Figure 6 b) if the valid clock edge can be selected (arrow in Figure 6). Note that the clock delay is not avoided even in this case.

The device incorporates the clock edge selection function for each DCLK and GSCLK. By using this function, the falling edge or rising edge for the valid edge can be selected depending on the status of DPOL and GSPOL. Thus the degradation for the duty ratio can be reduced. The relation between each signals is shown in Table 5.

PRINCIPLES OF OPERATION

clock edge selection (continued)

Table 5. Valid Edge For DCLK and GSCLK

DPOL	DCLK valid edge	Operation at XENABLE = H
H	DCLK↑	Pull DCLK to low level
L	DCLK↓	Pull DCLK to high level

GSPOL	GSCLK valid edge	PLL operation
H	GSCLK↑	Synchronize to the high level of DCLK
L	GSCLK↓	Synchronize to the low level of DCLK

The device supplies XPOUT and XGSOUT output terminals for the cascade operation which invert GSPOL and GSCLK respectively. It also supplies the BOUT output terminal as a buffered BLANK to make easy timing with GSCLK and XGSOUT.

gray scale clock generation

When MAG<0:2> are all low, the clock input from GSCLK terminal is used as the gray scale clock with no change, and except for this case internal PLL generates the clock for the gray scale control clock. When using the PLL, the gray scale clock is generated by adjusting the clock having the same number of pulses as the multiple ratio of the GSCLK reference period (when GSCLK and GSPOL are keeping the same level). Note that the reference period is required above 40% of the GSCLK period. The ratio in this case is determined depending on MAG 0 to MAG 2 as shown in Table 6.

When using PLL, internal PLLCLK is clocked out at the XGSOUT terminal. Therefore, this clock can be utilized for other devices on the same print-circuit board. Note that the number of ICs connected is limited depending on the frequency.

Table 6. PLL Multiple Ratio

MAG2	MAG1	MAG0	MULTIPLE RATIO	XGSOUT
L	L	L	1 (Signal to control GSCLK by GSPOL)	Inverted GSCLK
L	L	H	2^8+6(=262)	PLLCLK (Gray scale clock internally generated)
L	H	L	2^9+10(=522)	
L	H	H	2^{10}+18(=1042)	
H	L	L	2^{11}+34(=2082)	
H	L	H	2^{12}+66(=4162)	
H	H	L	2^{13}+130(=8322)	
H	H	H	2^{14}+258(=16642)	

PRINCIPLES OF OPERATION

gray scale clock generation (continued)

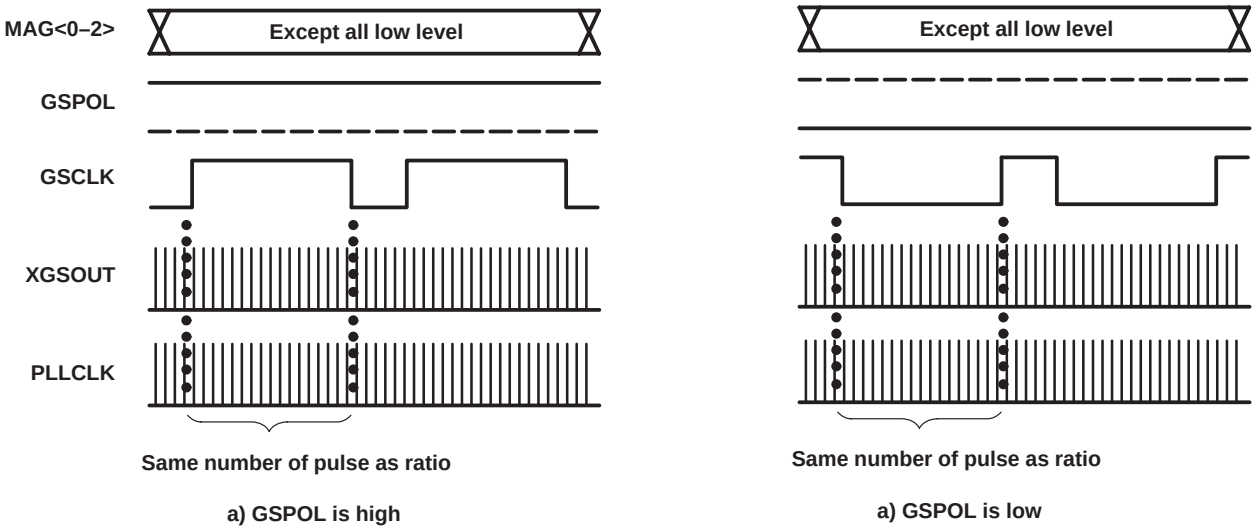


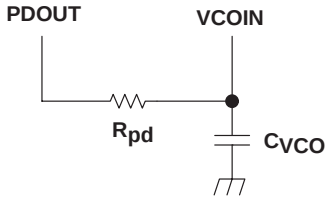
Figure 7. Gray Scale Clock Generation

The oscillation frequency bandwidth as referenced for PLL can be set by an external resistor connected between RBIAS and GND. The relation between the external resistor and oscillation frequency is shown in Table 7.

Table 7. PLL Oscillation Frequency

RBIAS	22 kΩ	30 kΩ	62 kΩ	120 kΩ
FREQUENCY	13 to 20 MHz	8 to 14 MHz	4 to 9 MHz	3 to 5 MHz

To make PLL stabilization, a resistor and acapacitor connection is required between VCOIN, PDOUT, and GND. The recommended value is shown in the following table in Figure 8.



	C_{VCO}	R_{pd}
Recommeded Value	0.1 to 1 μF	22 to 62 kΩ

Figure 8. Resistor and Capacitor Connection

PRINCIPLES OF OPERATION

protection

This device incorporates WDT and TSD functions. If WDT or TSD functions, the constant current output is stopped and XDOWN1 goes low. Therefore, by monitoring the XDOWN1 terminal, these failures can be detected immediately. Since the XDOWN1 output is configured as an open collector, outputs of multiple ICs are brought together.

WDT (watchdog timer)

The constant current output is forced to turn off and XDOWN1 goes low when the fixed period elapses after the signal applied to WDTRG has not been changed. Therefore, by connecting a scan signal (signal to control line displayed) to WDTRG, the stop of the scan signal can be detected and the constant current output is turned off. This prevents the LED from burning and damage caused by continuous LED turnon at the dynamic scanning operation. The detection time can be set using an external capacitor, Cext. The typical value is approximately 10 ms without a capacitor, 160 ms with a 1000 pF capacitor, and 1500 ms with a0.01 μF capacitor. During static operation, the WDT function is disabled connecting WDCAP to GND (high or low level should be applied to WDTRG). Note that normal operations will resume changing the WDTRG level when WDT functions.

WDT operational time: T (ms) ≅ 10 + 0.15 × Cext (pF)

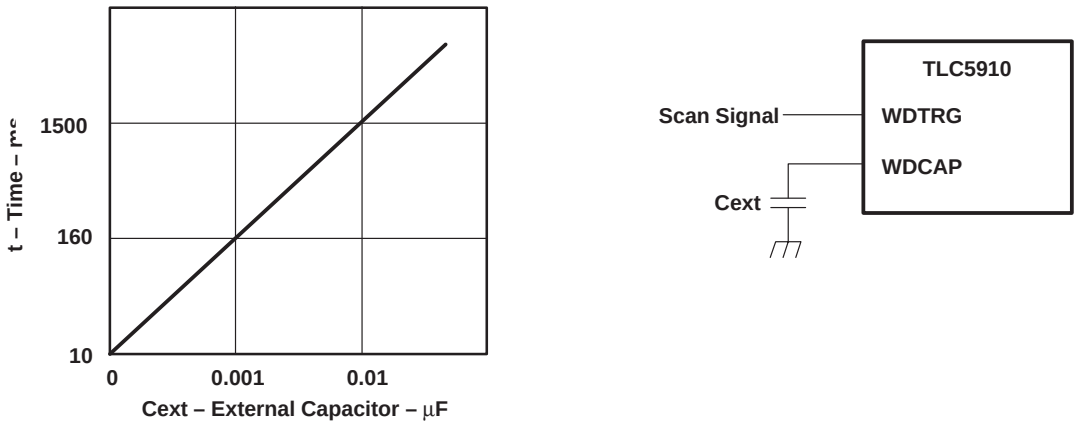


Figure 9. WDT Operational Time and Usage Example

TSD (thermal shutdown)

When the junction temperature exceeds the limit, TSD starts to function and turns constant current output off, and XDOWN1 goes low. When TSD is used, TSENA should be pulled high. When TSD is not used, TSENA should be pulled low. To recover from constant current output off-state to normal operation, the power supply should be turned off or TSENA should be pulled low once.

PRINCIPLES OF OPERATION

LOD function (LED open detection)

When LEDCHK is low, the LED disconnection detection function is disabled and XDOWN2 goes to a high-impedance state. When LEDCHK is high, the LED disconnection detection function is enabled, and XDOWN2 goes low if any LED is disconnected monitoring OUTn terminals to be turned on. This function is operational for sixteen OUTn terminals individually. To know which constant current output is disconnected, the level of XDOWN2 is repeatedly checked 16 times from OUT0 to OUT15 turning one constant current output on. The power supply voltage should be set so the constant current output is applied to above 0.4 V when the LED is lighting normally. Also, since the time of approximately 1000 ns is required from turning the constant current output on to XDOWN2 output, the gray scale data to be turned on during that period should be applied.

Table 8 is an example for XDOWN2 output status using four LEDs .

Table 8. XDOWN2 Output Example

LED NUMBER	1	2	3	4
LED STATUS	GOOD	NG	GOOD	NG
OUTn	ON	ON	ON	ON
XDOWN2	LOW (by case 2, 4)			
LED NUMBER	1	2	3	4
LED STATUS	GOOD	NG	GOOD	NG
OUTn	ON	ON	OFF	OFF
DETECTION RESULT	GOOD	NG	GOOD	GOOD
XDOWN2	LOW (by case 2)			
LED NUMBER	1	2	3	4
LED STATUS	GOOD	NG	GOOD	NG
OUTn	OFF	OFF	OFF	OFF
DETECTION RESULT	GOOD	GOOD	GOOD	GOOD
XDOWN2	HIGH–IMPEDANCE			

noise reduction

concurrent switching noise reduction

Concurrent switching noise has the potential to occur when multiple outputs turn on or off at the same time. To prevent this noise, the device has a delay output terminal such as XGSOUT and BOUT for GSCLK (gray scale clock) and BLANK (blanking signal) respectively. Connecting these outputs to the GSCLK and BLANK terminals of next stage IC allows differences of the switching time between ICs. When GSCLK is output to GSOUT through the device, duty will be changed between input and output. The number of stages to be connected will be limited depending on frequency.

delay between constant current output

The constant current output has a delay time of approximately 20 ns between outputs. This means approximately 300 ns delay time exists between OUT0 and OUT15. This time differences by delay reduces the concurrent switching noise.

PRINCIPLES OF OPERATION

power supply

The followings should be taken into consideration:

- VCCLOG, VCCANA and VCCLED should be supplied by a single power supply to minimize voltage differences between these terminals.
- The bypass capacitor should be located between the power supply and GND to eliminate the variation of power supply voltage.

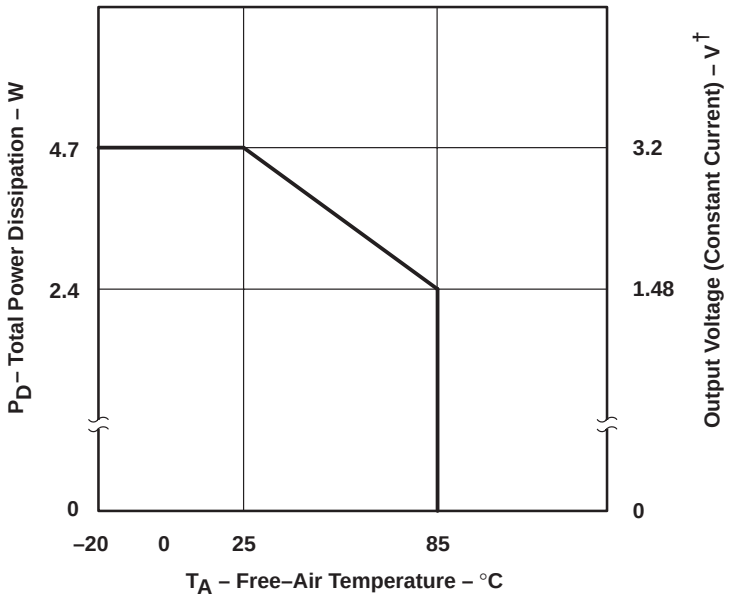
GND

Although GNDLOG, GNDANA, and GNDLED are internally tied together, these terminals should be externally connected to reduce noise influence.

thermal pad

The thermal pad should be connected to GND to eliminate the noise influence when it is connected to the bottom side of IC chip. Also, the desired thermal effect will be obtained by connecting this pad to the PCB pattern with better thermal conductivity.

power rating – free-air temperature



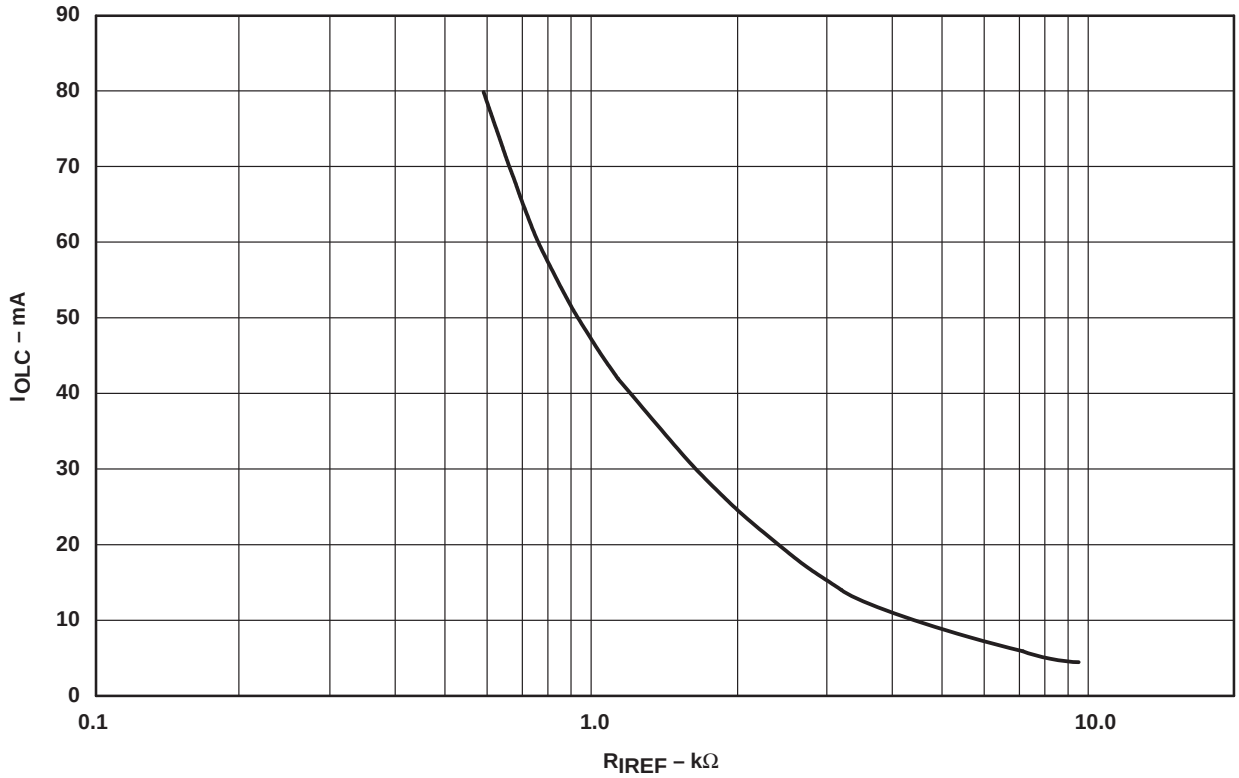
† VCCLOG=VCCANA=VCCLED=5.0V, I_{OLC} = 80mA, I_{CC} is typical value.

NOTES: A. IC is mounted on PCB.
PCB size: 102 × 76 x 1.6 [mm^3], four layers with the internal two layer being plane. The thermal pad is soldered to the PCB pattern of 10 × 10 [mm^2]. For operation above 25°C free-air temperature, derate linearly at the rate of 38.2 mW/°C.
B. The thermal impedance will be varied depending on mounting conditions. Since the PZP package established low thermal impedance by radiating heat from the thermal pad, the thermal pad should be soldered to the pattern with a low thermal impedance.
C. Consider thermal characteristics when selecting the material for the PCB, since the temperature will rise around the thermal pad.

Figure 10. Power Rating

PRINCIPLES OF OPERATION

constant output current



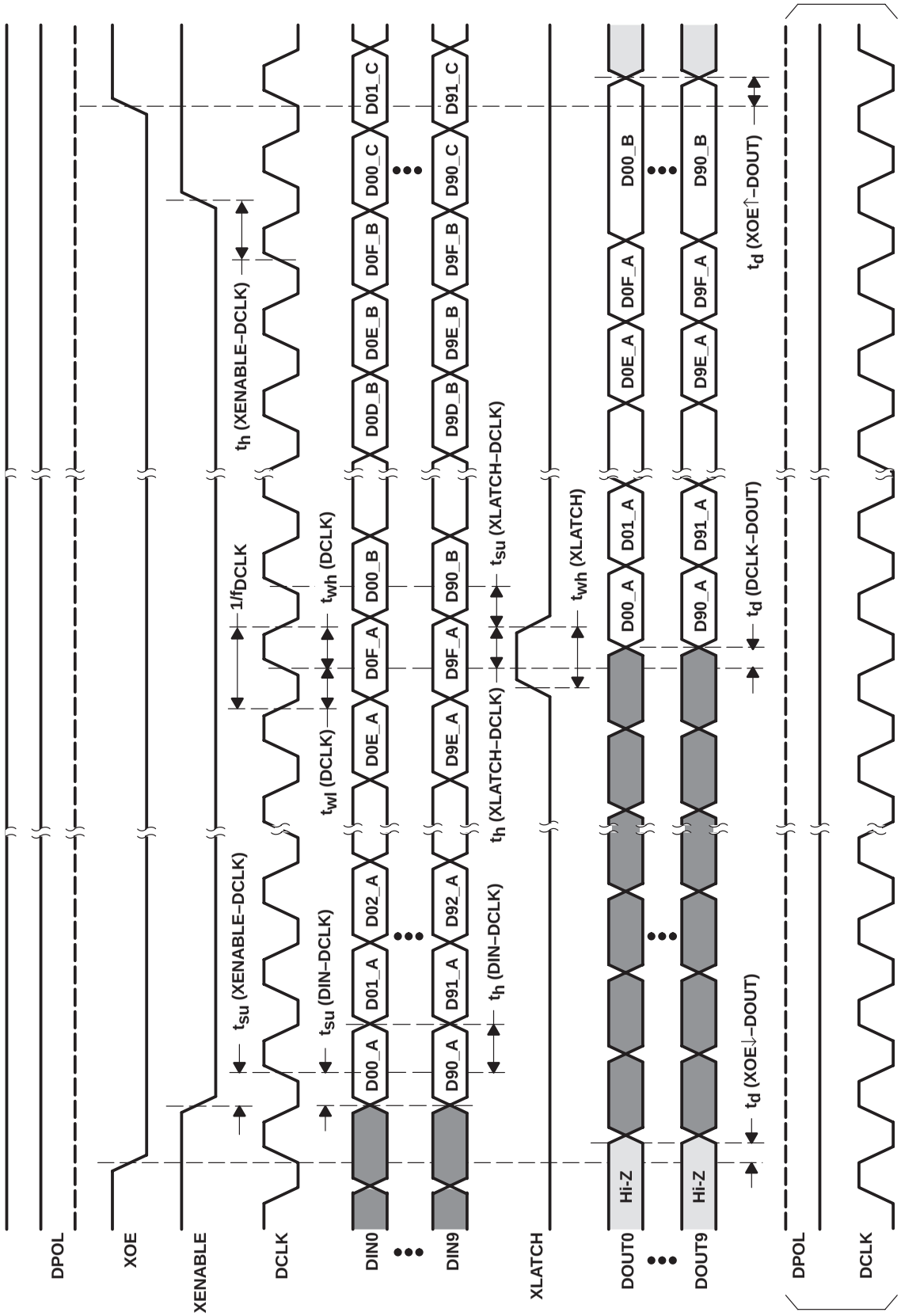
Conditions: V_{OUT} = 1.0V, V_{IREF} = 1.21V

$$I_{OLC}(mA) \quad \frac{V_{IREF}(V)}{R_{IREF}(k\Omega)} \times 38$$

$$R_{IREF}\ (k\Omega) \cong \frac{47}{I_{OLC}(mA)}$$

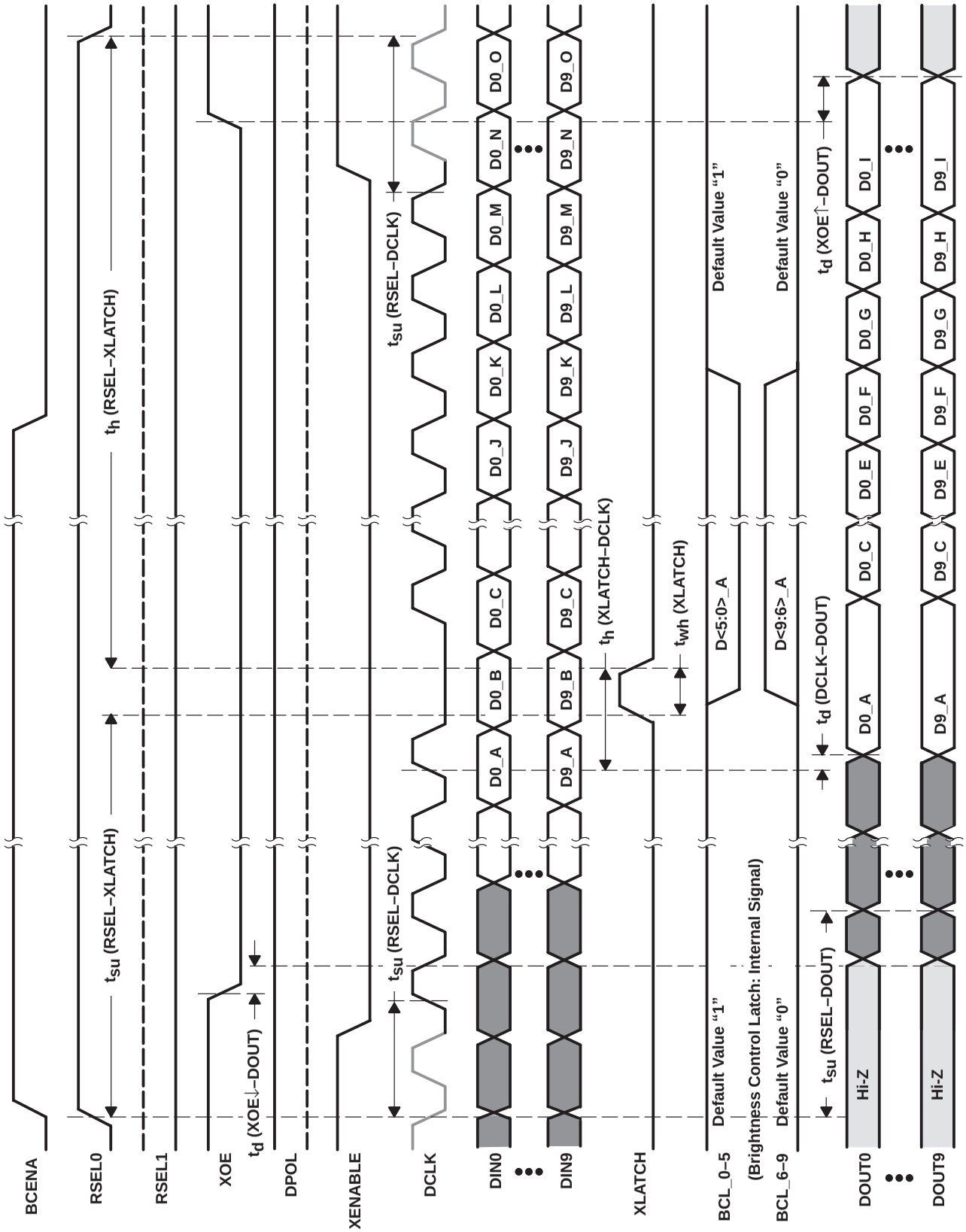
NOTE: The brightness control and dot corrected value are 100%. The resistor, R_{IREF}, should be located as close to the IREF terminal as possible to avoid the noise influence.

Figure 11. Current on Constant Current Output vs External Resistor



DPOL and DCLK can be replaced with the combination of these signals enclosed by the parenthesis (Both are inverted with each other).

Figure 12. Timing Diagram (Shift Register for Gray Scale Data)



DPOL and DCLK can be replaced with signals inverted with each other. Same as the shift register for the gray scale data.

Figure 13. Timing Diagram (Shift Register for Brightness Control)

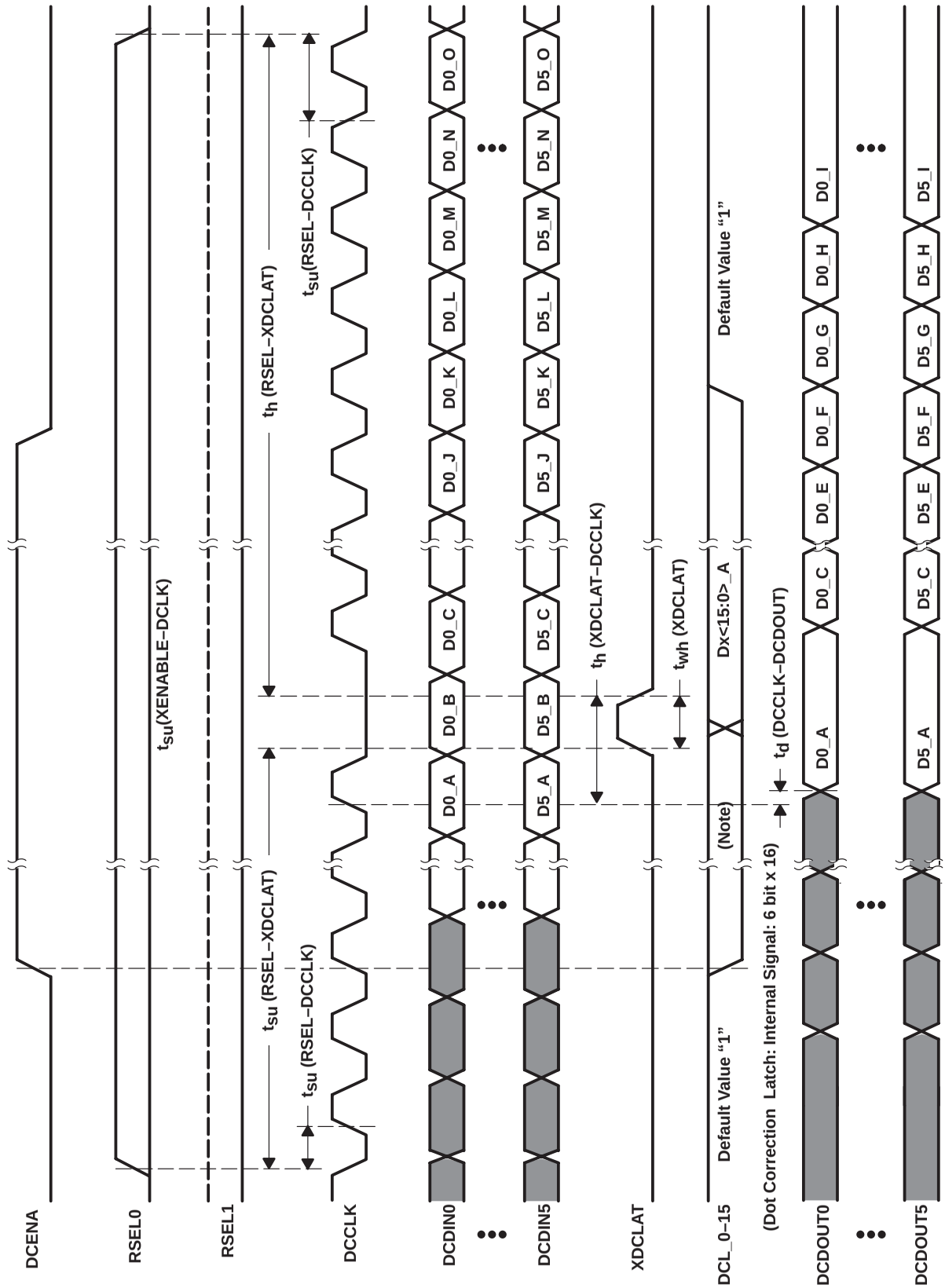
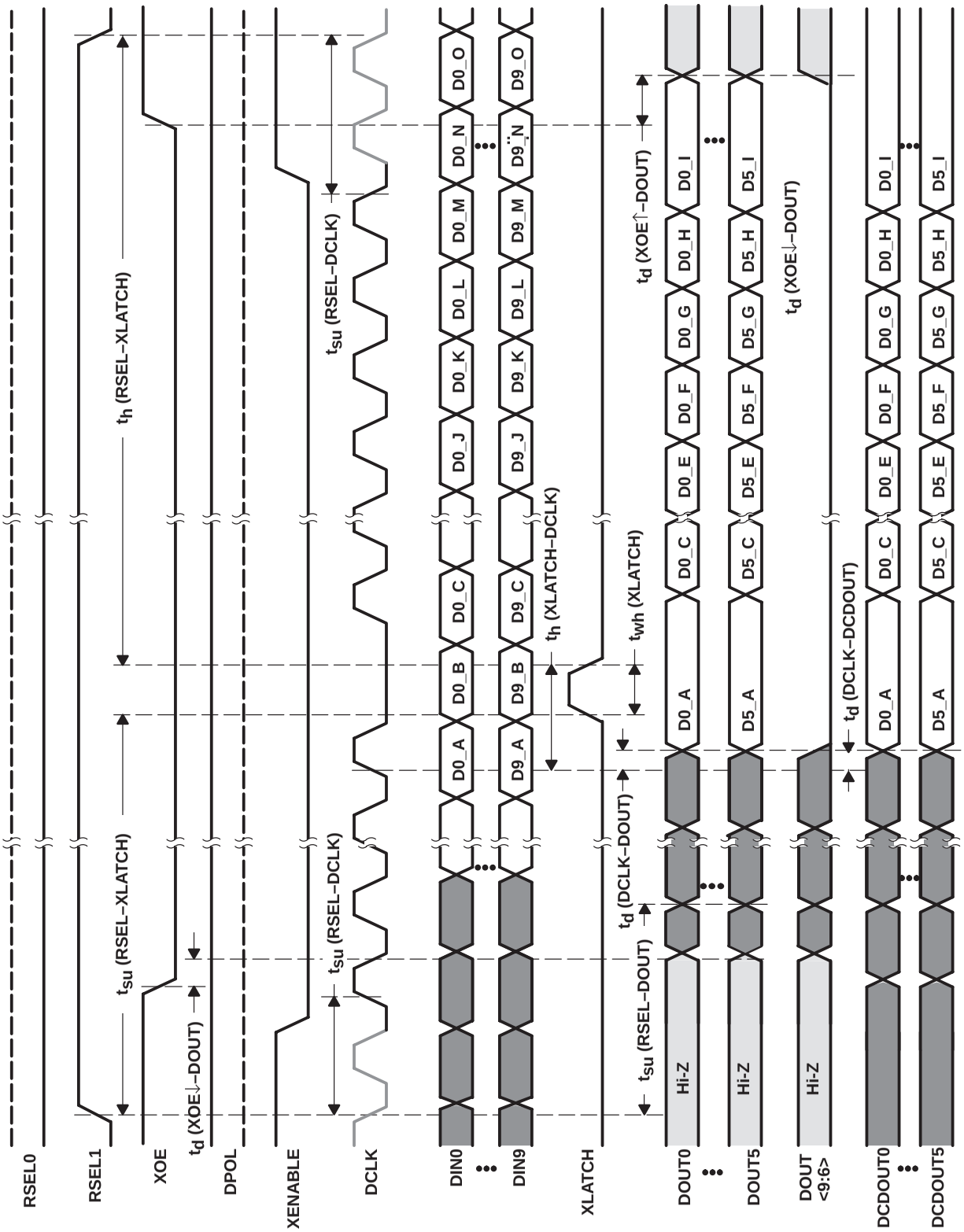


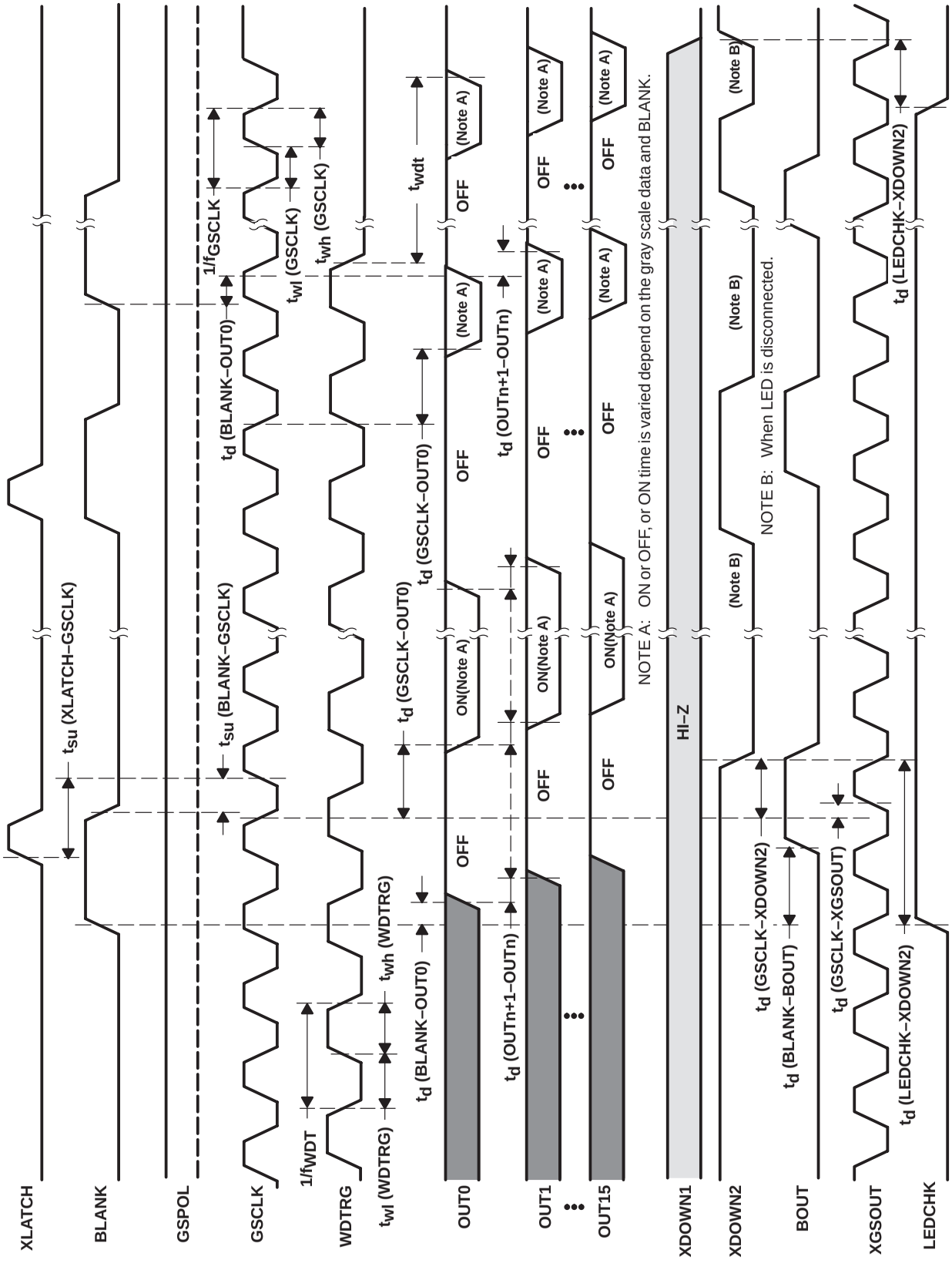
Figure 14. Timing Diagram (Shift Register for Dot Correction : Using Port B)

NOTE: Register value is immediately before DCLAT↓.



DPOL and DCLK can be replaced with signals inverted with each other. Same as the shift register for the gray scale data.

Figure 15. Timing Diagram (Shift Register for Dot Correction : Using Port A)



NOTE A: ON or OFF, or ON time is varied depend on the gray scale data and BLANK.

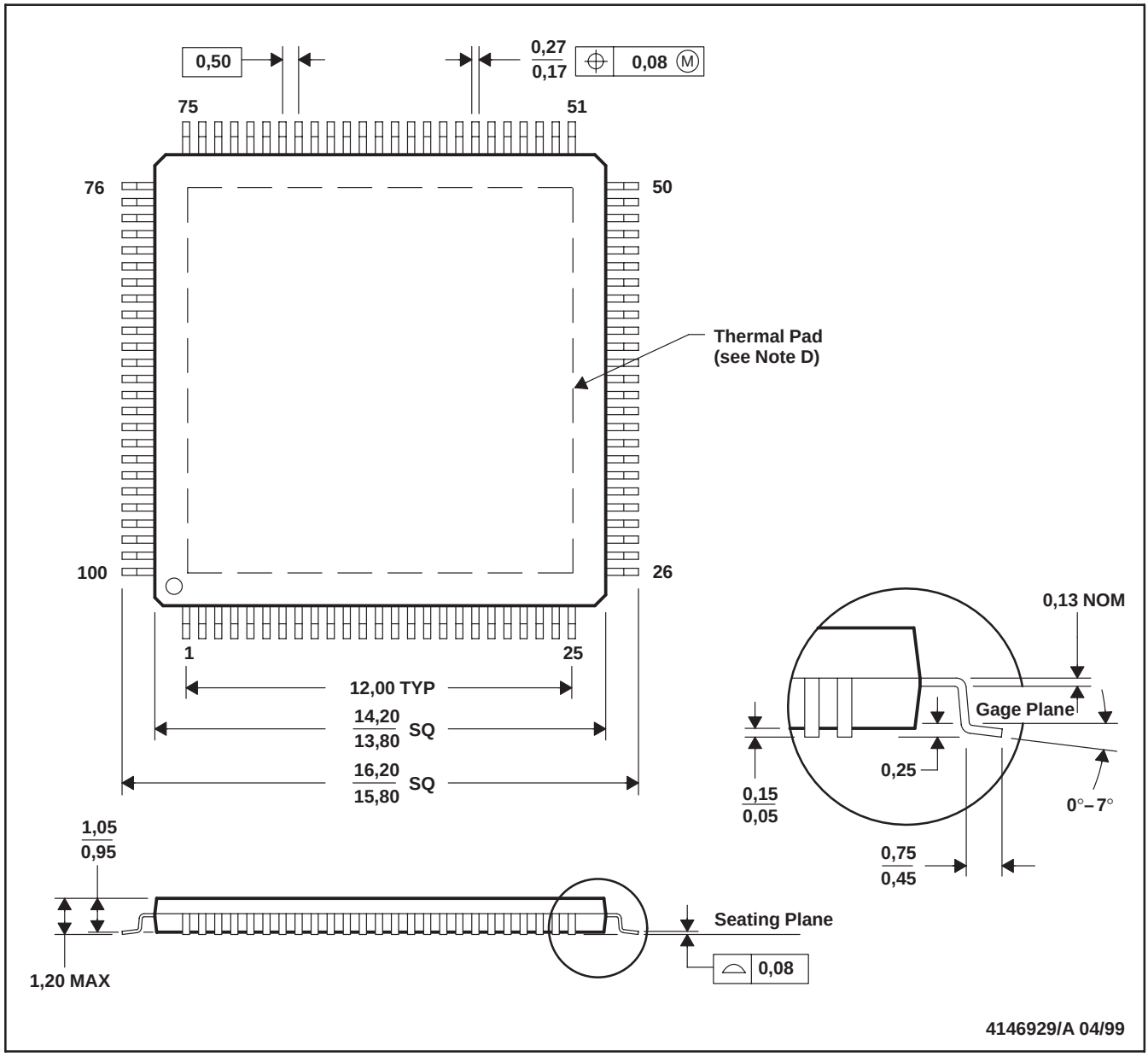
NOTE B: When LED is disconnected.

GSPOL, GSCLK and XGSOUT can be replaced with signals inverted with each other.

Figure 16. Timing Diagram (Constant Current Output) – MAG0 to MAG2 are all zero

MECHANICAL DATA

PZP (S-PQFP-G100) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads.. The demensions of the thermal pad are 2 mm x 2 mm. The pad is centered on the bottom of the package.
E. Falls within JEDEC MS-026

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC5910PZP	OBSOLETE	HTQFP	PZP	100		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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