

- Member of the Texas Instruments Widebus+™ Family
- Supports SSTL_2 Data Inputs
- Outputs Meet SSTL_2 Class II Specifications
- Differential Clock Inputs (CLK and $\overline{\text{CLK}}$)
- Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Flow-through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description

This 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The SN74SSTV32877 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level. When $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ are high, the outputs are in the high-impedance state.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.



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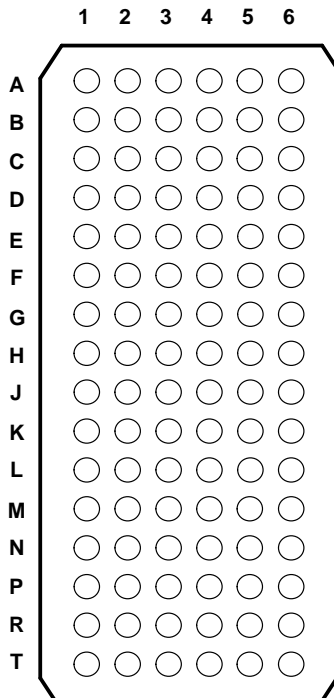
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SN74SSTV32877
26-BIT REGISTERED BUFFER
WITH SSTL_2 INPUTS AND OUTPUTS

Obsolete Device

SCES378B – OCTOBER 2001 – REVISED MAY 2002

GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	D1	V _{CC}	GND	V _{DDQ}	Q1	Q2
B	D3	D2	V _{REF}	GND	Q3	Q4
C	D5	D4	NC	GND	Q5	Q6
D	D7	D6	GND	V _{DDQ}	Q7	Q8
E	D9	D8	V _{CC}	GND	Q9	V _{DDQ}
F	D11	D10	GND	V _{DDQ}	Q10	GND
G	D13	D12	V _{CC}	V _{DDQ}	Q12	Q11
H	D15	D14	GND	GND	GND	Q13
J	CLK	NC	GND	GND	GND	Q14
K	$\overline{\text{CLK}}$	$\overline{\text{RESET}}$	V _{CC}	V _{DDQ}	Q15	Q16
L	D16	D17	GND	V _{DDQ}	Q17	GND
M	D18	D19	V _{CC}	GND	Q18	V _{DDQ}
N	D20	D21	GND	V _{DDQ}	Q20	Q19
P	D22	D23	NC	GND	Q22	Q21
R	D24	D25	$\overline{\text{OE}}$	GND	Q24	Q23
T	D26	V _{CC}	GND	V _{DDQ}	Q26	Q25

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	LFBGA – GKE	Tape and reel	SN74SSTV32877GKER	SV877

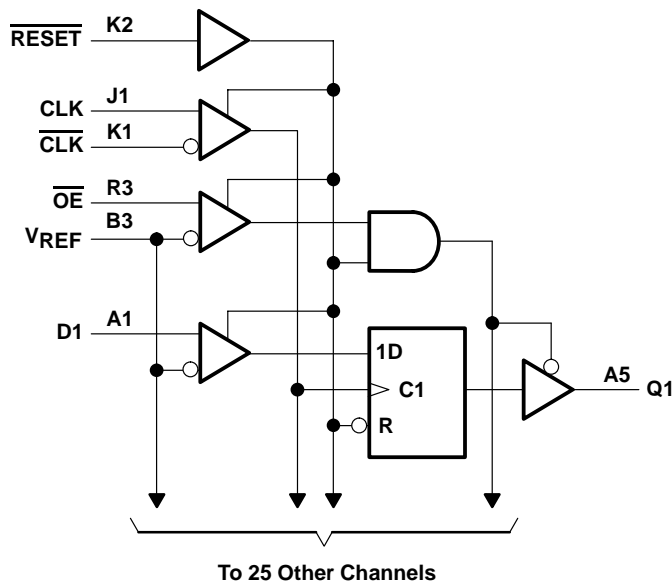
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS					OUTPUT
$\overline{\text{RESET}}$	$\overline{\text{OE}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	L	↑	↓	H	H
H	L	↑	↓	L	L
H	L	L or H	L or H	X	Q ₀
H	H	X	X	X	Z
L	X or floating	X or floating	X or floating	X or floating	L



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ}	-0.5 V to 3.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{DDQ} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	± 50 mA
Continuous current through each V_{CC} , V_{DDQ} , or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3)	40°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 3.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage	V _{DDQ}		2.7	V	
V _{DDQ}	Output supply voltage	2.3		2.7	V	
V _{REF}	Reference voltage (V _{REF} = V _{DDQ} /2)	1.15	1.25	1.35	V	
V _{TT}	Termination voltage	V _{REF} -40mV	V _{REF}	V _{REF} +40mV	V	
V _I	Input voltage	0		V _{CC}	V	
V _{IH}	AC high-level input voltage	OE, data inputs		V _{REF} +310mV	V	
V _{IL}	AC low-level input voltage	OE, data inputs		V _{REF} -310mV	V	
V _{IH}	DC high-level input voltage	OE, data inputs		V _{REF} +150mV	V	
V _{IL}	DC low-level input voltage	OE, data inputs		V _{REF} -150mV	V	
V _{IH}	High-level input voltage	RESET		1.7	V	
V _{IL}	Low-level input voltage	RESET		0.7	V	
V _{ICR}	Common-mode input voltage range	CLK, CLK		0.97	1.53	V
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK		360	mV	
I _{OH}	High-level output current				-20	mA
I _{OL}	Low-level output current				20	
T _A	Operating free-air temperature	0		70	°C	

NOTE 4: The RESET input of the device must be held at V_{CC} or GND to ensure proper device operation. The differential inputs must not be floating unless RESET is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT		
V _{IK}		I _I = -18 mA	2.3 V			-1.2	V		
V _{OH}		I _{OH} = -100 μA	2.3 V to 2.7 V	V _{CC} -0.2			V		
		I _{OH} = -16 mA	2.3 V	1.95					
V _{OL}		I _{OL} = 100 μA	2.3 V to 2.7 V			0.2	V		
		I _{OL} = 16 mA	2.3 V			0.35			
I _I	All inputs	V _I = V _{CC} or GND	2.7 V			±5	μA		
I _{CC}	Static standby	RESET = GND	2.7 V			40	μA		
	Static operating	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC)						I _O = 0	95
I _{CCD}	Dynamic operating – clock only	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle	2.5 V			44	μA/MHz		
	Dynamic operating – per each data input	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle						I _O = 0	5
I _{OZ}	Outputs	V _O = V _{CC} or GND, V _I (OE) = V _{CC}	2.7 V			±10	μA		
r _{OH}	Output high	I _{OH} = -20 mA	2.3 V to 2.7 V	7	20		Ω		
r _{OL}	Output low	I _{OL} = 20 mA	2.3 V to 2.7 V	7	20		Ω		
r _{O(Δ)}	r _{OH} - r _{OL}	I _O = 20 mA, T _A = 25°C	2.5 V			6	Ω		
C _i ‡	Data inputs and OE	V _I = V _{REF} ± 310 mV	2.5 V			2.5	3.3	4	pF
	CLK, CLK	V _{ICR} = 1.25 V, V _I (PP) = 360 mV				3	3.5	4	
	RESET	V _I = V _{CC} or GND				3	4	4.5	
C _o ‡	Outputs	V _O = 1.7 V or 0.8 V	2.5 V	6.5	7.6	9	pF		

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

‡ Measured with 50-MHz input frequency

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	MAX	
f _{clock}	Clock frequency		200		MHz
t _w	Pulse duration, CLK, $\overline{\text{CLK}}$ high or low		2.5		ns
t _{act}	Differential inputs active time (see Note 5)		22		ns
t _{inact}	Differential inputs inactive time (see Note 6)		22		ns
t _{su}	Setup time	Fast slew rate (see Notes 7 and 9)	Data before CLK \uparrow , $\overline{\text{CLK}}\downarrow$		ns
		Slow slew rate (see Notes 8 and 9)			
t _h	Hold time	Fast slew rate (see Notes 7 and 9)	Data after CLK \uparrow , $\overline{\text{CLK}}\downarrow$		ns
		Slow slew rate (see Notes 8 and 9)			

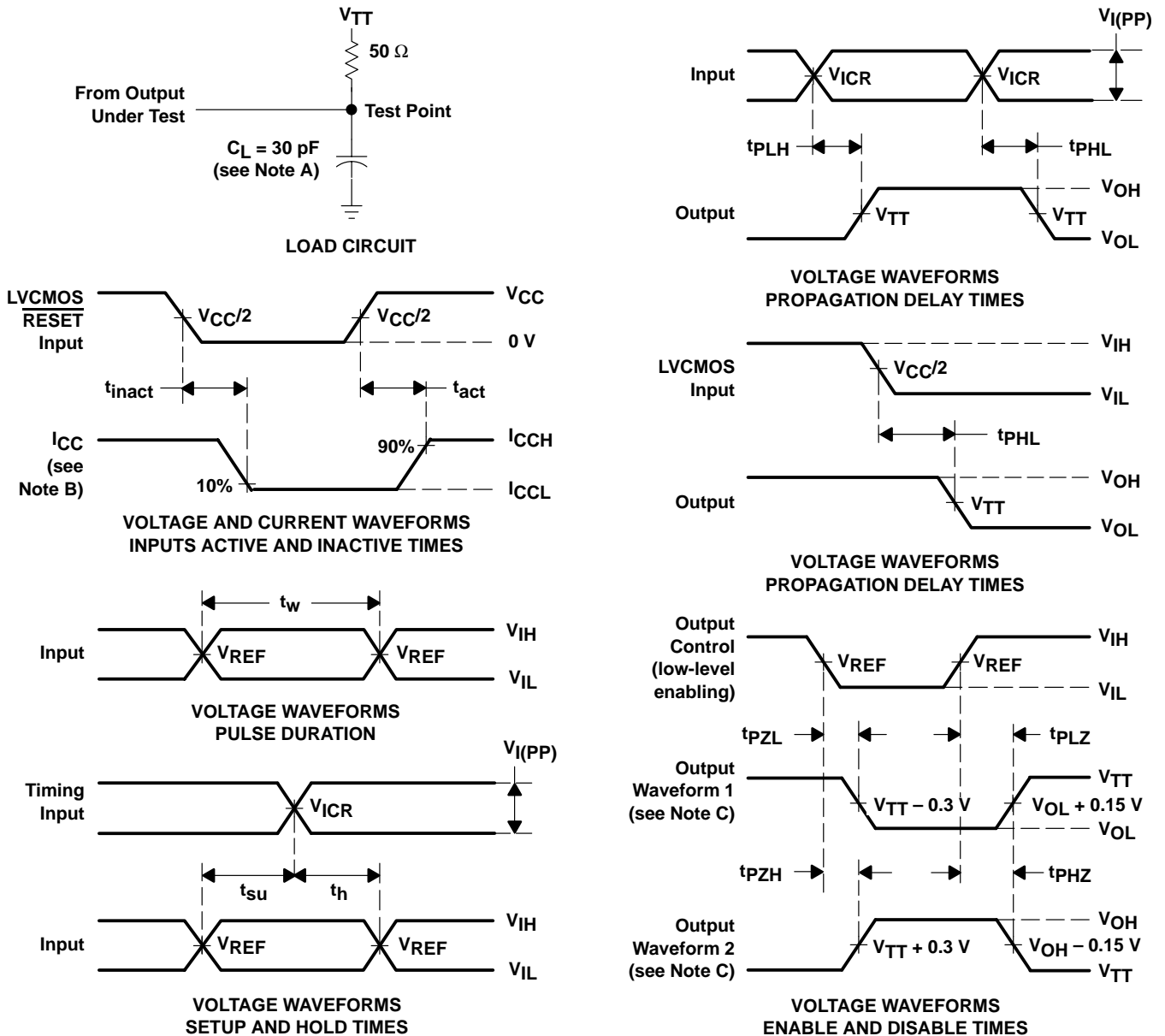
- NOTES: 5. Data inputs must be low a minimum time of t_{act} min, after $\overline{\text{RESET}}$ is taken high.
6. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} min, after $\overline{\text{RESET}}$ is taken low.
7. Data signal input slew rate ≥ 1 V/ns
8. Data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns
9. CLK, $\overline{\text{CLK}}$ input slew rates are ≥ 1 V/ns.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	MAX	
f _{max}			200		MHz
t _{pd}	CLK and $\overline{\text{CLK}}$	Q	1.1	2.8	ns
t _{PHL}	$\overline{\text{RESET}}$	Q	5		ns
t _{en}	$\overline{\text{OE}}$	Q	5		ns
t _{dis}	$\overline{\text{OE}}$	Q	6.3		ns



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and $I_O = 0$ mA.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, input slew rate = $1 V/ns \pm 20\%$ (unless otherwise noted).
 - E. The outputs are measured one at a time with one transition per measurement.
 - F. $V_{TT} = V_{REF} = V_{DDQ}/2$
 - G. $V_{IH} = V_{REF} + 310$ mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVC MOS input.
 - H. $V_{IL} = V_{REF} - 310$ mV (ac voltage levels) for differential inputs. $V_{IL} = GND$ for LVC MOS input.
 - I. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - J. t_{PZL} and t_{PZH} are the same as t_{en} .
 - K. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74SSTV32877GKER	OBSOLETE	LFBGA	GKE	96		TBD	Call TI	Call TI	0 to 70	SV877	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

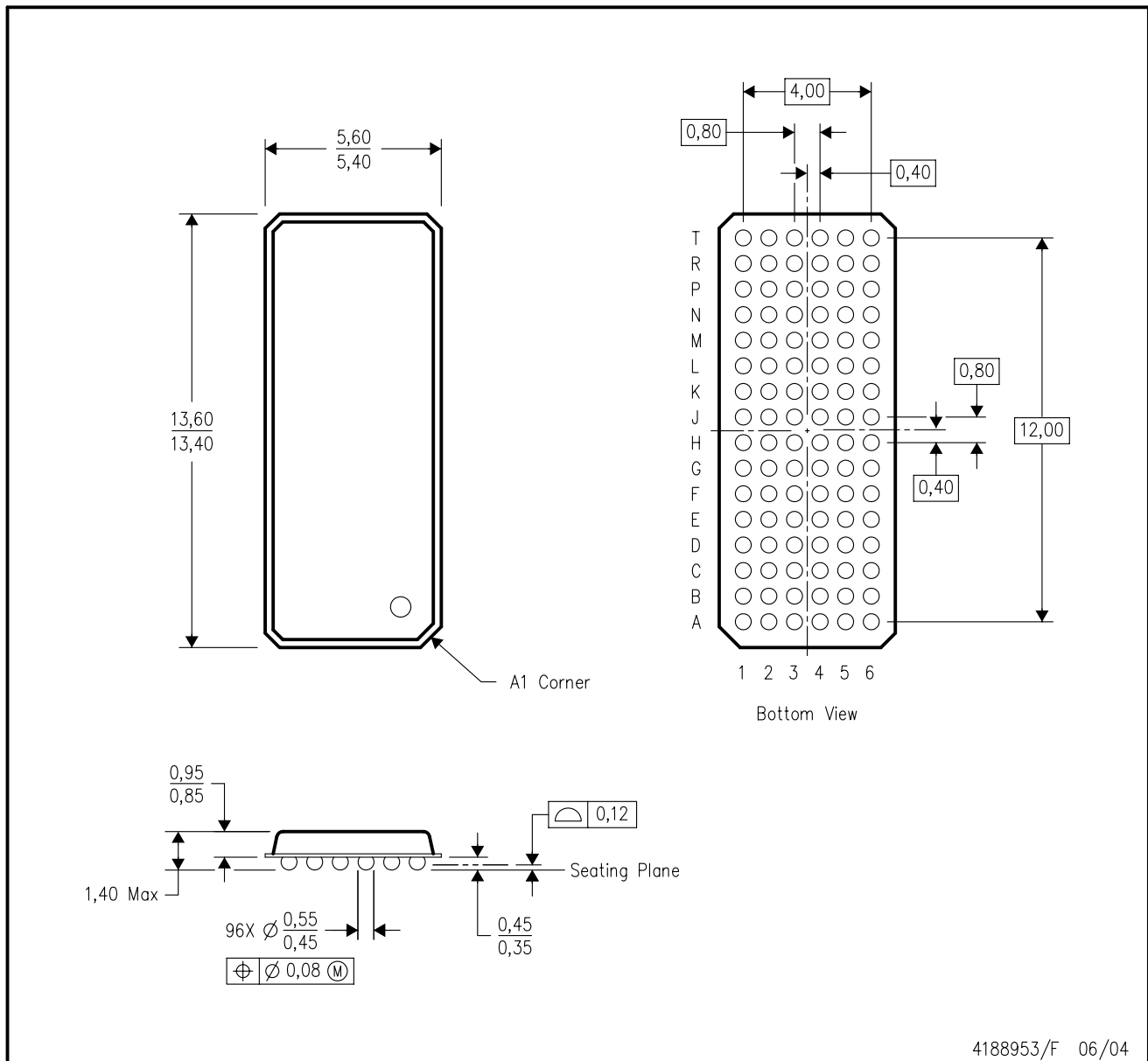
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

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