## Internal Registers (continued)

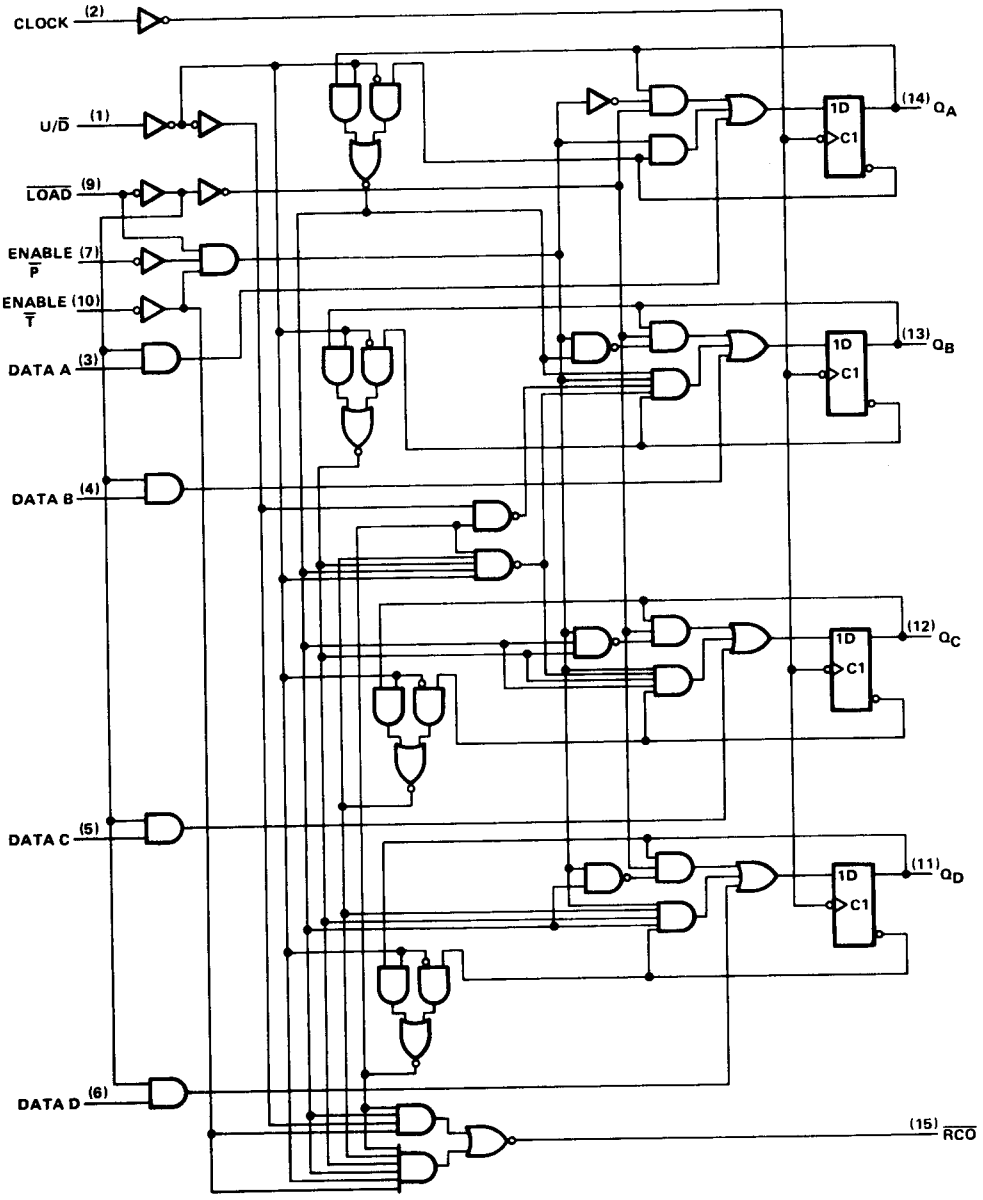
T-51-09-08

### *Revision Register (Revision B only)*

This 8-bit register is a read-only register, specifying the revision of the Bt459. The four most significant bits signify

**logic diagram (positive logic)**

SN54LS668, SN74LS668, DECADE COUNTERS




Pin numbers shown are for D, J, N, and W packages.





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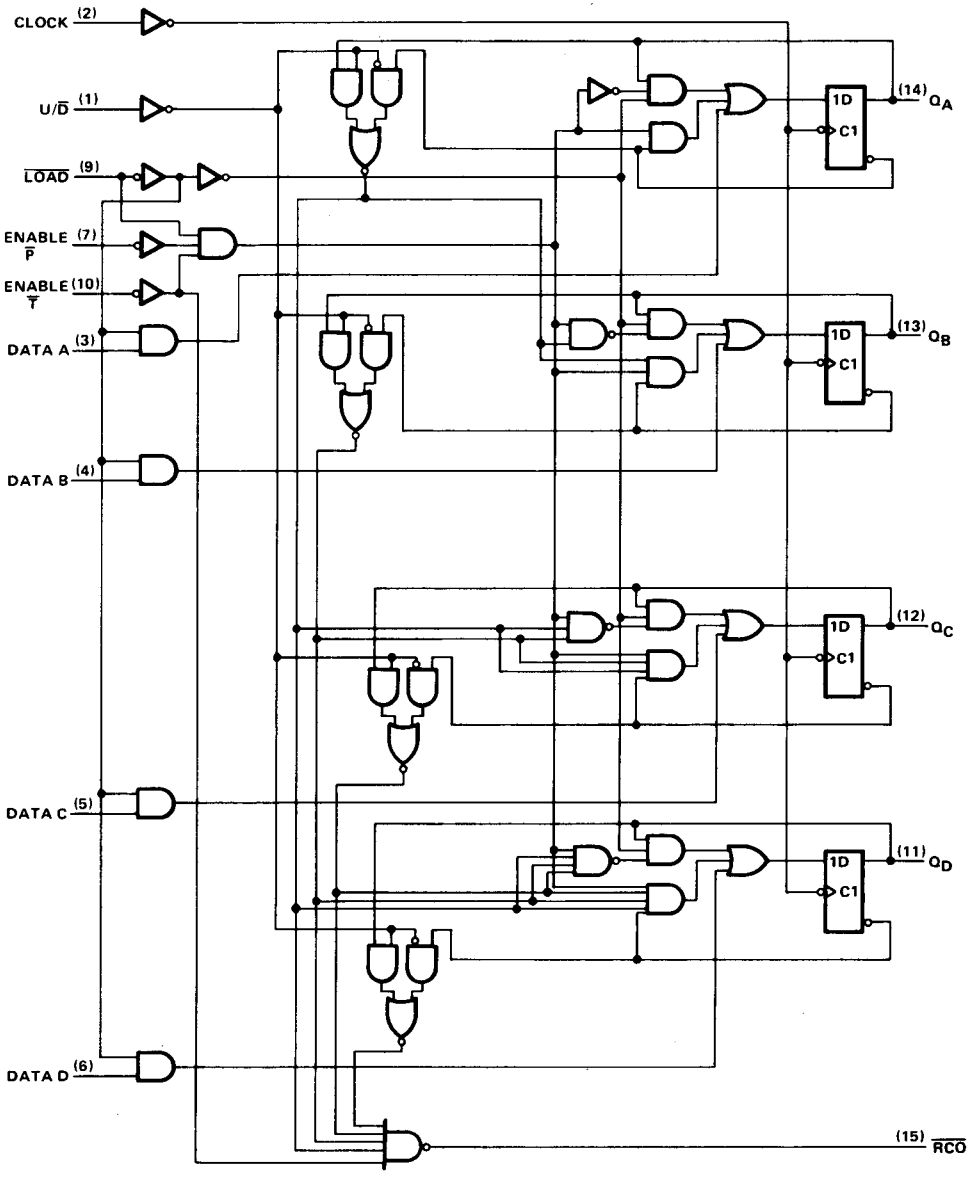
**logic diagram (positive logic) (continued)**

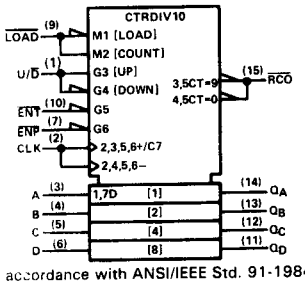
SN54LS669, SN74LS669, BINARY COUNTERS




Pin numbers shown are for D, J, N, and W packages.

## 'LS668 DECADE COUNTERS

### logic symbol†

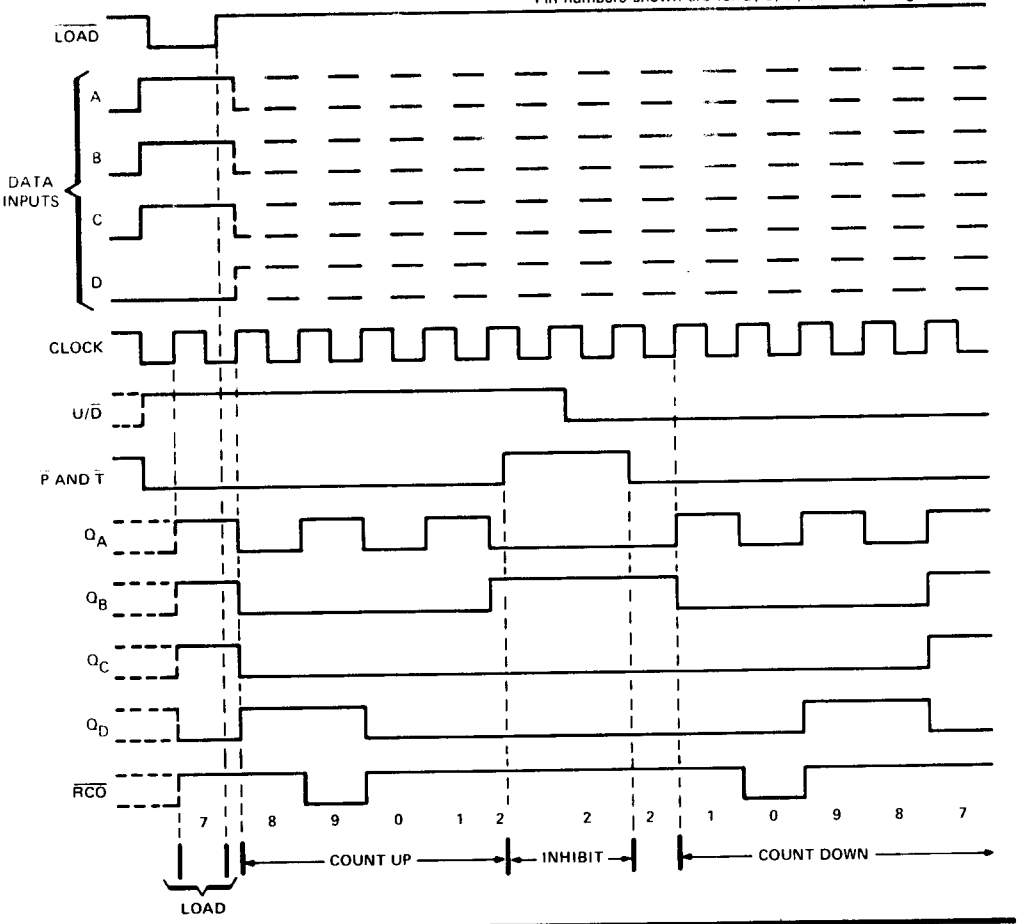



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

### typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven





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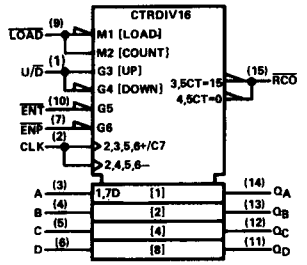
## 'LS669 BINARY COUNTERS

### logic symbol†

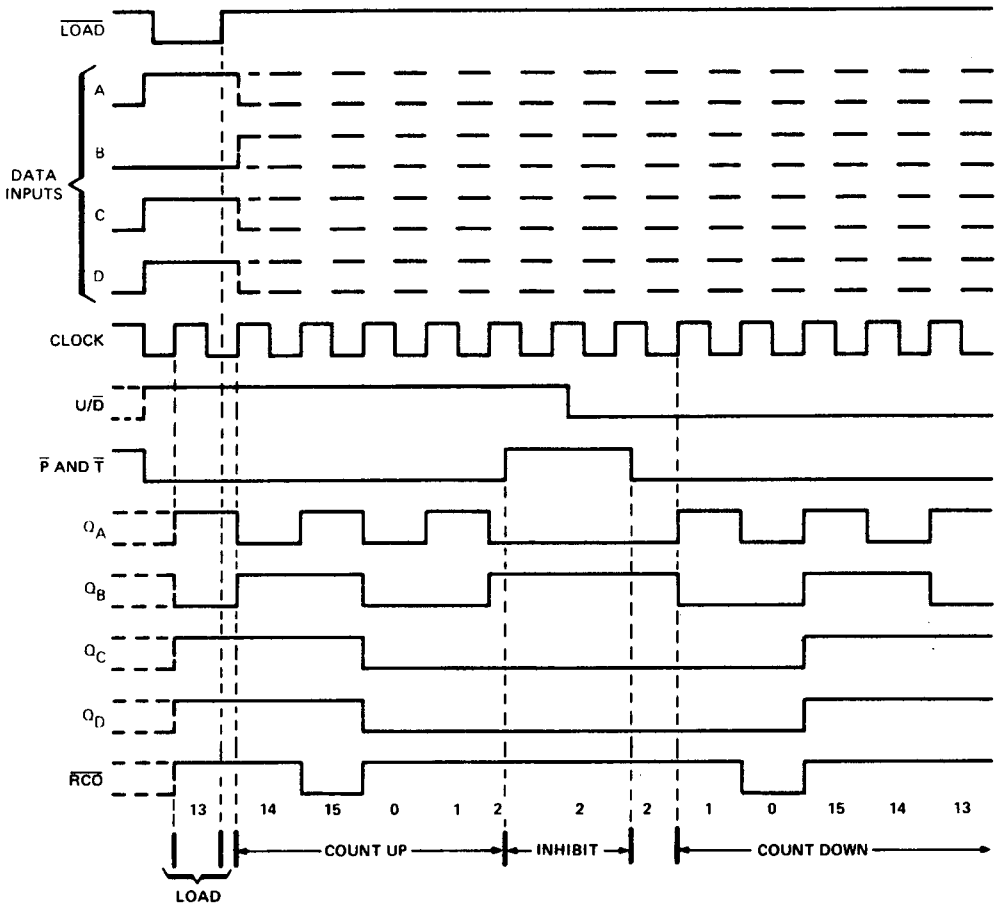



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

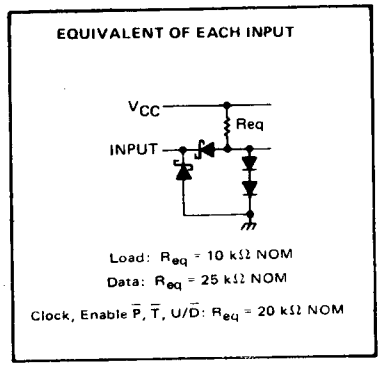
### typical load, count, and inhibit sequences

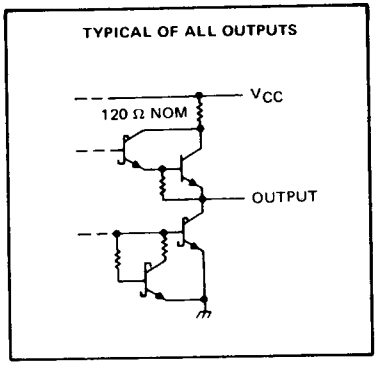
Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



## schematics of inputs and outputs






## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS668, SN54LS669 . . . . . −55°C to 125°C
SN74LS668, SN74LS669 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | SN54LS668 SN54LS669 | | | SN74LS668 SN74LS669 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | | 4 | | | 8 | mA |
| Clock frequency, $f_{clock}$ | | 0 | | 25 | 0 | | 25 | MHz |
| Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1) | | 20 | | | 20 | | | ns |
| Setup time, $t_{su}$ (see Figure 1) | Data inputs A, B, C, D | 25 | | | 25 | | | ns |
| | $\overline{ENP}$ or $\overline{ENT}$ | 40 | | | 40 | | | |
| | $\overline{LOAD}$ | 30 | | | 30 | | | |
| | U/$\overline{D}$ | 45 | | | 45 | | | |
| Hold time at any input with respect to clock, $t_h$ (see Figure 1) | | 0 | | | 0 | | | ns |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | 0 | | 70 | °C |



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | SN54LS668 SN54LS669 | | | SN74LS668 SN74LS669 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = −400 μA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| | | Clock, $\overline{T}$ | | | | | 0.1 | | | 0.1 | |
| | | $\overline{LOAD}$ | | | | | 0.2 | | | 0.2 | |
| $I_{IH}$ | High-level input current | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| | | Clock, $\overline{T}$ | | | | | 20 | | | 20 | |
| | | $\overline{LOAD}$ | | | | | 40 | | | 40 | |
| $I_{IL}$ | Low-level input current | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −0.4 | | | −0.4 | mA |
| | | Clock, $\overline{T}$ | | | | | −0.4 | | | −0.4 | |
| | | $\overline{LOAD}$ | | | | | −0.8 | | | −0.8 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, | See Note 2 | | 20 | 34 | | 20 | 34 | mA |

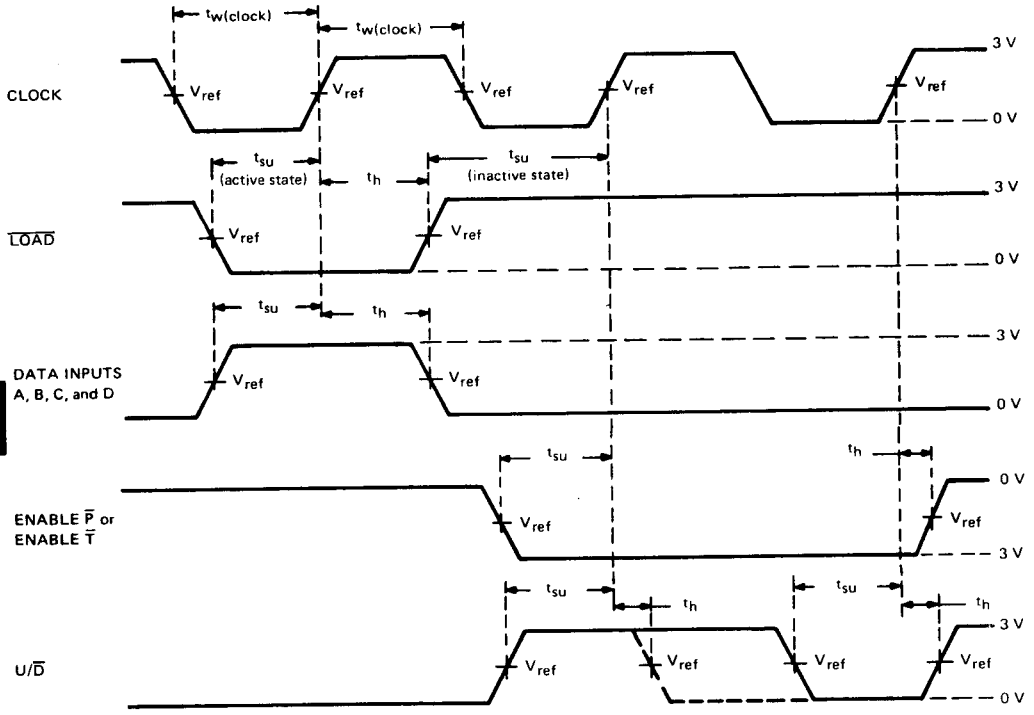
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Figures 2 and 3 | 25 | 32 | | MHz |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | | | 26 | 40 | ns |
| $t_{PHL}$ | | | | | 40 | 60 | |
| $t_{PLH}$ | CLK | Any Q | | | 18 | 27 | ns |
| $t_{PHL}$ | | | | | 18 | 27 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | | | 11 | 17 | ns |
| $t_{PHL}$ | | | | | 29 | 45 | |
| $t_{PLH}$# | U/$\overline{D}$ | $\overline{RCO}$ | | | 22 | 35 | ns |
| $t_{PHL}$# | | | | | 26 | 40 | |

¶ $f_{max}$ = Maximum clock frequency.
$t_{PLH}$ = propagation delay time, low-to-high-level output.
$t_{PHL}$ = propagation delay time, high-to-low-level output.
# Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.

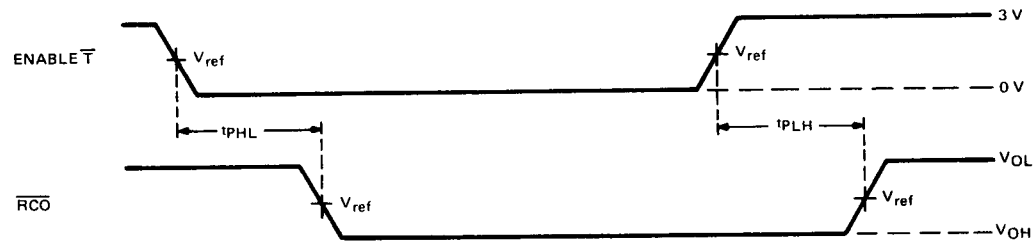
## PARAMETER MEASUREMENT INFORMATION




VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. $V_{ref} = 1.3$ V.

FIGURE 1–PULSE WIDTHS, SETUP TIMES, HOLD TIMES




VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. $t_{PLH}$ and $t_{PHL}$ from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count ($Q_A$ and $Q_D$ high for 'LS668, all Q outputs high for 'LS669).
C. $V_{ref} = 1.3$ V.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668, or 15 for 'LS669) the ripple carry output will be out of phase.

FIGURE 2–PROPAGATION DELAY TIMES TO CARRY OUTPUT





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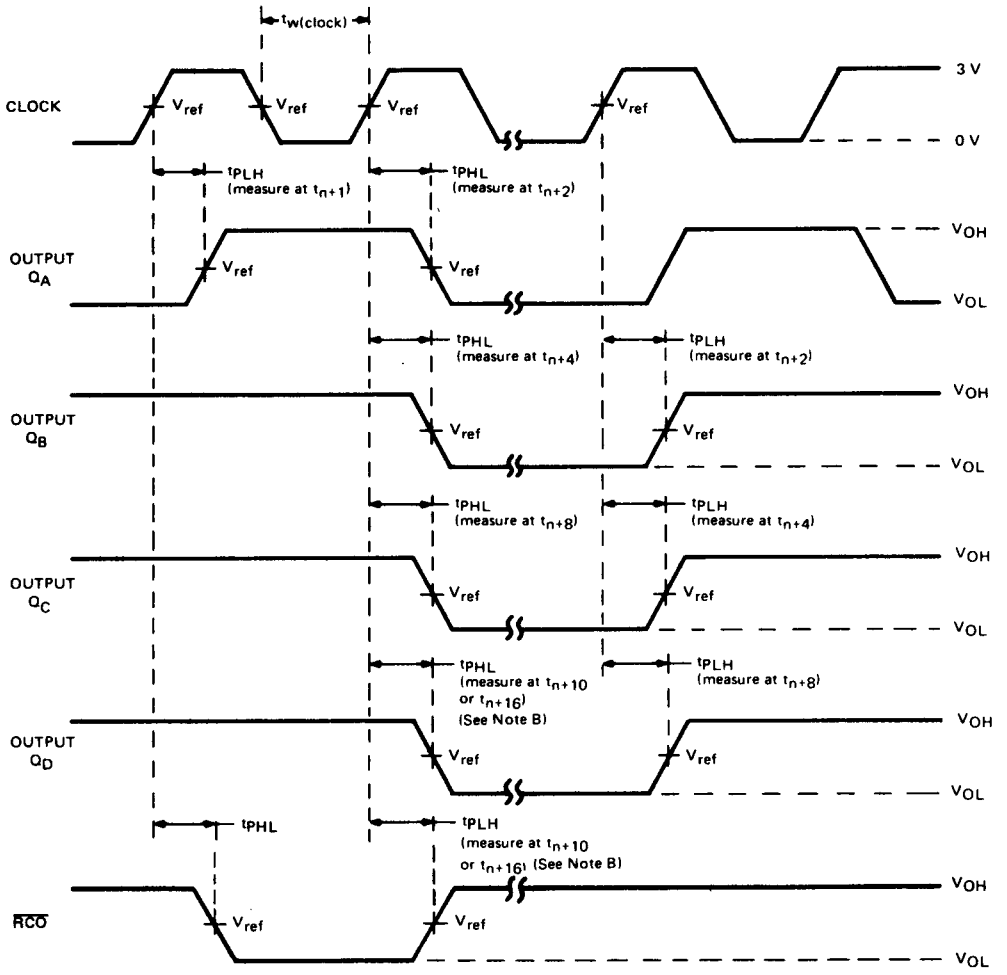
## PARAMETER MEASUREMENT INFORMATION




**UP-COUNT VOLTAGE WAVEFORMS**

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure $f_{max}$.
B. Outputs $Q_D$ and carry are tested at $t_{n+10}$ for the 'LS668, and at $t_{n+16}$ for the 'LS669, where $t_n$ is the bit-time when all outputs are low.
C. $V_{ref} = 1.3$ V.

**FIGURE 3–PROPAGATION DELAY TIMES FROM CLOCK**