FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{\text{ERC}}$) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DESCRIPTION/ORDERING INFORMATION

The SN74GTLPH3245 is a high-drive, 32-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as four 8-bit transceivers. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC circuitry, and TI-OPC circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH3245 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{\text{ERC}}$). Changing the $\overline{\text{ERC}}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry is provided to hold unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

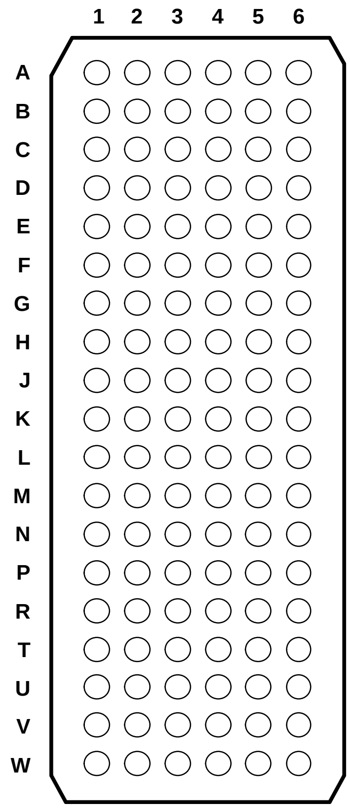
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{\text{OE}}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKF	Tape and reel	SN74GTLPH3245GKFR	GM45

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GKF PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS[(1)]

	1	2	3	4	5	6
A	1A3	1A2	1A1	1B1	1B2	1B3
B	GND	1A4	1DIR	$1\overline{OE}$	1B4	GND
C	1A6	1A5	GND	GND	1B5	1B6
D	1A8	1A7	$1V_{CC}$	$1V_{CC}$	1B7	1B8
E	$1\overline{ERC}$	GND	GND	GND	1BIAS V_{CC}	$1V_{REF}$
F	2A2	2A1	GND	GND	2B1	2B2
G	2A4	2A3	$1V_{CC}$	$1V_{CC}$	2B3	2B4
H	GND	2A5	GND	GND	2B5	GND
J	2A6	2A7	2A8	2B8	2B7	2B6
K	NC	3A1	2DIR	$2\overline{OE}$	3B1	NC
L	3A3	3A2	3DIR	$3\overline{OE}$	3B2	3B3
M	GND	3A4	GND	GND	3B4	GND
N	3A6	3A5	$2V_{CC}$	$2V_{CC}$	3B5	3B6
P	3A8	3A7	GND	GND	3B7	3B8
R	$2\overline{ERC}$	GND	GND	GND	2BIAS V_{CC}	$2V_{REF}$
T	4A2	4A1	$2V_{CC}$	$2V_{CC}$	4B1	4B2
U	4A4	4A3	GND	GND	4B3	4B4
V	GND	4A5	4A8	4B8	4B5	GND
W	4A6	4A7	4DIR	$4\overline{OE}$	4B7	4B6

(1) NC – No internal connection

FUNCTIONAL DESCRIPTION

The SN74GTLPH3245 is a high-drive (100-mA), 32-bit bus transceiver partitioned in four 8-bit segments and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. $\overline{OE}$ can be used to disable the device so the buses effectively are isolated. Data polarity is noninverting.

For A-to-B data flow, when $\overline{OE}$ is low and DIR is high, the B outputs take on the logic value of the A inputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except $\overline{OE}$ and DIR are low.

FUNCTION TABLES

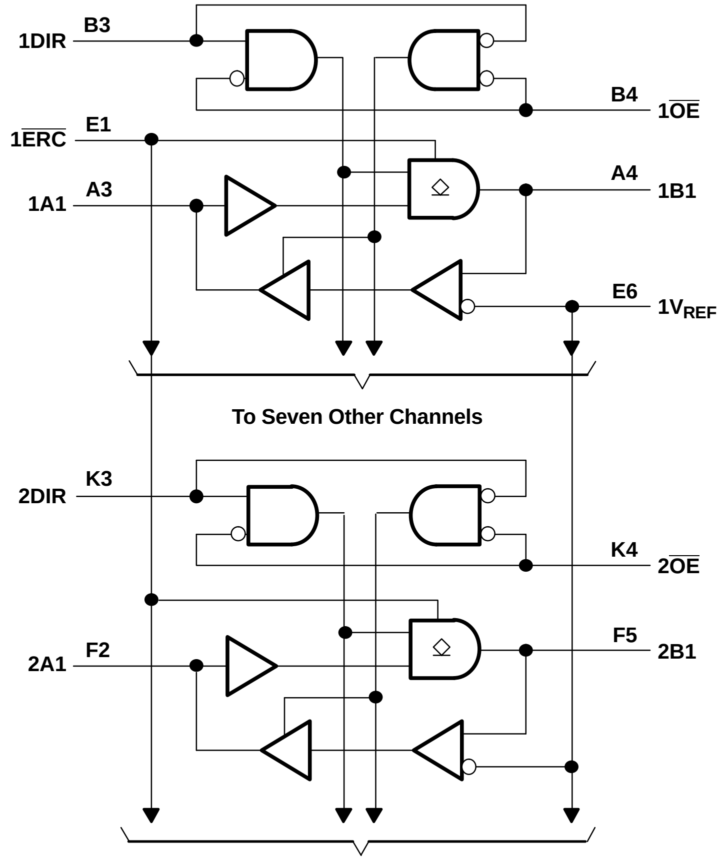
OUTPUT CONTROL

INPUTS		OUTPUT	MODE
$\overline{OE}$	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

B-PORT EDGE-RATE CONTROL ($\overline{ERC}$)

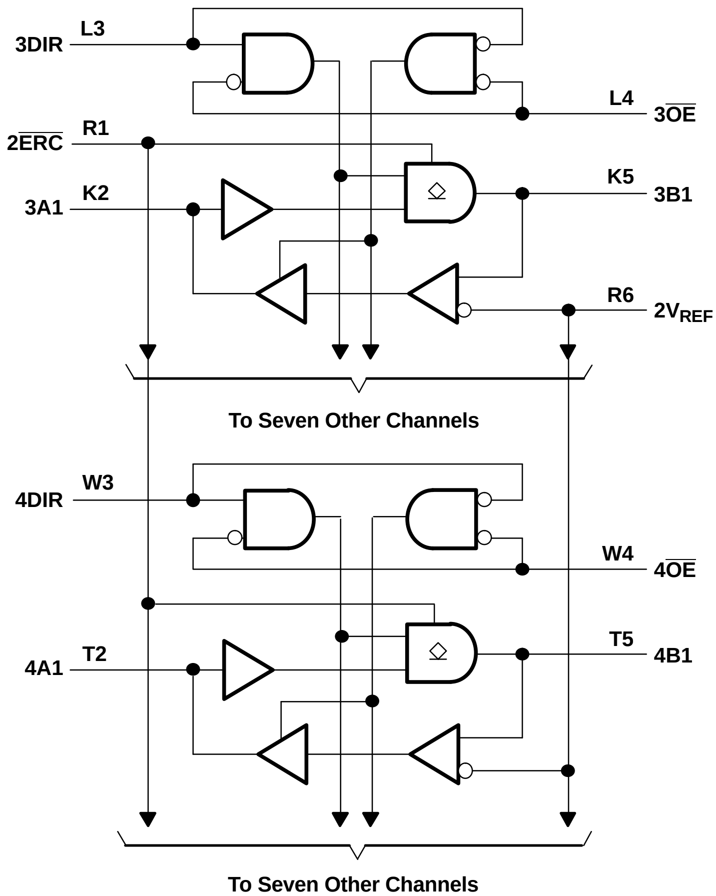
INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

LOGIC DIAGRAM (POSITIVE LOGIC)(1)



(1) $1V_{CC}$ and 1BIAS V_{CC} are associated with these channels.

LOGIC DIAGRAM (POSITIVE LOGIC) (CONTINUED)(1)



(1) $2V_{CC}$ and 2BIAS V_{CC} are associated with these channels.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range[2]	A-port, $\overline{ERC}$, and control inputs	–0.5	7	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	7	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		48	mA
		B port		200	
I_O	Current into any A-port output in the high state[3]			48	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance[4]			36	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[(1)(2)(3)(4)]

			MIN	NOM	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 0.05			V
		$\overline{ERC}$	V_{CC} – 0.6	V_{CC}	5.5	
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF} – 0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

<table>
<tr><th colspan="2">PARAMETER</th><th colspan="2">TEST CONDITIONS</th><th>MIN</th><th>TYP(1)</th><th>MAX</th><th>UNIT</th></tr>
<tr><td colspan="2">V_{IK}</td><td>V_{CC} = 3.15 V,</td><td>I_I = –18 mA</td><td></td><td></td><td>–1.2</td><td>V</td></tr>
<tr><td rowspan="3">V_{OH}</td><td rowspan="3">A port</td><td>V_{CC} = 3.15 V to 3.45 V,</td><td>I_{OH} = –100 µA</td><td>V_{CC} – 0.2</td><td></td><td></td><td rowspan="3">V</td></tr>
<tr><td rowspan="2">V_{CC} = 3.15 V</td><td>I_{OH} = –12 mA</td><td>2.4</td><td></td><td></td></tr>
<tr><td>I_{OH} = –24 mA</td><td>2</td><td></td><td></td></tr>
<tr><td rowspan="6">V_{OL}</td><td rowspan="3">A port</td><td>V_{CC} = 3.15 V to 3.45 V,</td><td>I_{OL} = 100 µA</td><td></td><td></td><td>0.2</td><td rowspan="6">V</td></tr>
<tr><td rowspan="2">V_{CC} = 3.15 V</td><td>I_{OL} = 12 mA</td><td></td><td></td><td>0.4</td></tr>
<tr><td>I_{OL} = 24 mA</td><td></td><td></td><td>0.5</td></tr>
<tr><td rowspan="3">B port</td><td rowspan="3">V_{CC} = 3.15 V</td><td>I_{OL} = 10 mA</td><td></td><td></td><td>0.2</td></tr>
<tr><td>I_{OL} = 64 mA</td><td></td><td></td><td>0.4</td></tr>
<tr><td>I_{OL} = 100 mA</td><td></td><td></td><td>0.55</td></tr>
<tr><td rowspan="3">I_I(2)</td><td rowspan="2">A-port and control inputs</td><td rowspan="3">V_{CC} = 3.45 V</td><td>V_I = 0 or V_{CC}</td><td></td><td></td><td>±10</td><td rowspan="3">µA</td></tr>
<tr><td>V_I = 5.5 V</td><td></td><td></td><td>±20</td></tr>
<tr><td>B port</td><td>V_I = 0 to 1.5 V</td><td></td><td></td><td>±10</td></tr>
<tr><td>I_{BHL}(3)</td><td>A port</td><td>V_{CC} = 3.15 V,</td><td>V_I = 0.8 V</td><td>75</td><td></td><td></td><td>µA</td></tr>
<tr><td>I_{BHH}(4)</td><td>A port</td><td>V_{CC} = 3.15 V,</td><td>V_I = 2 V</td><td>–75</td><td></td><td></td><td>µA</td></tr>
<tr><td>I_{BHLO}(5)</td><td>A port</td><td>V_{CC} = 3.45 V,</td><td>V_I = 0 to V_{CC}</td><td>500</td><td></td><td></td><td>µA</td></tr>
<tr><td>I_{BHHO}(6)</td><td>A port</td><td>V_{CC} = 3.45 V,</td><td>V_I = 0 to V_{CC}</td><td>–500</td><td></td><td></td><td>µA</td></tr>
<tr><td rowspan="3">I_{CC}</td><td rowspan="3">A or B port</td><td rowspan="3">V_{CC} = 3.45 V, I_O = 0,
V_I (A-port or control input) = V_{CC} or GND,
V_I (B port) = V_{TT} or GND</td><td>Outputs high</td><td></td><td></td><td>80</td><td rowspan="3">mA</td></tr>
<tr><td>Outputs low</td><td></td><td></td><td>80</td></tr>
<tr><td>Outputs disabled</td><td></td><td></td><td>80</td></tr>
<tr><td colspan="2">ΔI_{CC}(7)</td><td colspan="2">V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V,
Other A-port or control inputs at V_{CC} or GND</td><td></td><td></td><td>1.5</td><td>mA</td></tr>
<tr><td>C_i</td><td>Control inputs</td><td colspan="2">V_I = 3.15 V or 0</td><td></td><td>4</td><td>5</td><td>pF</td></tr>
<tr><td rowspan="2">C_{io}</td><td>A port</td><td colspan="2">V_O = 3.15 V or 0</td><td></td><td>6.5</td><td>7.5</td><td rowspan="2">pF</td></tr>
<tr><td>B port</td><td colspan="2">V_O = 1.5 V or 0</td><td></td><td>9.5</td><td>11</td></tr>
</table>

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) For I/O ports, the parameter I_I includes the off-state output leakage current.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
(7) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

<table>
<tr><th>PARAMETER</th><th colspan="3">TEST CONDITIONS</th><th>MIN</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>I_{off}</td><td>V_{CC} = 0,</td><td>BIAS V_{CC} = 0,</td><td>V_I or V_O = 0 to 5.5 V</td><td></td><td>10</td><td>µA</td></tr>
<tr><td>I_{OZPU}</td><td>V_{CC} = 0 to 1.5 V,</td><td>V_O = 0.5 V to 3 V,</td><td>$\overline{OE}$ = 0</td><td></td><td>±30</td><td>µA</td></tr>
<tr><td>I_{OZPD}</td><td>V_{CC} = 1.5 V to 0,</td><td>V_O = 0.5 V to 3 V,</td><td>$\overline{OE}$ = 0</td><td></td><td>±30</td><td>µA</td></tr>
</table>

Live-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

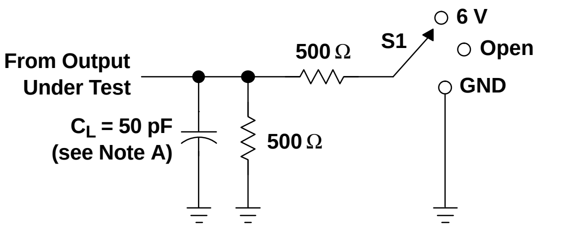
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	MIN	TYP(2)	MAX	UNIT
t_{PLH}	A	B	Slow	3.9		7.2	ns
t_{PHL}				3.1		8.4	
t_{PLH}	A	B	Fast	2.6		5.7	ns
t_{PHL}				2.1		5.8	
t_{en}	$\overline{OE}$	B	Slow	4.1		7.3	ns
t_{dis}				4		9.4	
t_{en}	$\overline{OE}$	B	Fast	2.9		5.9	ns
t_{dis}				4		6.9	
t_r	Rise time, B outputs (20% to 80%)		Slow		3		ns
			Fast		1.5		
t_f	Fall time, B outputs (80% to 20%)		Slow		4		ns
			Fast		2.5		
t_{PLH}	B	A		0.5		6.7	ns
t_{PHL}				1.2		4.5	
t_{en}	$\overline{OE}$	A		1.1		6.3	ns
t_{dis}				1.7		5.1	

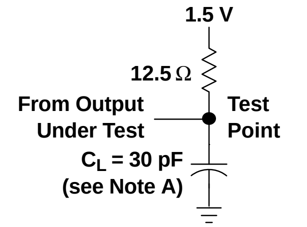
(1) Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

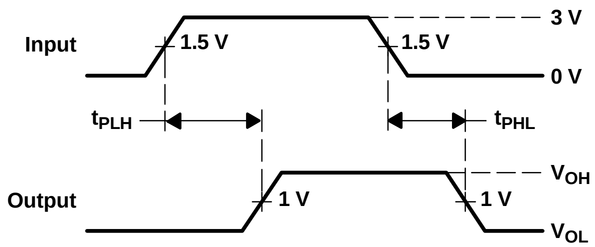


LOAD CIRCUIT FOR A OUTPUTS

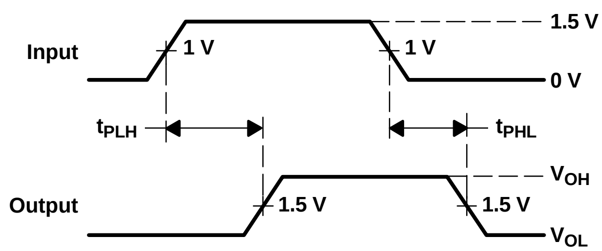
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



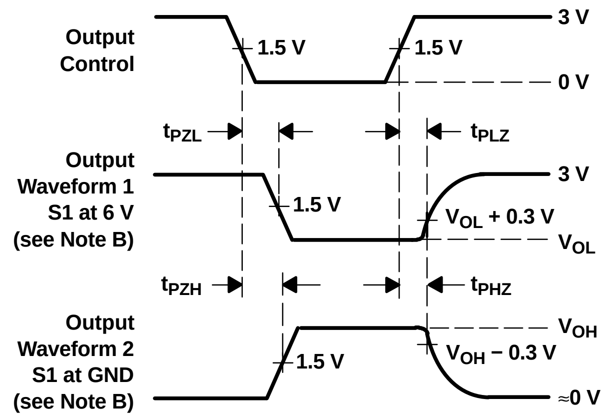
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

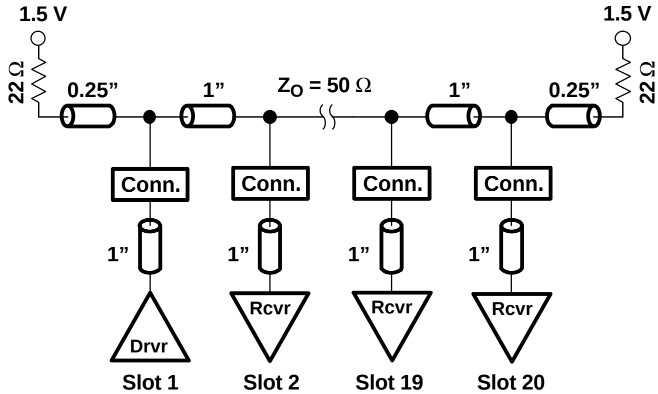


Figure 2. High-Drive Test Backplane

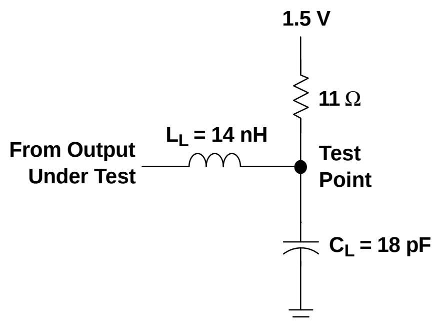


Figure 3. High-Drive RLC Network

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	TYP(2)	UNIT
t_{PLH}	A	B	Slow	4.9	ns
t_{PHL}				4.9	
t_{PLH}	A	B	Fast	3.7	ns
t_{PHL}				3.7	
t_{en}	$\overline{OE}$	B	Slow	5.1	ns
t_{dis}				5.4	
t_{en}	$\overline{OE}$	B	Fast	4.1	ns
t_{dis}				4.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

(1) Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74GTLPH3245GKFR	NRND	BGA MICROSTAR	GKF	114		TBD	Call TI	Call TI	-40 to 85	GM45	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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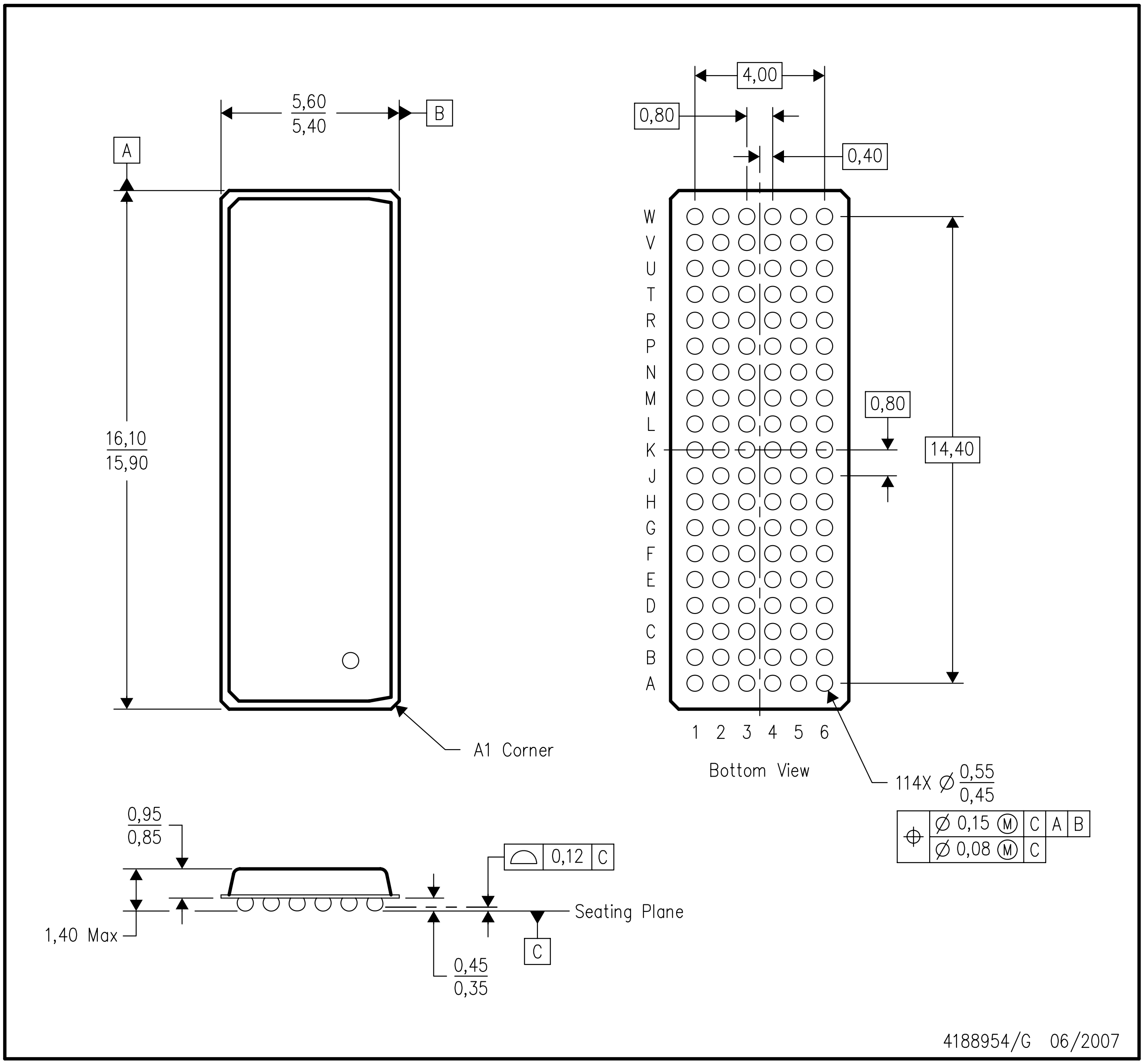
GKF (R–PBGA–N114) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation DC.
D. This package is tin–lead (SnPb). Refer to the 114 ZKF package (drawing 4204494) for lead–free.

IMPORTANT NOTICE

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