- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **2048 Words by 9 Bits**
- **Low-Power Advanced CMOS Technology**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 12 ns With a 50-pF Load**
- **Data Rates up to 67 MHz**
- **3-State Outputs**
- **Package Options Include 44-Pin Plastic Leaded Chip Carrier (FN) and 64-Pin Thin Quad Flat (PAG, PM) Packages**

description

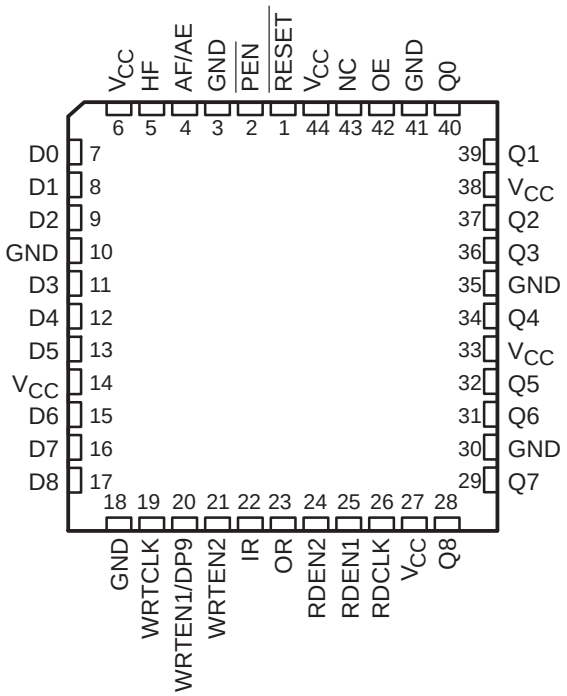
The SN74ACT7807 is a 2048-word by 9-bit FIFO with high speed and fast access times. It processes data at rates up to 67 MHz and access times of 12 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The write-clock (WRTCLK) and read-clock (RDCLK) inputs should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when the write-enable (WRTEN1/DP9, WRTEN2) inputs are high and the input-ready (IR) flag output is high. Data is read from memory on the rising edge of RDCLK when the read-enable (RDEN1, RDEN2) and output-enable (OE) inputs are high and the output-ready (OR) flag output is high. The first word written to memory is clocked through to the output buffer regardless of the levels on RDEN1, RDEN2, and OE. The OR flag indicates that valid data is present on the output buffer.

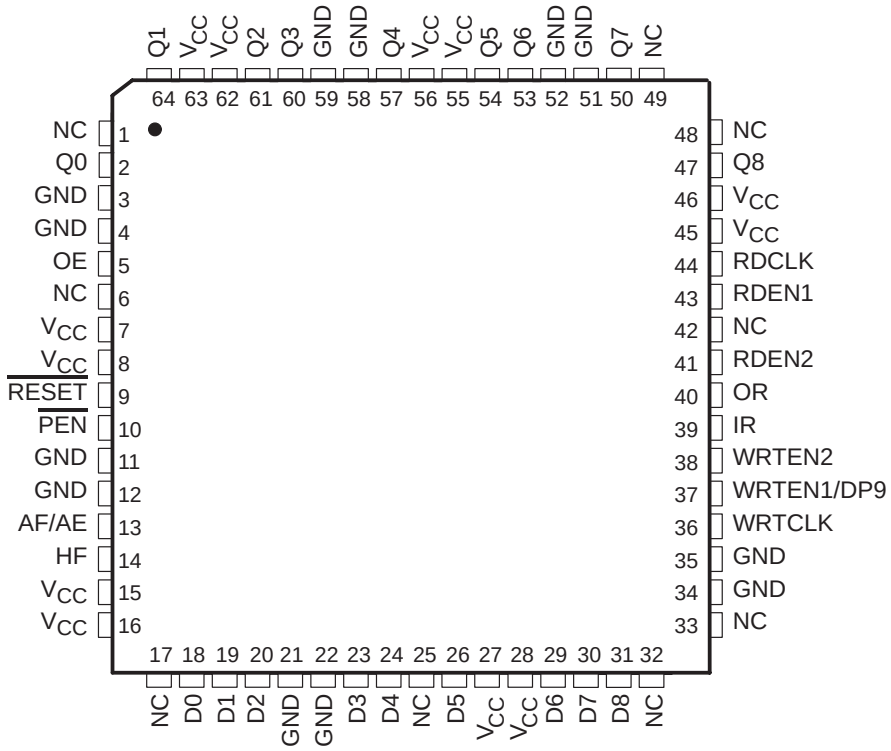
The FIFO can be reset asynchronous to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK cycles occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and half-full (HF) flags low and the almost-full/almost-empty (AF/AE) flag high. The FIFO must be reset upon power up.

The SN74ACT7807 is characterized for operation from 0°C to 70°C.

FN PACKAGE
(TOP VIEW)

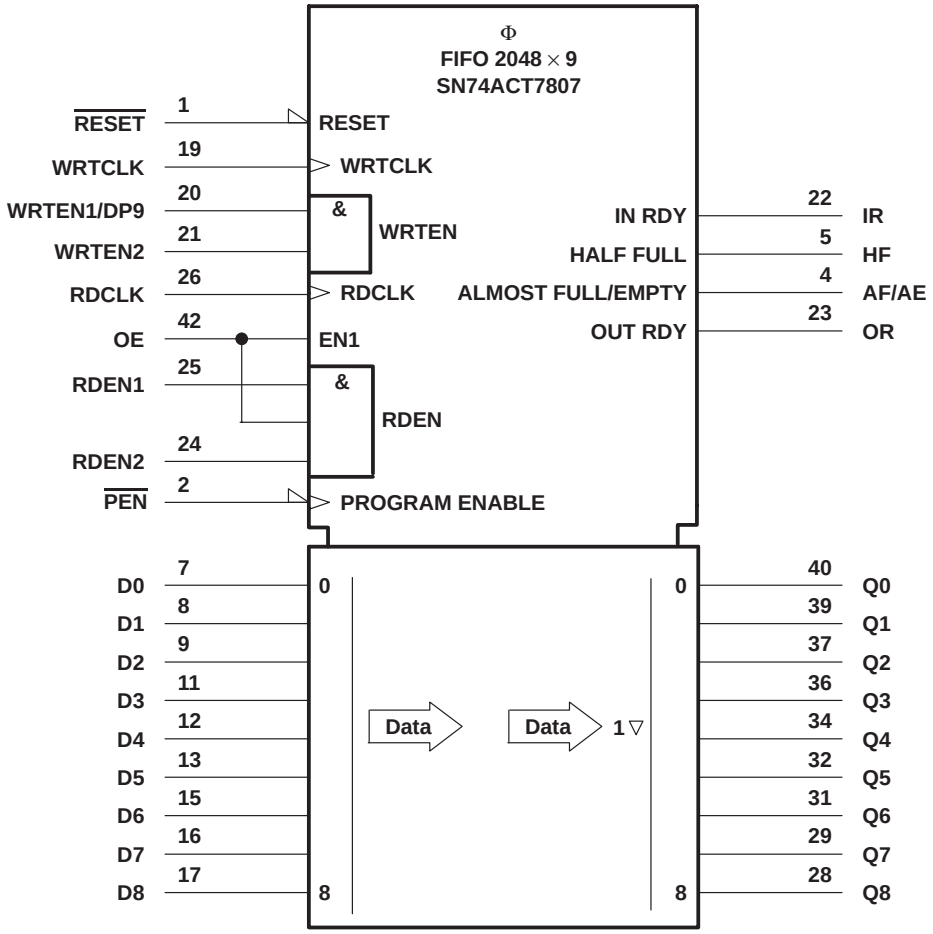


PAG OR PM PACKAGE
(TOP VIEW)



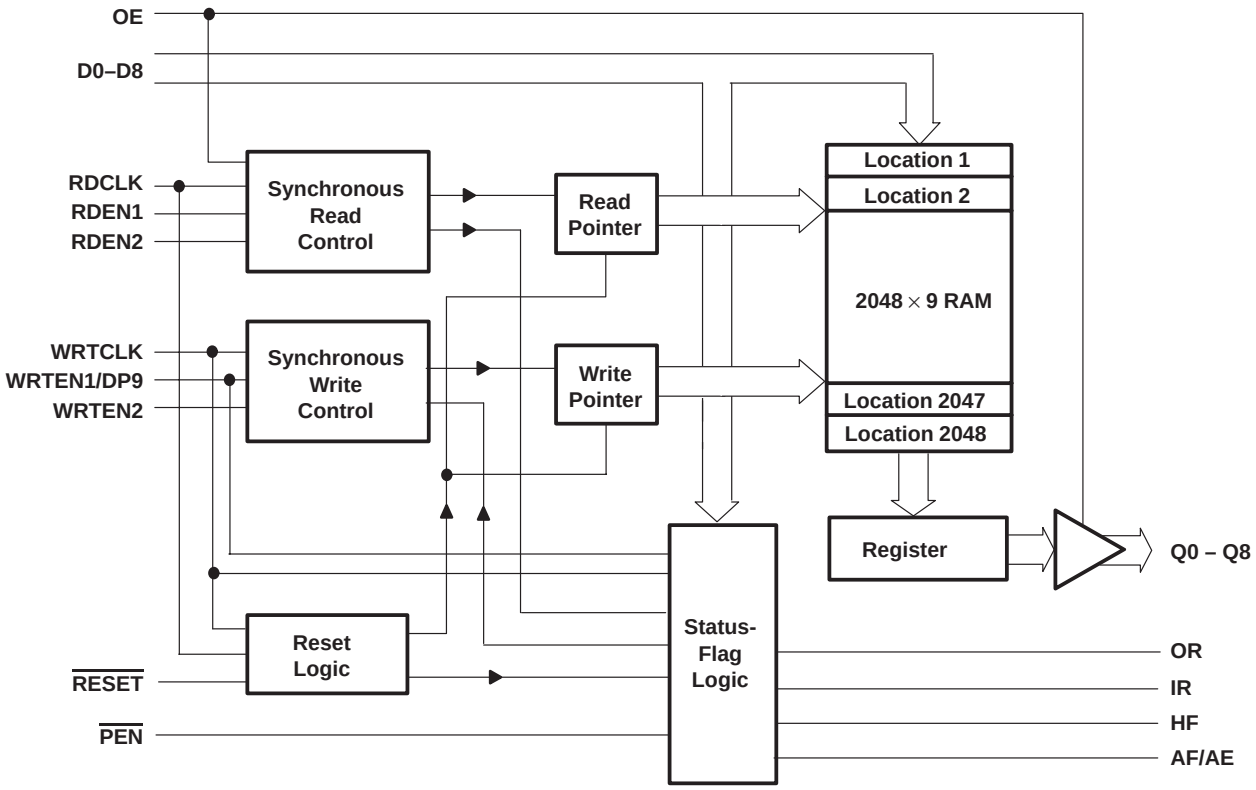
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
AF/AE	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE or the default value of 256 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or fewer words or (2048 – Y) or more words. AF/AE is high after reset.
D0–D8	I	Nine-bit data input port
HF	O	Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
OE	I	Output enable. When OE, RDEN1, RDEN2 and OR are high, data is read from the FIFO on a low-to-high transition of RDCLK. When OE is low, reads are disabled and the data outputs are in the high-impedance state.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\text{PEN}}$	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q8	O	Nine-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q8 on the third rising edge of RDCLK. OR also is asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q8.
RDCLK	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when RDEN1, RDEN2, OE, and OR are high. OR is synchronous to the low-to-high transition of RDCLK.
RDEN1 RDEN2	I	Read enables. When RDEN1, RDEN2, OE, and OR are high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\text{RESET}}$	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when WRTEN1/DP9, WRTEN2, and IR are high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1/DP9	I	Write enable/data pin 9. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. When programming an AF/AE offset value, WRTEN1/DP9 is used as the most-significant data bit.
WRTEN2	I	Write enable. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

offset values for AF/AE

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or fewer words or (2048 – Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D8 and WRTEN1/DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D8 and WRTEN1/DP9 at the time of the second WRTCLK low-to-high transition. While the offsets are programmed, data is not written to the FIFO memory, regardless of the state of the write enables (WRTEN1/DP9, WRTEN2). A maximum value of 1023 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 256, $\overline{PEN}$ must be held high.

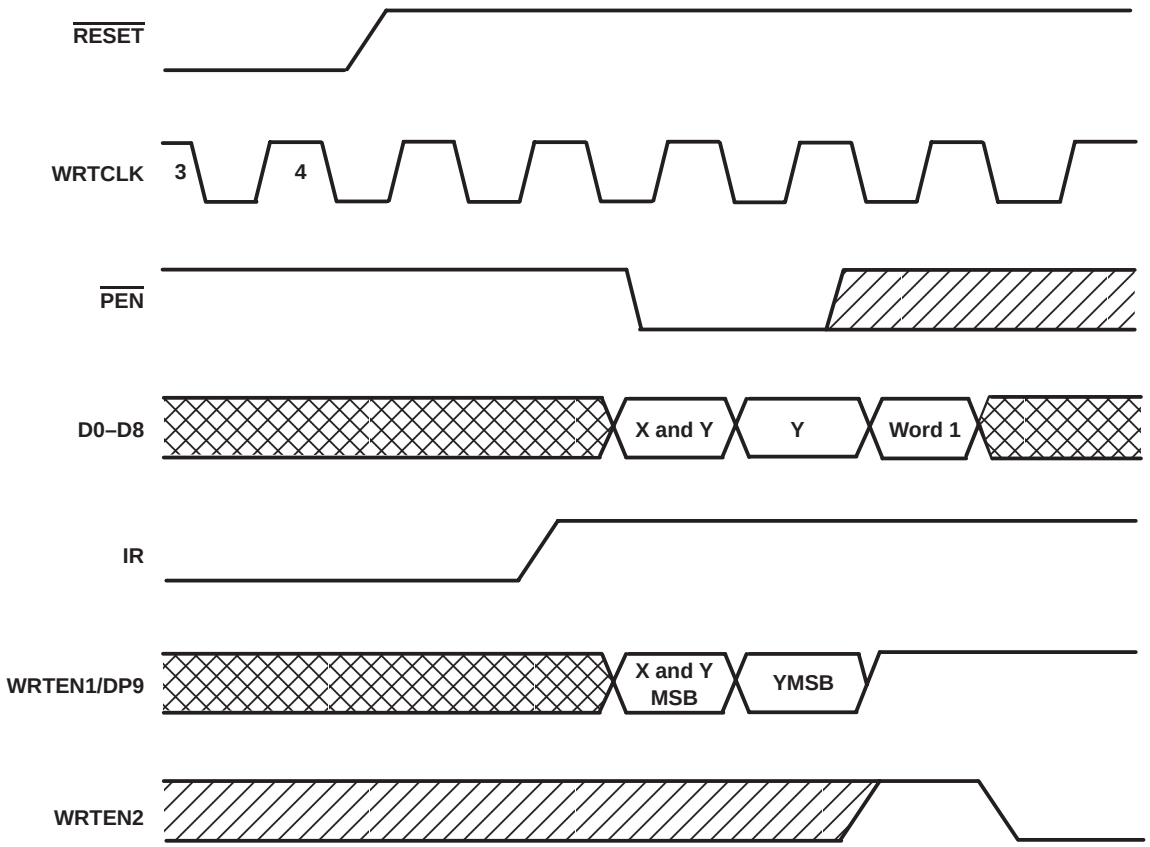


Figure 1. Programming X and Y Separately

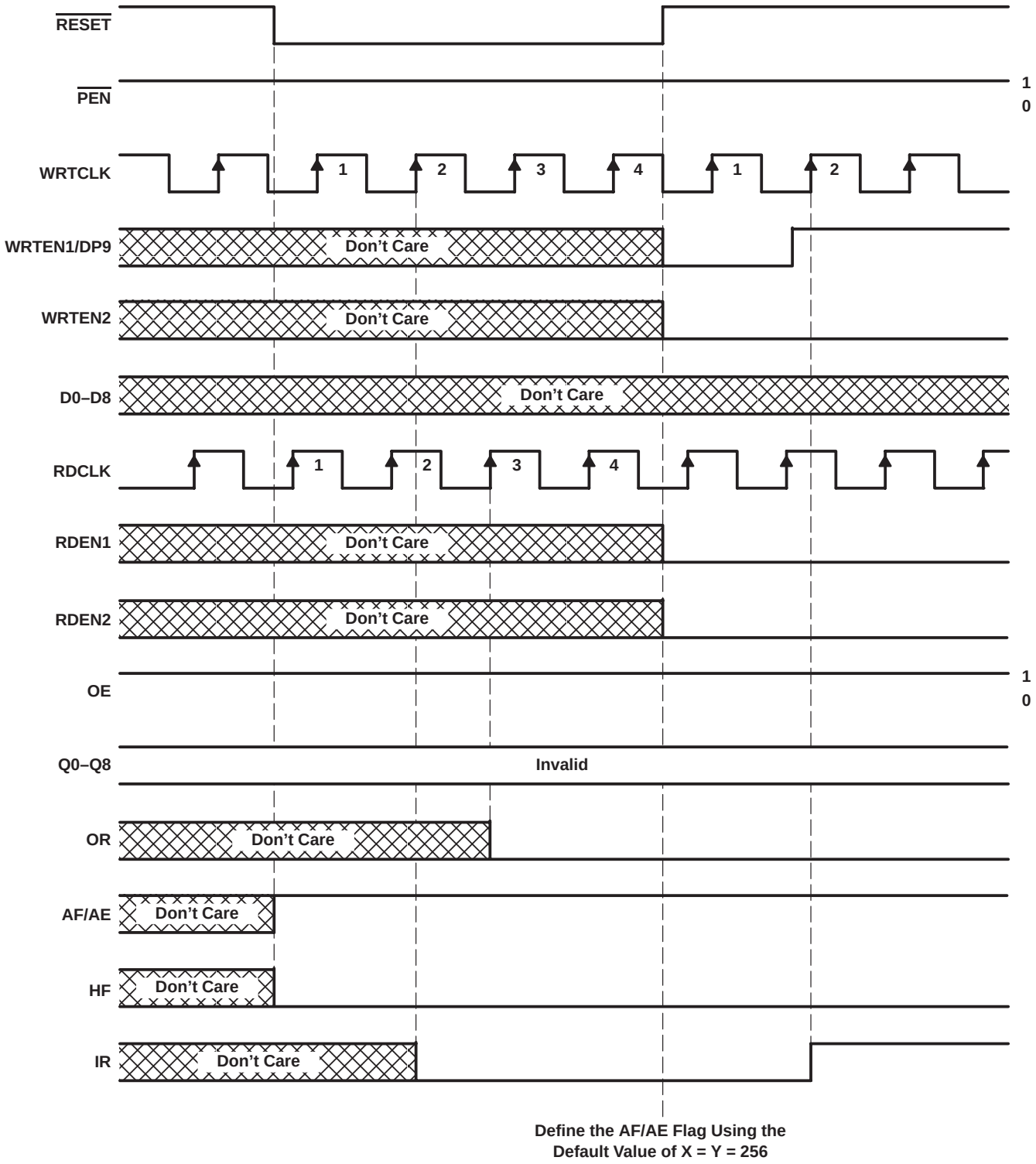


Figure 2. Reset Cycle

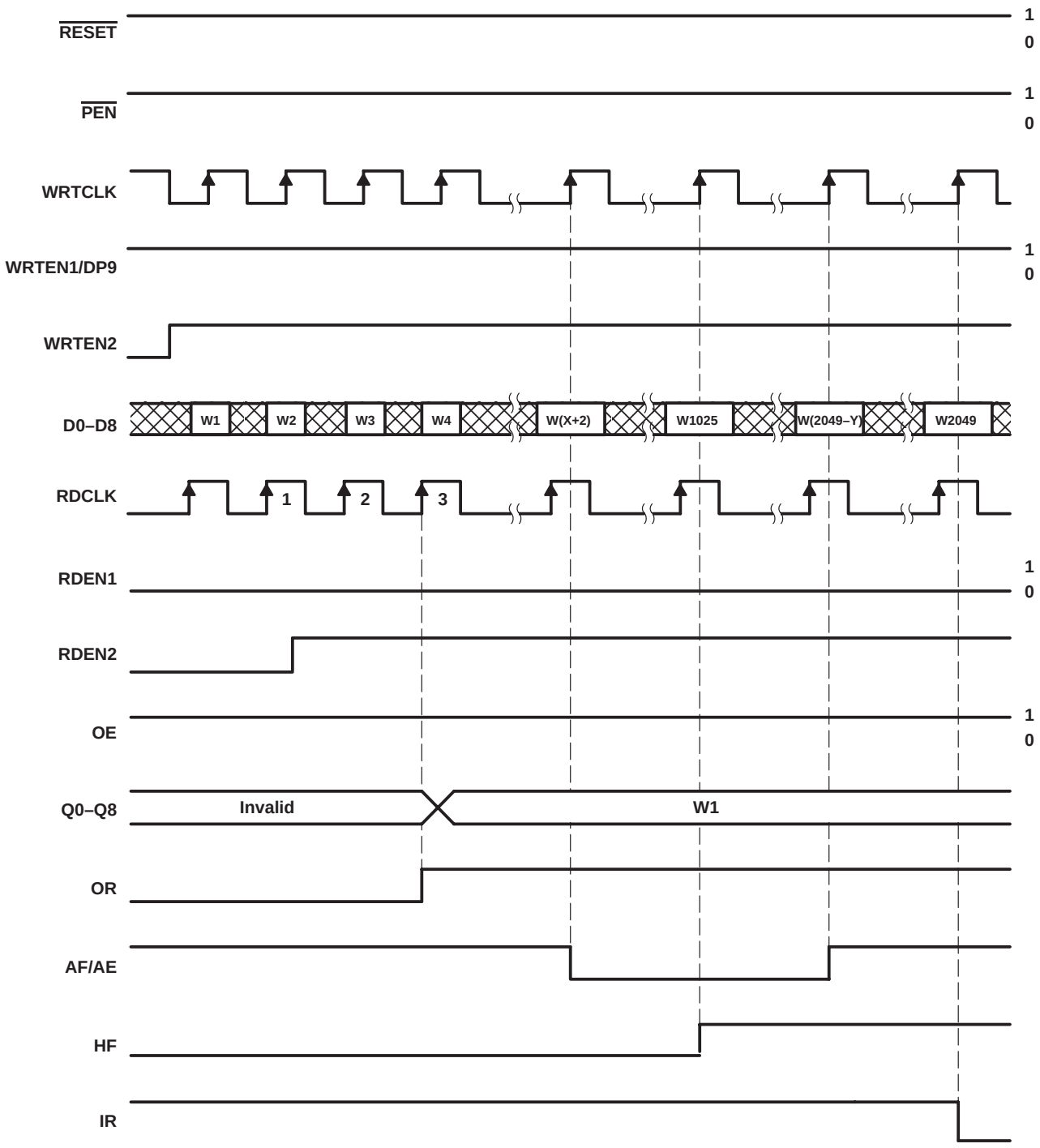


Figure 3. Write Cycle

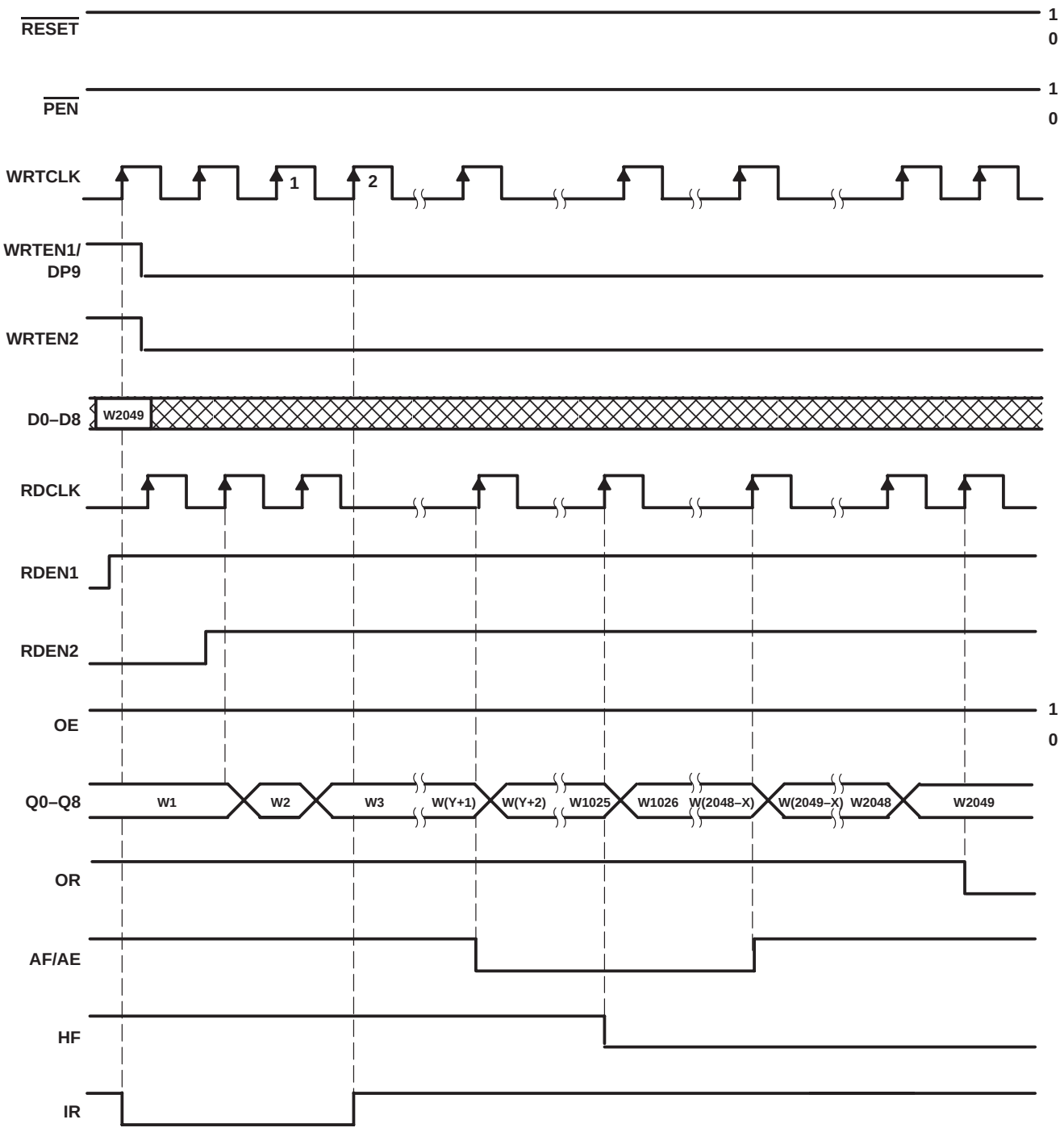


Figure 4. Read Cycle

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Voltage range applied to a disabled 3-state output . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): FN package . . . . . 46°C/W
PAG package . . . . . 58°C/W
PM package . . . . . 67°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			’ACT7807-15		’ACT7807-20		’ACT7807-25		’ACT7807-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, flags		–8		–8		–8		–8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0				400	µA
ΔI_{CC}§	WRTEN1/DP9	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2	mA
	Other inputs						1	
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 5)

			'ACT7807-15		'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		8		9		13		ns
		RDCLK high or low	6		8		9		13		
		$\overline{PEN}$ low	6		9		9		13		
t_{su}	Setup time	D0–D8 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, WRTEN2 before WRTCLK↑	4		5		5		5		
		OE, RDEN1, RDEN2 before RDCLK↑	5		6		6		6.5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑†	7		8		8		8		
		$\overline{PEN}$ before WRTCLK↑	4		5		5		5		
t_h	Hold time	D0–D8 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, WRTEN2 after WRTCLK↑	0		0		0		0		
		OE, RDEN1, RDEN2 after RDCLK↑	0		0		0		0		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑†	5		5		5		5		
		$\overline{PEN}$ high after WRTCLK↓	0		0		0		0		
		$\overline{PEN}$ low after WRTCLK↑	3		3		3		3		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 5)

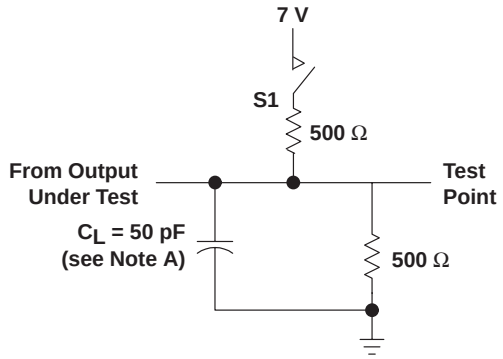
PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7807-15			'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	3	9	12	3	13	3	18	3	25	ns
t_{pd}§	RDCLK↑	Any Q		8								ns
t_{pd}	WRTCLK↑	IR	1		9	1	12	1	14	1	16	ns
	RDCLK↑	OR	1		9	2	12	2	14	2	16	
	WRTCLK↑	AF/AE	2		16	2	20	2	25	2	30	
	RDCLK↑		2		17	2	20	2	25	2	30	
t_{PLH}	WRTCLK↑	HF	2		19	2	21	2	23	2	25	ns
t_{PHL}	RDCLK↑	HF	2		16	2	18	2	20	2	22	ns
t_{PLH}	$\overline{RESET}$ low	AF/AE	1		12	1	18	1	22	1	24	ns
t_{PHL}	$\overline{RESET}$ low	HF	2		12	2	18	2	22	2	24	ns
t_{en}	OE	Any Q	2		10	2	13	2	15	2	18	ns
t_{dis}	OE	Any Q	1		11	1	13	1	15	1	18	ns

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This parameter is measured with C_L = 30 pF (see Figure 6).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

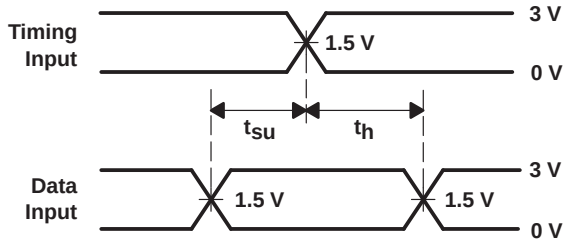
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	91	pF

PARAMETER MEASUREMENT INFORMATION

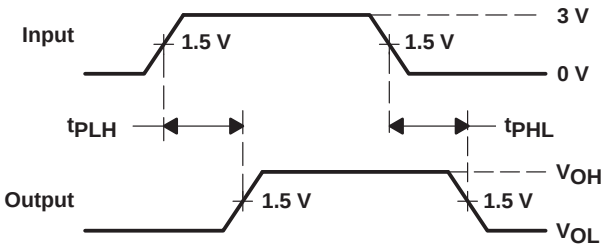


LOAD CIRCUIT

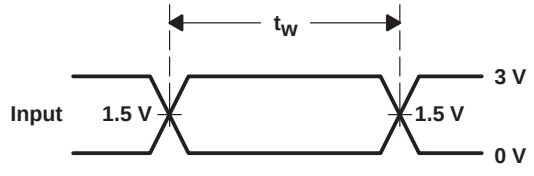
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



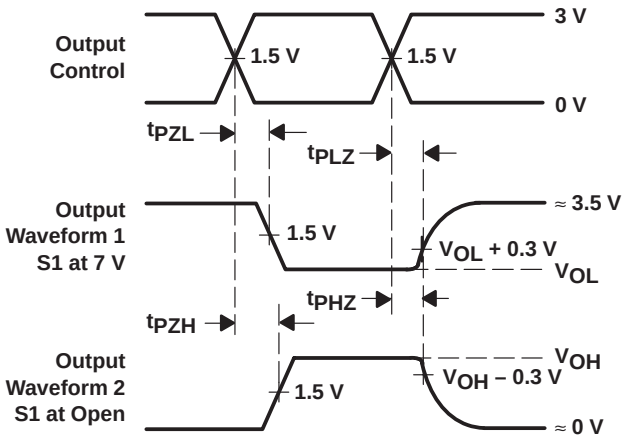
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTE A: C_L includes probe and jig capacitance.

Figure 5. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

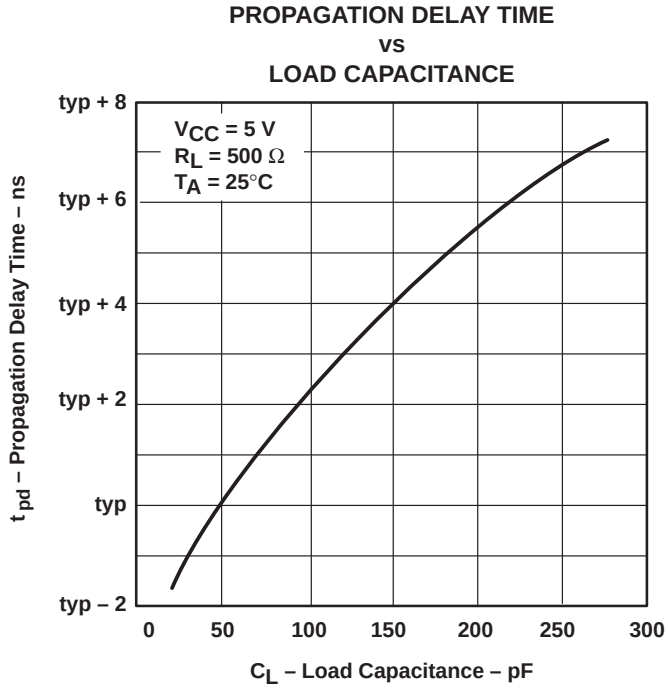


Figure 6

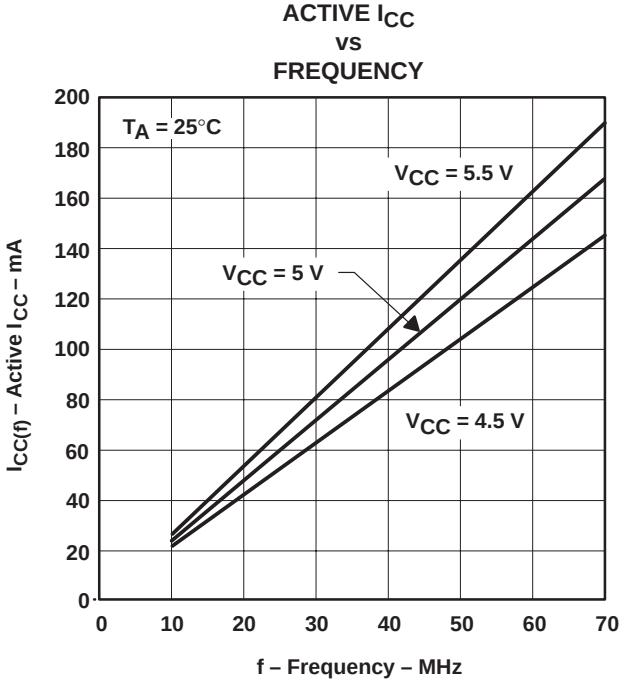


Figure 7

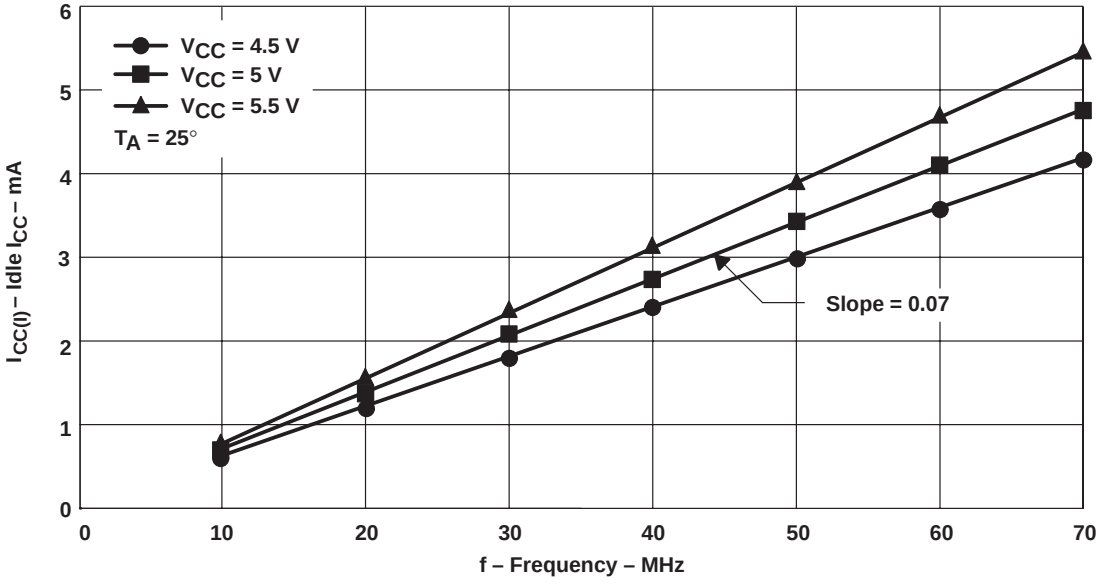


Figure 8. SN74ACT7807 Idle I_{CC} With WRTCLK Switching, Other Inputs at 0 or V_{CC} – 0.2 V and Outputs Disconnected

APPLICATION INFORMATION

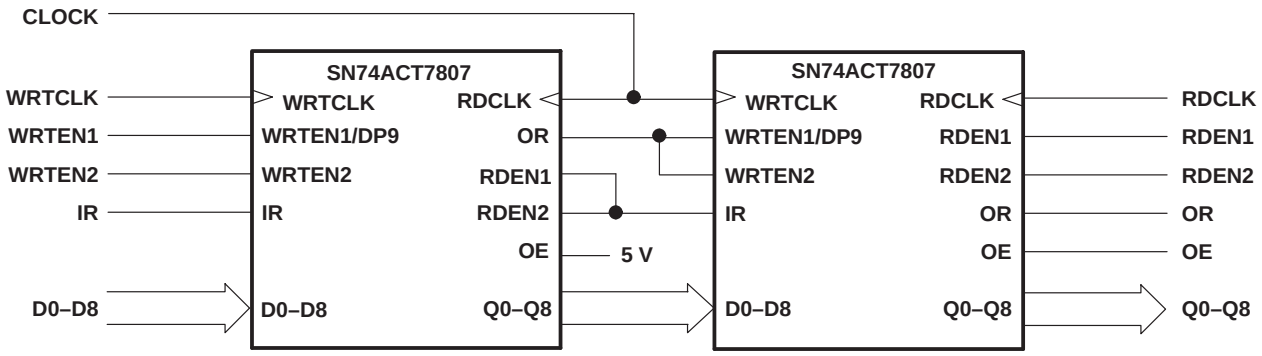


Figure 9. Word-Depth Expansion: 4096 × 9 Bits

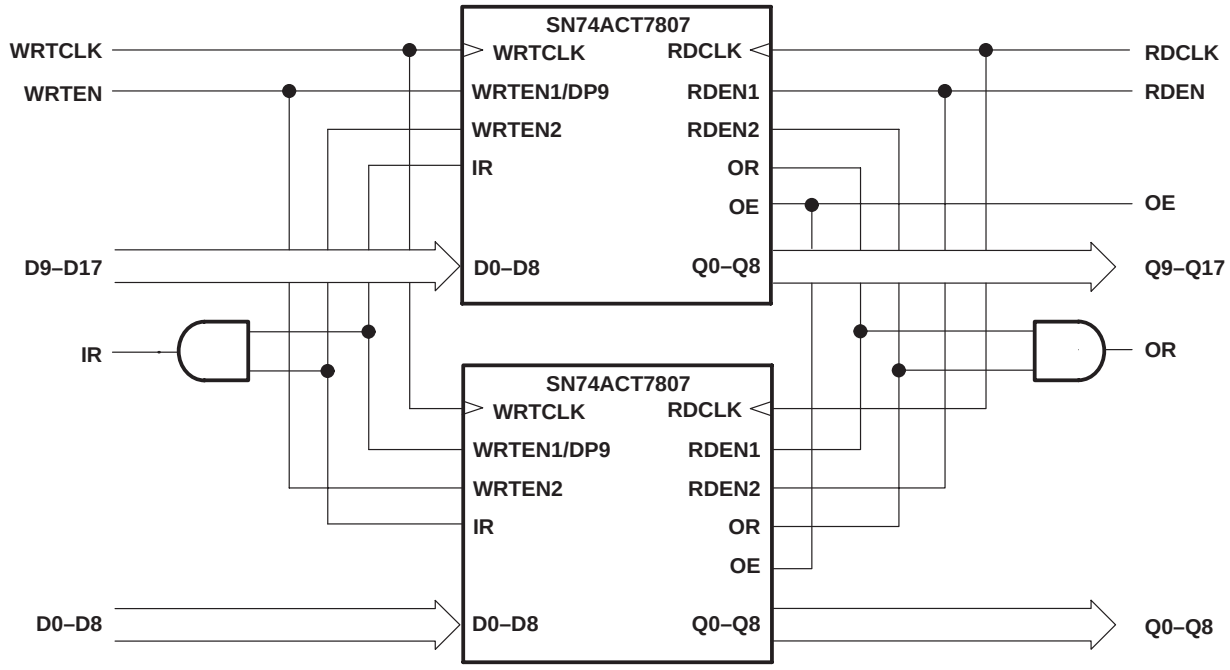


Figure 10. Word-Width Expansion: 2048 × 18 Bits

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT7807-15FN	NRND	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	SN74 ACT7807-15FN	
SN74ACT7807-15PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI	0 to 70		
SN74ACT7807-20FN	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	SN74 ACT7807-20FN	Samples
SN74ACT7807-20PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI	0 to 70		
SN74ACT7807-25PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI	0 to 70		
SN74ACT7807-40PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

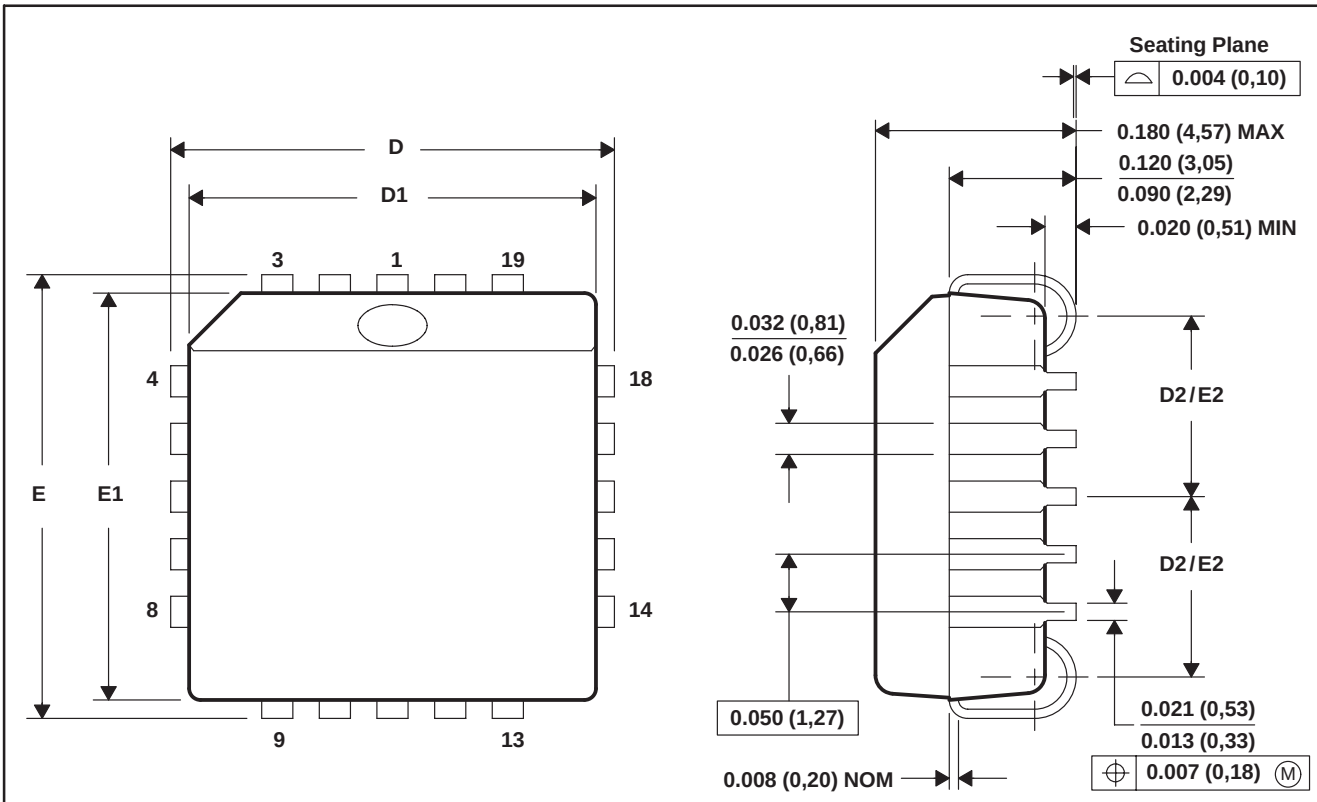
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN

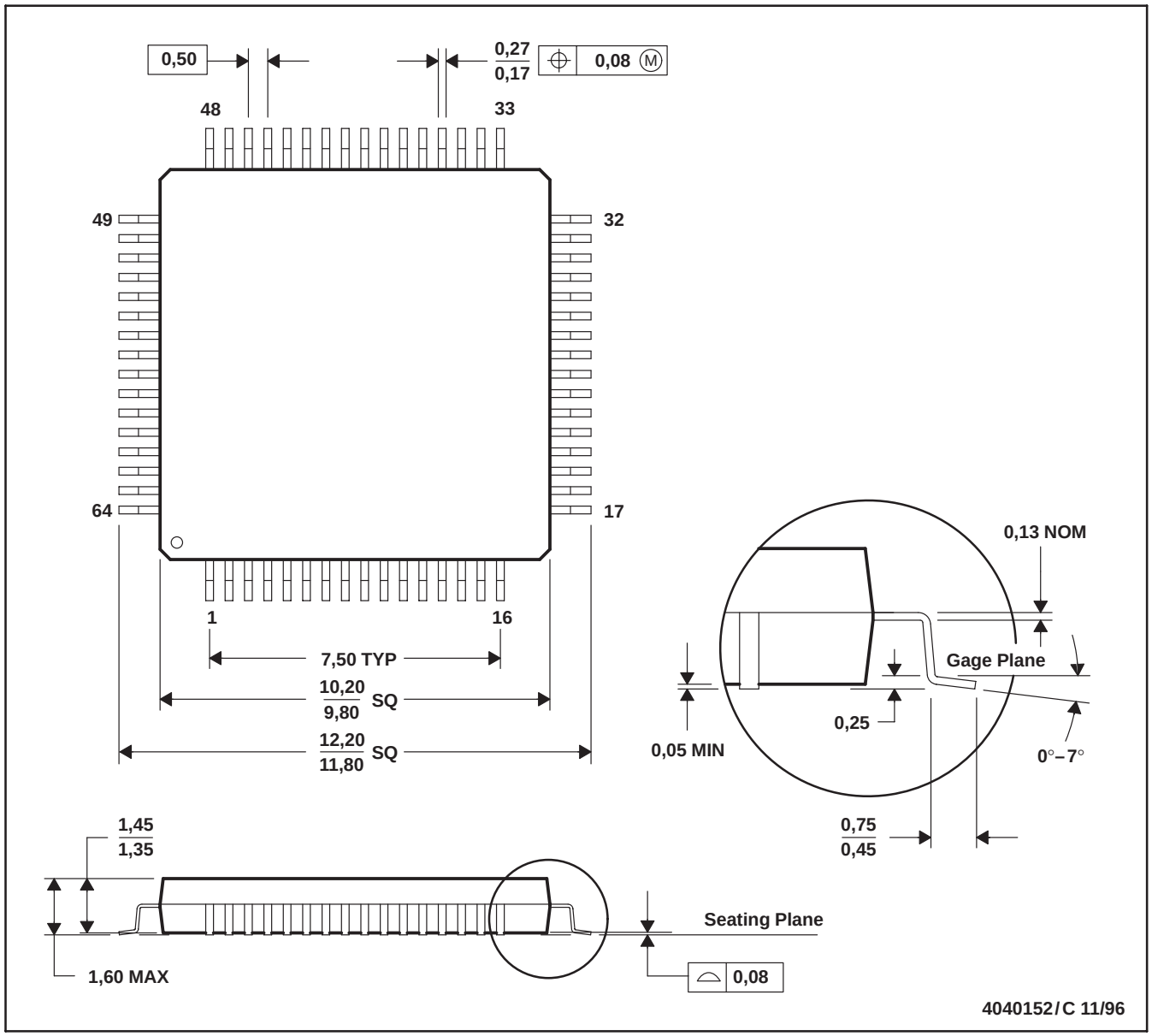


NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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