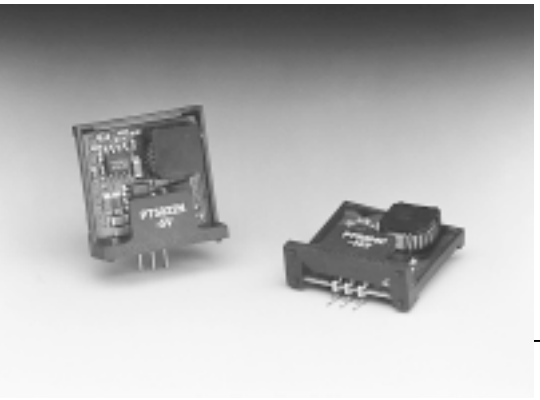
PT5020 Series

Positive Input/Negative Output Integrated Switching Regulator

SLTS025B

(Revised 12/19/2001)



Features

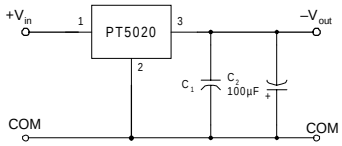
- Negative Output
- Input Voltage Range: +4.75 to +7 Volts
- Laser-Trimmed
- Small Footprint
- Soft Start
- 5-Pin Mount Option (Suffixes L & M)

Description

The PT5020 series of integrated switching regulators (ISRs) convert a positive input voltage, typically +5V, to a negative output voltage for a wide range of analog and datacom applications.

These Plus to Minus ISRs incorporate a "Buck-Boost" topology and are packaged in the 3-pin, single in-line pin (SIP) package configuration.

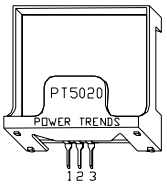
Standard Application



C_1 = Optional ceramic (1-5µF)
C_2 = Required Electrolytic (100µF)

Pin-Out Information

Pin	Function
1	V_{in}
2	GND
3	V_{out}



Ordering Information

PT5021 ☐ = -3.3 Volts
PT5022 ☐ = -5 Volts
PT5023 ☐ = -9 Volts
PT5024 ☐ = -12 Volts
PT5025 ☐ = -15 Volts
PT5026 ☐ = -5.2 Volts
PT5027 ☐ = -8.0 Volts
PT5028 ☐ = -6.5 Volts
PT5029 ☐ = -5.5 Volts
PT5030 ☐ = -6.0 Volts
PT5031 ☐ = -1.7 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code *
Vertical	**N**	(EAD)
Horizontal	**A**	(EAA)
SMD	**C**	(EAC)
Horizontal, 2-pin Tab	**M**	(EAM)
SMD, 2-Pin Tab	**L**	(EAL)

** Previously known as package styles 100/110.*

(Reference the applicable package code drawing for the dimensions and PC board layout)

NOTE: PT5020 ISRs are not Short-Circuit Protected.

Specifications (Unless otherwise stated, T_a =25°C, V_{in} =5V, I_o =$I_o$max, C_2 =100µF)

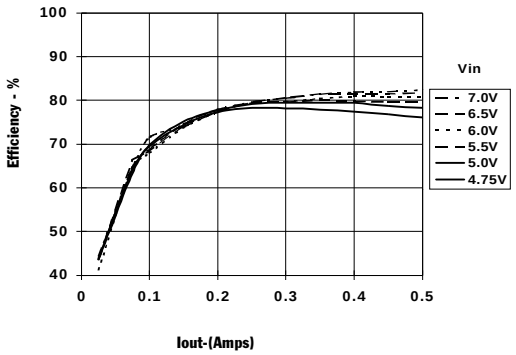
Characteristics	Symbol	Conditions	PT5020 SERIES Min	Typ	Max	Units
Output Current	I_o	Over V_{in} range, V_o= –1.7V to –6.5V	0.25 (1)	—	1.0	A
		V_o= –9V	0.10 (1)	—	0.60	
		V_o= –12V	0.10 (1)	—	0.50	
		V_o= –15V	0.10 (1)	—	0.30	
Input Voltage Range	V_{in}	Over I_o range	4.75	—	7 (2)	V
Output Voltage Tolerance	ΔV_o	Over V_{in} Range, T_a = -20°C to SOA limit (3)	—	±1.5	±3	%V_o
Line Regulation	Reg_{line}	Over V_{in} range	—	±0.5	±1	%V_o
Load Regulation	Reg_{load}	$I_o$min ≤ I_o ≤ $I_o$max	—	±0.5	±1	%V_o
Efficiency	η	I_o =0.5 $I_o$max	—	75	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	—	±2	±5	%V_o
Transient Response	t_{tr}	25% load change	—	500	—	µSec
		V_o over/undershoot	—	3.0	5.0	%V_o
Current Limit	I_{lim}		—	150	—	%$I_o$max
Inrush Current	I_{ir}	On start up	—	1.0 (3)	—	A
	t_{ir}		—	1.0	—	mSec
Switching Frequency	f_s	Over I_o range, $\lvert V_o \rvert$ =1.7 to 8V	0.8	1	1.2	MHz
		$\lvert V_o \rvert$ ≥8 V	500	650	800	kHz
Operating Temperature Range	T_a	—	-20	—	+85 (4)	°C
Thermal Resistance	θ_{ja}	Free Air Convection (40-60LFM)	—	50	—	°C/W
Storage Temperature	T_s		-40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, Half Sine, mounted to a fixture	—	500	—	G's
Mechanical Vibration Per Mil-STD-883D, 20-2000 Hz		Suffixes N, A, & C	—	5	—	G's
		Suffixes L & M	—	20	—	
Weight		Suffixes N, A, & C	—	4.5	—	grams
		Suffixes L & M	—	6.5 (5)	—	

Notes: *(1) The ISR will operate at no load with reduced specifications.*
(2) For applications with input voltages greater than 7 VDC, use the PT78NR100 Series.
(3) The inrush current stated is above the normal input current for the associated output load.
(4) See Safe Operating Area curves or consult the factory for the appropriate derating
(5) The tab pins on the 5-pin mount package types (suffixes L & M) must be soldered. For more information see the applicable package outline drawing.

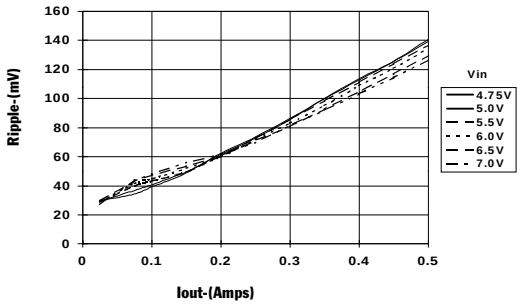
Typical Characteristics

PT5024 (-12VDC) (See Note A)

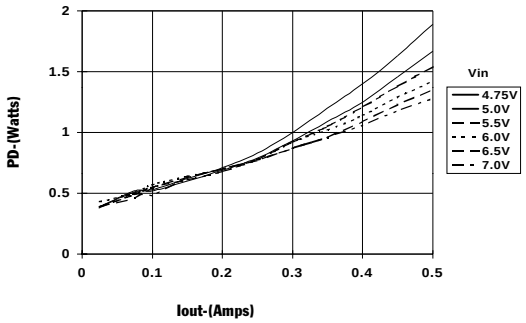
Efficiency vs Output Current



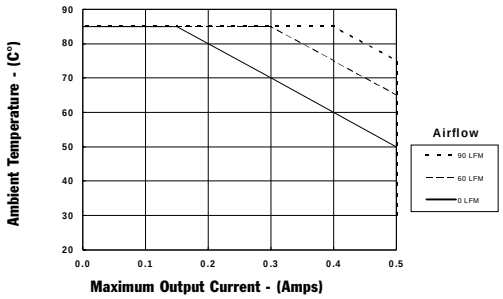
Ripple Voltage vs Output Current



Power Dissipation vs Output Current

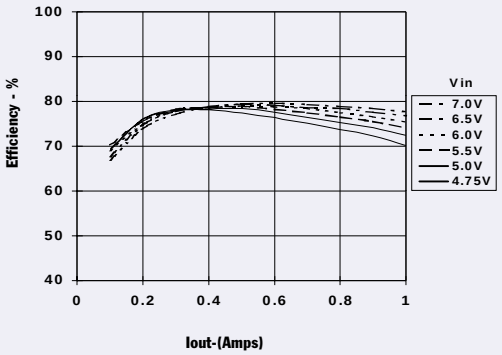


Safe Operating Area (V_{IN}=5V) (See Note B)

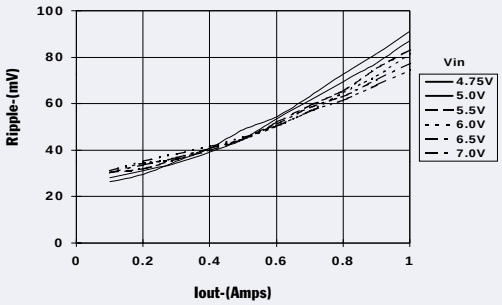


PT5022 (-5VDC) (See Note A)

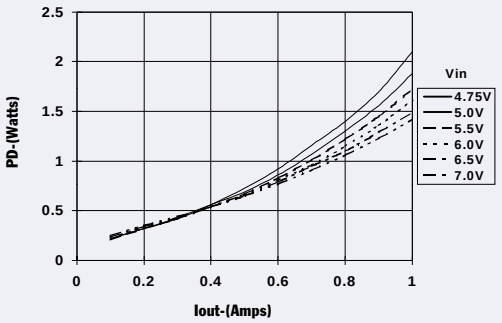
Efficiency vs Output Current



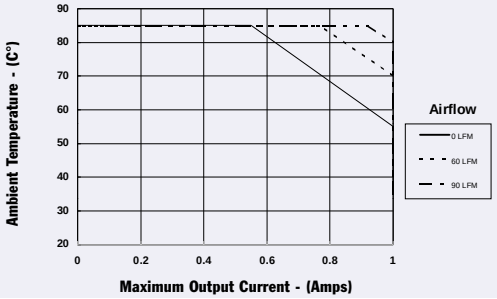
Ripple Voltage vs Output Current



Power Dissipation vs Output Current



Safe Operating Area (V_{IN}=5V) (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *Thermal derating graphs are developed in free-air convection cooling, which corresponds to approximately 40–60LFM of airflow.*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PT5021J	OBSOLETE	SIP MODULE	EAJ	3		TBD	Call TI	Call TI			
PT5023A	OBSOLETE	SIP MODULE	EAA	3		TBD	Call TI	Call TI			
PT5026LT	OBSOLETE	SIP MODULE	EAL	3		TBD	Call TI	Call TI			
PT5027A	OBSOLETE	SIP MODULE	EAA	3		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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