

# NTHD5905T1

## Power MOSFET Dual P-Channel ChipFET™

3.0 Amps, 8 Volts

### Features

- Low  $R_{DS(on)}$  for Higher Efficiency
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package

### Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	5 secs	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	-8.0		V
Gate-Source Voltage	$V_{GS}$	$\pm 8.0$		V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$I_D$	$\pm 4.1$ $\pm 2.9$	$\pm 3.0$ $\pm 2.2$	A
Pulsed Drain Current	$I_{DM}$	$\pm 10$		A
Continuous Source Current (Diode Conduction) (Note 1)	$I_S$	-1.8	-0.9	A
Maximum Power Dissipation (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$P_D$	2.1 1.1	1.1 0.6	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150		$^\circ\text{C}$

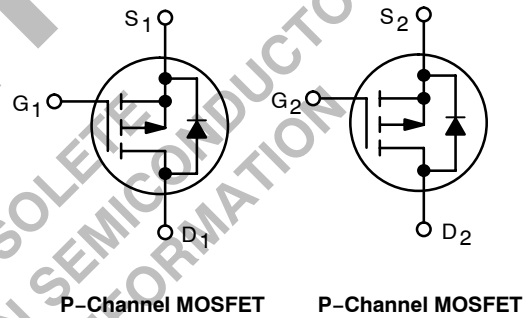
1. Surface Mounted on 1" x 1" FR4 Board.



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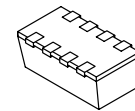
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**DUAL P-CHANNEL  
3.0 AMPS, 8 VOLTS  
 $R_{DS(on)} = 90 \text{ m}\Omega$**



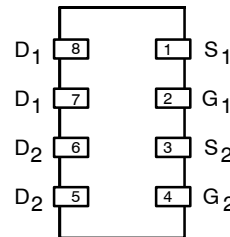
P-Channel MOSFET

P-Channel MOSFET

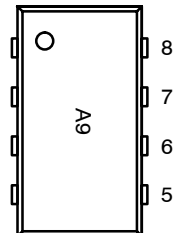


ChipFET  
CASE 1206A  
STYLE 2

### PIN CONNECTIONS



### MARKING DIAGRAM



A9 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
NTHD5905T1	ChipFET	3000/Tape & Reel

# NTHD5905T1

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient (Note 2) t ≤ 5 sec Steady State	R <sub>thJA</sub>	50 90	60 110	°C/W
Maximum Junction-to-Foot (Drain) Steady State	R <sub>thJF</sub>	30	40	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### Static

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.45	-	-	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8.0 V	-	-	±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -6.4 V, V <sub>GS</sub> = 0 V	-	-	-1.0	μA
		V <sub>DS</sub> = -6.4 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85°C	-	-	-5.0	
On-State Drain Current (Note 3)	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5.0 V, V <sub>GS</sub> = -4.5 V	-10	-	-	A
Drain-Source On-State Resistance (Note 3)	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.0 A	-	0.075	0.090	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -2.5 A	-	0.110	0.130	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -1.0 A	-	0.150	0.180	
Forward Transconductance (Note 3)	g <sub>fs</sub>	V <sub>DS</sub> = -5.0 V, I <sub>D</sub> = -3.0 A	-	7.0	-	S
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	I <sub>S</sub> = -0.9 A, V <sub>GS</sub> = 0 V	-	-0.8	-1.2	V

### Dynamic (Note 4)

Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -4.0 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.0 A	-	5.5	9.0	nC
Gate-Source Charge	Q <sub>gs</sub>		-	0.5	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	1.5	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -4.0 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> = -1.0 A, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6 Ω	-	10	15	ns
Rise Time	t <sub>r</sub>		-	45	70	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	30	45	
Fall Time	t <sub>f</sub>		-	10	15	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -0.9 A, di/dt = 100 A/μs	-	30	60	

2. Surface Mounted on 1" x 1" FR4 Board.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL CHARACTERISTICS

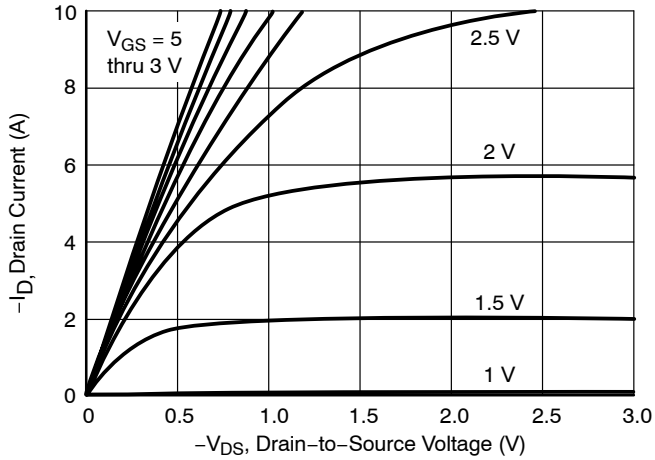


Figure 1. Output Characteristics

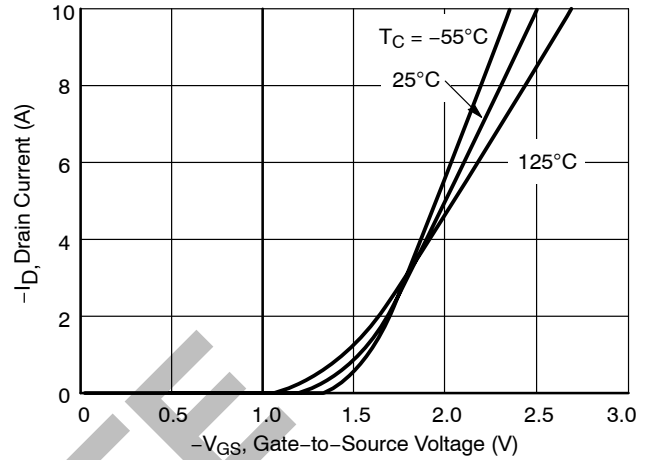


Figure 2. Transfer Characteristics

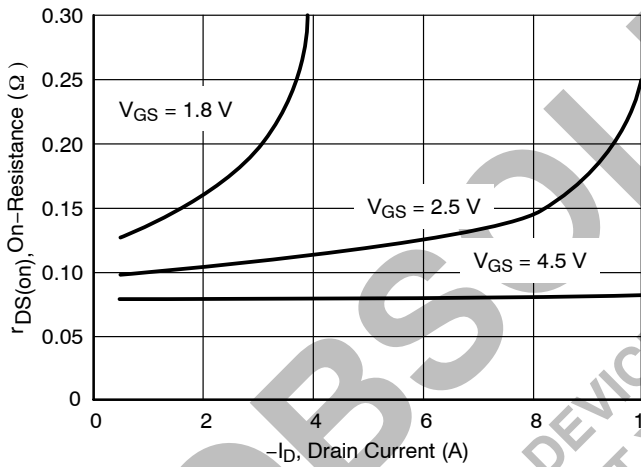


Figure 3. On-Resistance vs. Drain Current

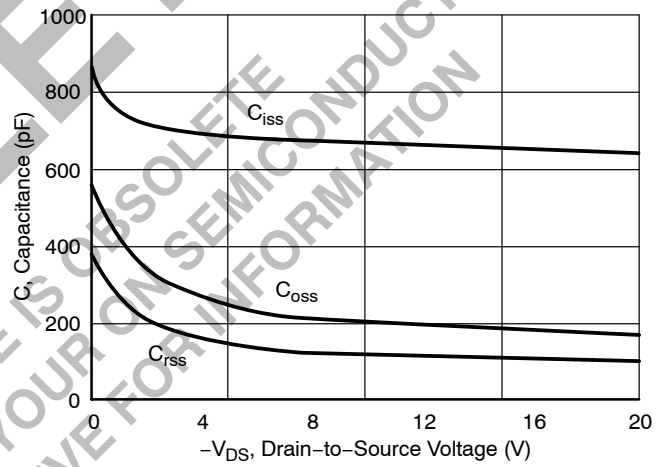


Figure 4. Capacitance

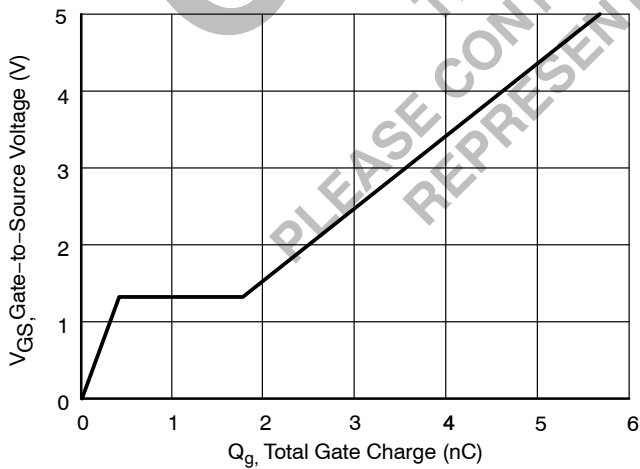


Figure 5. Gate Charge

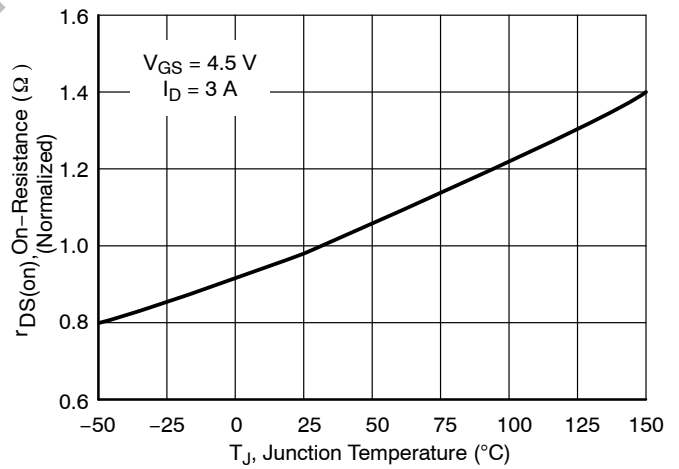


Figure 6. On-Resistance vs. Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

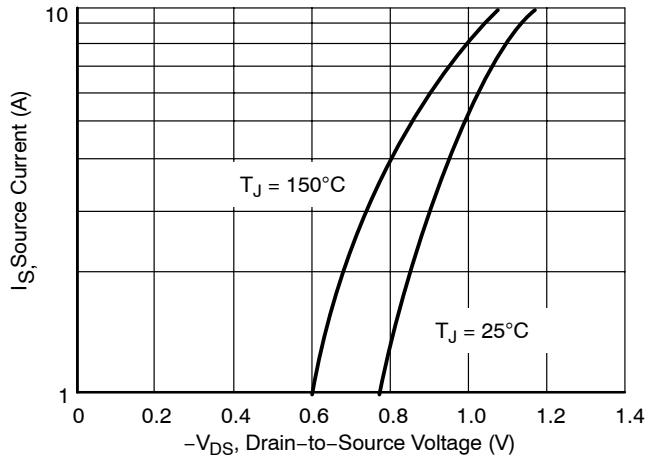


Figure 7. Source Diode Forward Voltage

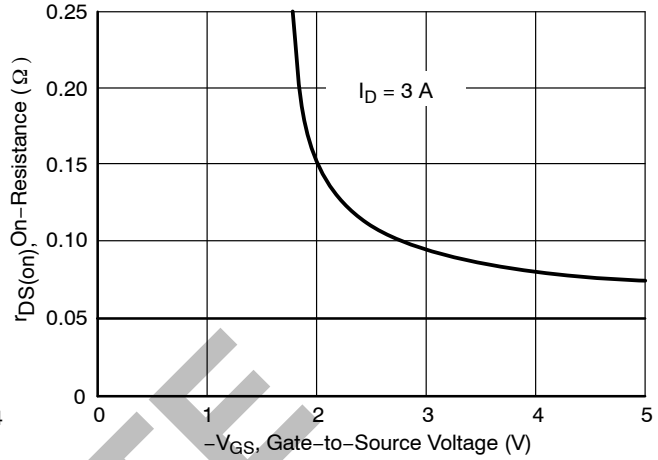


Figure 8. On-Resistance vs. Gate-to-Source Voltage

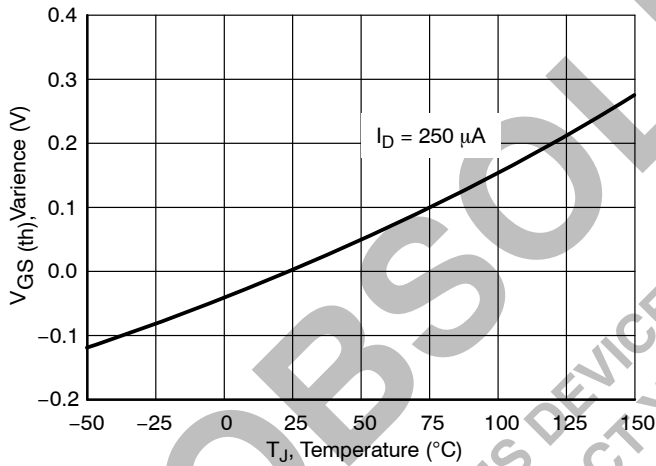


Figure 9. Threshold Voltage

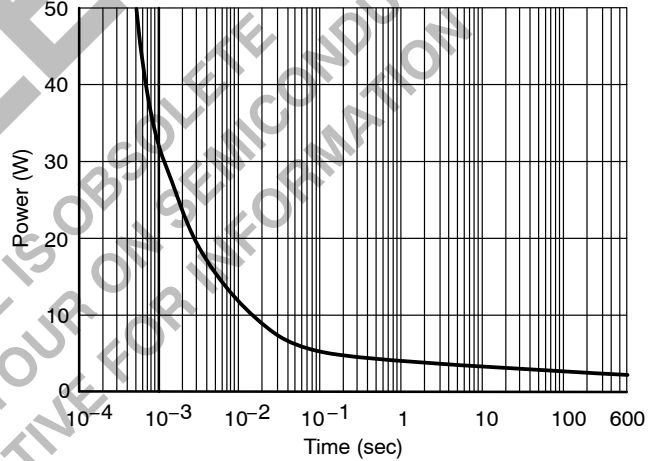


Figure 10. Single Pulse Power

TYPICAL ELECTRICAL CHARACTERISTICS

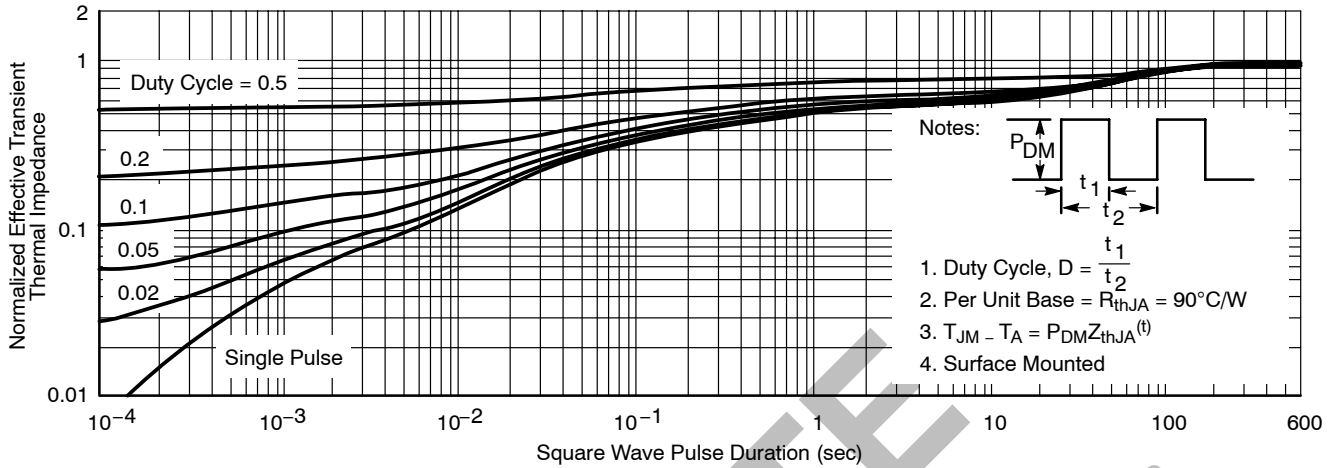


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

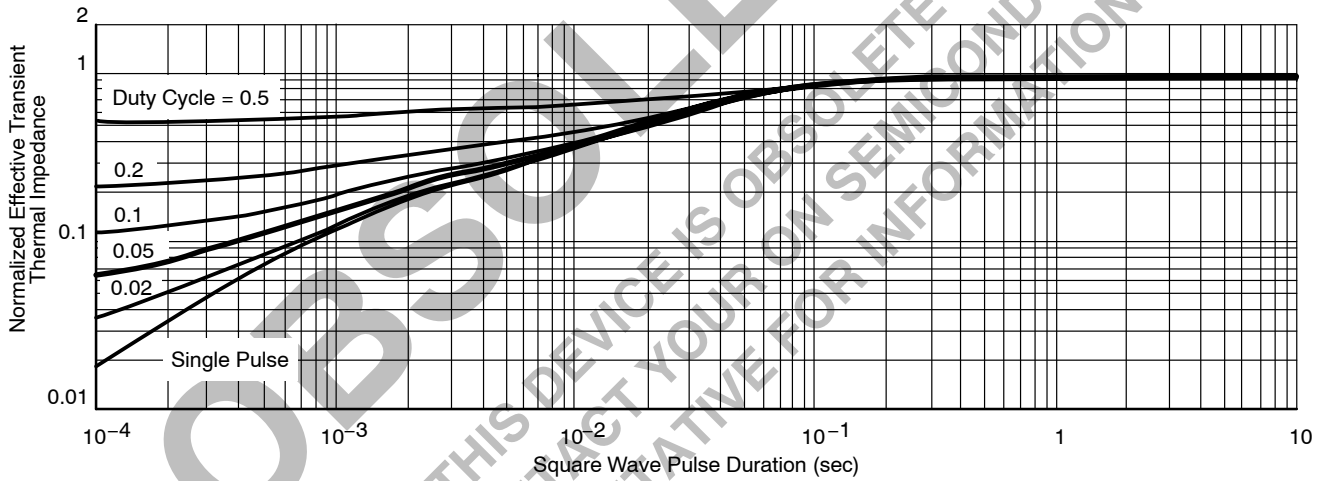


Figure 12. Normalized Thermal Transient Impedance, Junction-to-Foot

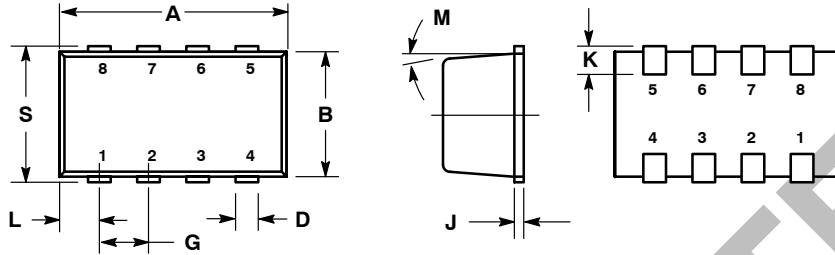
**Notes**

**OBSOLETE**  
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# NTHD5905T1

## PACKAGE DIMENSIONS

ChipFET  
CASE 1206A-03  
ISSUE D



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.



0.05 (0.002)

### STYLE 2:

- PIN 1. SOURCE 1  
2. GATE 1  
3. SOURCE 2  
4. GATE 2  
5. DRAIN 2  
6. DRAIN 2  
7. DRAIN 1  
8. DRAIN 1

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5° NOM		5° NOM	
S	1.80	2.00	0.072	0.080


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