Freescale Semiconductor
Advance Information

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MPC8641 and MPC8641D PowerPC™ Integrated Processor Hardware Specifications

1 Overview

The MPC8641 processor family integrates either one or two PowerPC™ e600 processor cores with system logic required for networking, storage, wireless infrastructure, and general-purpose embedded applications. The MPC8641 integrates one e600 core while the MPC8641D integrates two cores.

This section provides a high-level overview of the MPC8641 and MPC8641D features. When referring to the MPC8641 throughout the document, the functionality described applies to both the MPC8641 and the MPC8641D. Any differences specific to the MPC8641D are noted.

Figure 1 shows the major functional units within the MPC8641 and MPC8641D. The major difference between the MPC8641 and MPC8641D is that there are two cores on the MPC8641D.

Contents

This document contains information on a new product. Specifications and information herein are subject to change without notice.

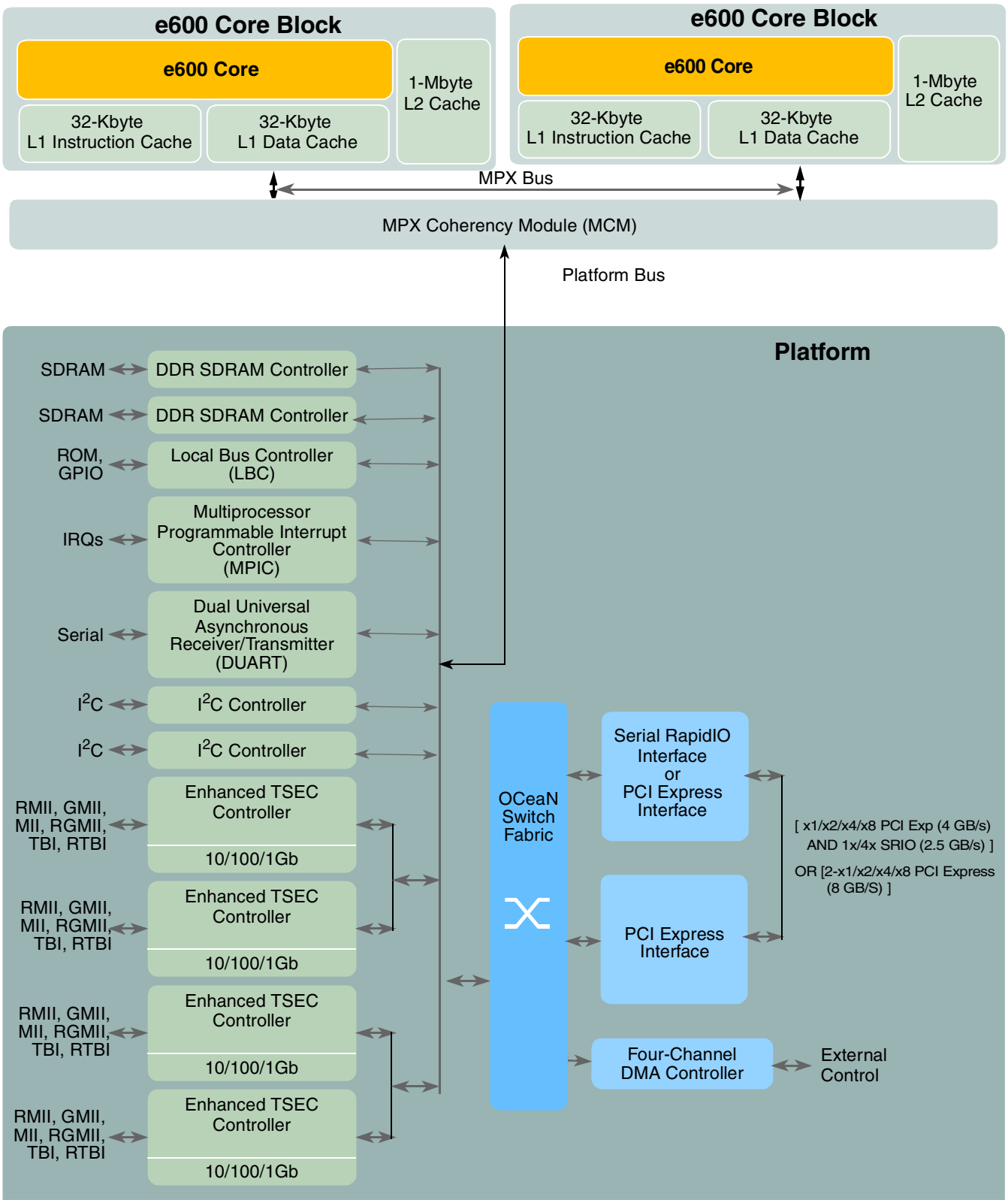


Figure 1. MPC8641 and MPC8641D

1.1 Key Features

The following lists an overview of the MPC8641 key feature set:

- Major features of the e600 core are as follows:
  - High-performance, 32-bit superscalar microprocessor that implements the PowerPC architecture
  - Eleven independent execution units and three register files
    - Branch processing unit (BPU)
    - Four integer units (IUs) that share 32 GPRs for integer operands
    - 64-bit floating-point unit (FPU)
    - Four vector units and a 32-entry vector register file (VRs)
    - Three-stage load/store unit (LSU)
  - Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle.
  - Rename buffers
  - Dispatch unit
  - Completion unit
  - Two separate 32-Kbyte instruction and data level 1 (L1) caches
  - Integrated 1-Mbyte, eight-way set-associative unified instruction and data level 2 (L2) cache with ECC
  - 36-bit real addressing
  - Separate memory management units (MMUs) for instructions and data
  - Multiprocessing support features
  - Power and thermal management
  - Performance monitor
  - In-system testability and debugging features
  - Reliability and serviceability
- MPX coherency module (MCM)
  - Ten local address windows plus two default windows
  - Optional low memory offset mode for core 1 to allow for address disambiguation
- Address translation and mapping units (ATMUs)
  - Eight local access windows define mapping within local 36-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
  - Three inbound windows plus a configuration window on PCI Express
  - Four inbound windows plus a default window on serial RapidIO
  - Four outbound windows plus default translation for PCI Express
  - Eight outbound windows plus default translation for serial RapidIO with segmentation and sub-segmentation support

- DDR memory controllers
  - Dual 64-bit memory controllers (72-bit with ECC)
  - Support of up to a 333-MHz clock rate and a 667-MHz DDR2 SDRAM
  - Support for DDR, DDR2 SDRAM
  - Up to 16 Gbytes per memory controller
  - Cache line and page interleaving between memory controllers.
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification*, Revision 1.2
  - Both 1x and 4x LP-Serial link interfaces
  - Transmission rates of 1.25-, 2.5-, and 3.125-Gbaud (data rates of 1.0-, 2.0-, and 2.5-Gbps) per lane
  - RapidIO–compliant message unit
  - RapidIO atomic transactions to the memory controller
- PCI Express interface
  - PCI Express 1.0a compatible
  - Supports x1, x2, x4, and x8 link widths
  - 2.5 Gbaud, 2.0 Gbps lane
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support of the following physical interfaces: MII, RMII, GMII, RGMII, TBI, and RTBI
  - Support a full-duplex FIFO mode for high-efficiency ASIC connectivity
  - TCP/IP off-load
  - Header parsing
  - Quality of service support
  - VLAN insertion and deletion
  - MAC address recognition
  - Buffer descriptors are backward compatible with PowerQUICC II and PowerQUICC III programming models
  - RMON statistics support
  - MII management interface for control and status
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts and 48 internal interrupts
  - Eight global high resolution timers/counters that can generate interrupts
  - Allows processors to interrupt each other with 32b messages

  - Support for PCI-Express message-shared interrupts (MSIs)
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 166 MHz
  - Eight chip selects support eight external slaves
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and the remote masters
  - Supports transfers to or from any local memory or I/O port
  - Ability to start and flow control each DMA channel from external 3-pin interface
- Device performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- Dual I^2C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- IEEE 1149.1-compliant, JTAG boundary scan
- Available as 1023 pin Hi-CTE flip chip ceramic land grid (FC-CLGA) and ceramic ball grid array (FC-CBGA)

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8641. The MPC8641 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Recommended Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0 V_{DD}_Core1	-0.3 to 1.21 V	V	2, 3
Cores PLL supply	AV_{DD}_Core0 AV_{DD}_Core1	-0.3 to 1.21 V	V	
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	-0.3 to 1.21 V	V	
SerDes Serial I/O Supply Port 1	XV_{DD}_SRDS1	-0.3 to 1.21V	V	
SerDes Serial I/O Supply Port 2	XV_{DD}_SRDS2	-0.3 to 1.21 V	V	
Serdes DLL and PLL supply voltage for Port 1 and Port 2	AV_{DD}_SRDS1 AV_{DD}_SRDS2	-0.3 to 1.21V	V	
Platform Supply voltage	V_{DD}_PLAT	-0.3 to 1.21V	V	
Local Bus and Platform PLL supply voltage	AV_{DD}_LB AV_{DD}_PLAT	-0.3 to 1.21V	V	
DDR and DDR2 SDRAM I/O supply voltages	D1_GV_{DD} D2_GV_{DD}	-0.3 to 2.75 V -0.3 to 1.98 V	V	3
eTSEC 1 and 2 I/O supply voltage	LV_{DD}	-0.3 to 3.63 V -0.3 to 2.75 V	V	4
eTSEC 3 and 4 I/O supply voltage	TV_{DD}	-0.3 to 3.63 V -0.3 to 2.75 V	V	4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD}	-0.3 to 3.63V	V	6

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Input voltage	DDR and DDR2 SDRAM signals	D*n*_MV_{IN}	- 0.3 to (D*n*_GV_{DD} + 0.3)	V	3, 5
	DDR and DDR2 SDRAM reference	D*n*_MV_{REF}	- 0.3 to (D*n*_GV_{DD} + 0.3)	V	5
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to (LV_{DD}+ 0.3) GND to (TV_{DD}+ 0.3)	V	4, 5
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{IN}	GND to ($0V_{DD}$+ 0.3)	V	6, 5
Storage temperature range		T_{STG}	-55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Core 1 characteristics apply only to MPC8641D
3. **Caution:** MV_{IN} must not exceed D*n*_GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,T,O)V_{IN} and D*n*_MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. The -0.3 to 2.75 V is for DDR and -0.3 to 1.98 V is for DDR2.

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8641. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 21, "Ordering Information."

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0 V_{DD}_Core1	1.10 ± 50 mV	V	1, 2, 8
		1.05 ± 50 mV		1, 2, 7
Cores PLL supply	AV_{DD}_Core0 AV_{DD}_Core1	1.10 ± 50 mV	V	8
		1.05 ± 50 mV		7
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	1.10 ± 50 mV	V	8
		1.05 ± 50 mV		7

Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
SerDes Serial I/O Supply Port 1		XV_{DD}_SRDS1	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
SerDes Serial I/O Supply Port 2		XV_{DD}_SRDS2	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
Serdes DLL and PLL supply voltage for Port 1 and Port 2		AV_{DD}_SRDS1 AV_{DD}_SRDS2	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
Platform Supply voltage		V_{DD}_PLAT	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
Local Bus and Platform PLL supply voltage		AV_{DD}_LB AV_{DD}_PLAT	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
DDR and DDR2 SDRAM I/O supply voltages		D1_GV_{DD} D2_GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	2, 3, 9
eTSEC 1 and 2 I/O supply voltage		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	2, 4
eTSEC 3 and 4 I/O supply voltage		TV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	2, 4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	2, 5
Input voltage	DDR and DDR2 SDRAM signals	D*n*_MV_{IN}	GND to D*n*_GV_{DD}	V	3, 6
	DDR and DDR2 SDRAM reference	D*n*_MV_{REF}	D*n*_GV_{DD}/2 ± 1%	V	6
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4, 6
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{IN}	GND to OV_{DD}	V	5, 6

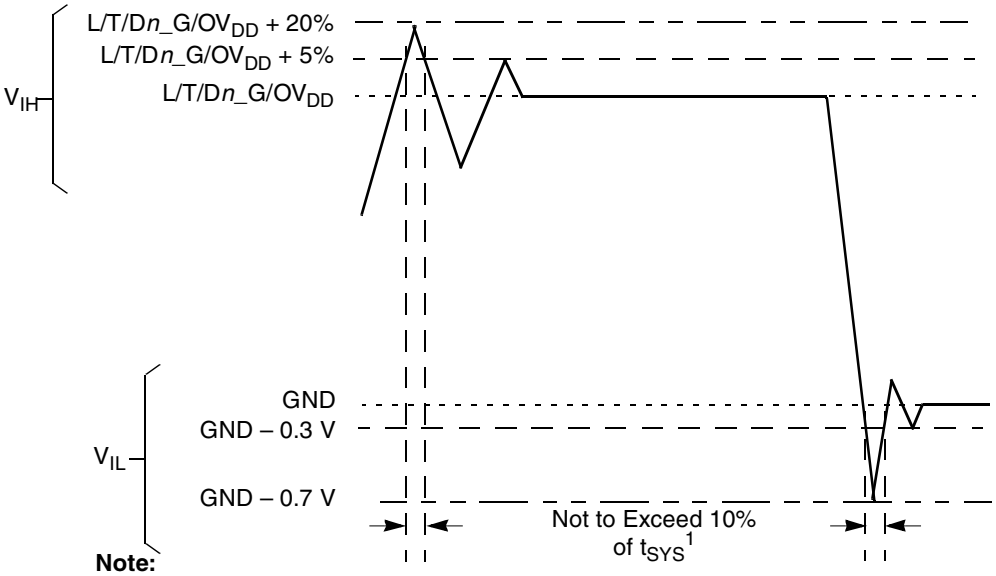
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	T_J	0 to 105	°C	

Notes:

1. Core 1 characteristics apply only to MPC8641D
2. **Caution:** Until V_{DD}_Core*n* reaches its recommended operating voltage, V_{DD}_Core*n* may exceed L/T/D*n*_G/S/OV_{DD} by up to 0.7 V. If 0.7 V is exceeded, extra current will be drawn by this device.
3. **Caution:** MV_{IN} must not exceed D*n*_GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. (M,L,T,O)V_{IN} and D*n*_MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2
7. Applies to a core frequency of 1333 MHz and below
8. Applies to a core frequency above 1333 MHz.
9. The 2.5 V ± 125 mV is for DDR and 1.8 V ± 90 mV is for DDR2.
10. GMII, MII, RMII, RGMII, RTBI, TBI and FIFO can be ran at 2.5 V ± 125 mV while GMII, MII, RMII, and TBI can be ran at 3.3 V ± 165 mV.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8641.



Note:
1. Note that t_{SYS} refers to the clock period associated with the SYSCLK signal.

Figure 2. Overshoot/Undershoot Voltage for D*n*_GV_{DD}/OV_{DD}/LV_{DD}

The MPC8641 core voltage must always be provided at nominal V_{DD}_Core*n* (See Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and L/TV_{DD} based receivers are simple CMOS I/O

circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied D*n*_MV_{REF} signal (nominally set to D*n*_GV_{DD}/2) as is appropriate for the (SSTL-18 and SSTL-2) electrical signaling standards.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR1 signal	18	D*n*_GV_{DD} = 2.5 V	4
DDR2 signal	18 32 (half strength mode)	D*n*_GV_{DD} = 1.8 V	1, 5
Local Bus signals	45 25	OV_{DD} = 3.3 V	2, 6
eTSEC/10/100 signals	45	T/LV_{DD} = 3.3 V	6
	30	T/LV_{DD} = 2.5 V	6
DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, JTAG and Miscellaneous I/O voltage	45	OV_{DD} = 3.3 V	6
I^2C	150	OV_{DD} = 3.3 V	7
SRIO, PCI Express	100	SV_{DD} = 1.1/1.05 V	3, 8

Notes:

1. See the DDR Control Driver registers in the MPC8641D reference manual for more information.
2. See the POR Impedance Control register in the MPC8641D reference manual for more information about local bus signals and their drive strength programmability.
3. See Section 17, “Signal Listings” for details on resistor requirements for the calibration (transmit and receive) signals
4. Stub Series Terminated Logic (SSTL-25) type pins.
5. Stub Series Terminated Logic (SSTL-18) type pins.
6. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
7. Open Drain type pins.
8. Low Voltage Differential Signaling (LVDS) type pins.

2.2 Power Sequencing

The MPC8641 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows:

The chronological order of power up is:

1.O/L/TV_{DD}

2. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core*n*, AV_{DD}_Core*n*, AV_{DD}_LB, SV_{DD}, XV_{DD}_SRDS*n*, AV_{DD}_SRDS*n* (This rail must reach 90% of its value before the rail for Dn_GV_{DD}, and Dn_MV_{REF} reaches 10% of its value)

3. D*n*_GV_{DD}, D*n*_MV_{REF}

4. SYSCLK

The recommended order of power down is as follows:

1. SYSCLK

2. D*n*_GV_{DD}, D*n*_MV_{REF}

3. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core*n*, AV_{DD}_Core*n*, AV_{DD}_LB, SV_{DD}, XV_{DD}_SRDS*n*, AV_{DD}_SRDS*n*

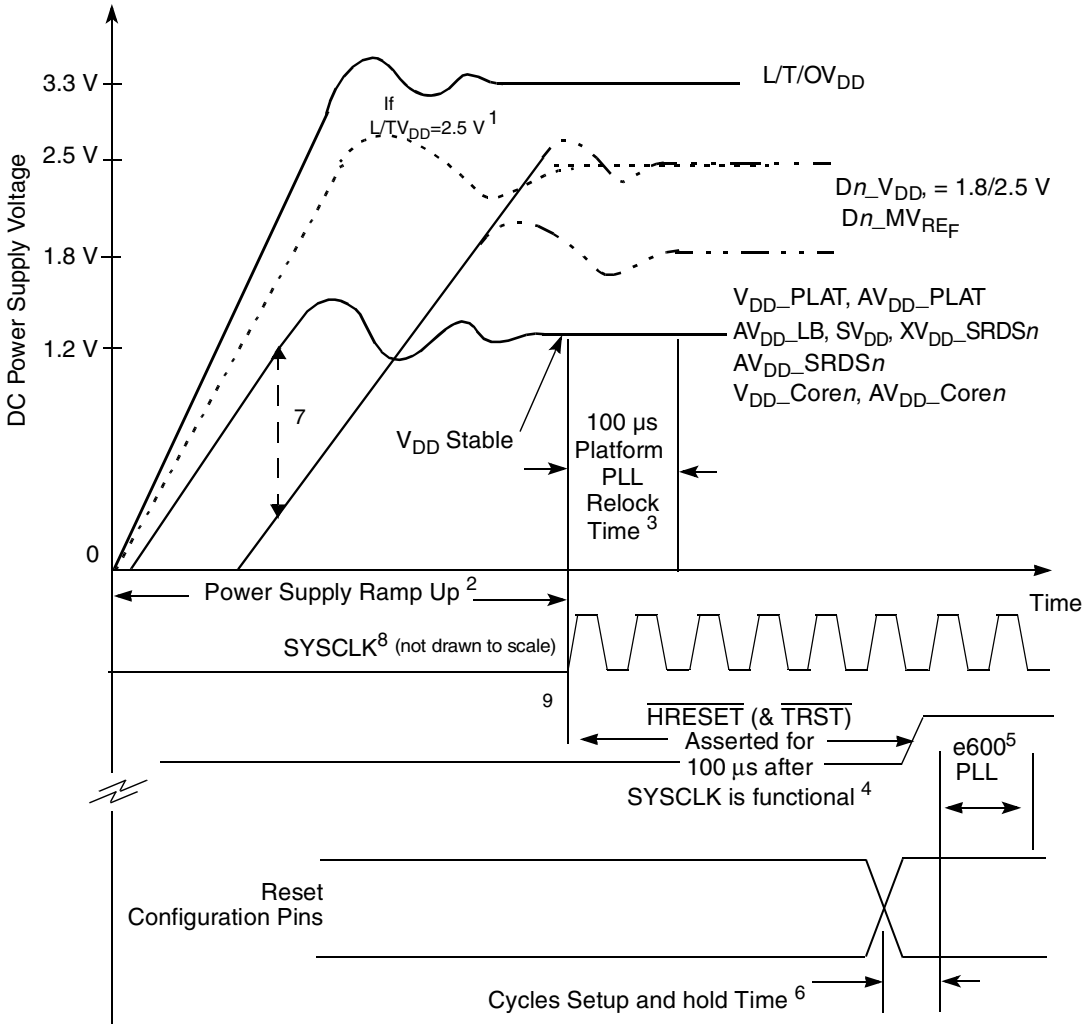
4. O/L/TV_{DD}

NOTE

The power supplies may power down simultaneously if the preservation of DDR*n* memory is not a concern.

AV_{DD} type supplies must be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 20.2.1, “PLL Power Supply Filtering”.

Figure 3 illustrates the Power Up sequence as described above.



Notes:

1. Dotted waveforms correspond to optional supply values for a specified power supply. See Table 2.
2. See Cautions section of Table 2 for additional information on this topic. Power supplies must be stable before SYSCLK is driven.
3. Refer to Section 5, "RESET Initialization" for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for additional information on reset configuration pin setup timing requirements. In addition see Figure 54 regarding HRESET and JTAG connection details including TRST.
5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
6. POR configuration signals must be driven on reset. See Section 5, "RESET Initialization" for more information on setup and hold time of reset configuration signals.
7. The rail for V$_{DD}$_PLAT, AV$_{DD}$_PLAT, V$_{DD}$_Core$n$, AV$_{DD}$_Core$n$, AV$_{DD}$_LB, SV$_{DD}$, XV$_{DD}$_SRDSn,and AV$_{DD}$_SRDSn must reach 90% of its value before the rail for Dn_GV$_{DD}$, and Dn_MV$_{REF}$ reaches 10% of its value.
8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
9. In sleep mode, the reset configuration signals for DRAM types (TSEC2_TXD[4],TSEC2_TX_ER) must be valid BEFORE HRESET is asserted.

Figure 3. MPC8641 Power Up Sequencing

3 Power Characteristics

The estimated power dissipation for the dual core MPC8641D device is shown in Table 4. The (est) listed next to each number is to indicate that the number is based on an estimate.

Table 4. MPC8641D Power Dissipation (Dual Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD}_Coren, V_{DD}_PLAT (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1500 MHz	600 MHz	1.1 V	65 °C	32.1 (est)	1, 2
Thermal				105 °C	43.4 (est)	1, 3
Maximum					49.9 (est)	1, 4
Typical	1333 MHz	533 MHz	1.05 V	65 °C	23.9 (est)	1, 2
Thermal				105 °C	30.0 (est)	1, 3
Maximum					34.1 (est)	1, 4
Typical	1250 MHz	500 MHz	1.05 V	65 °C	23.9 (est)	1, 2
Thermal				105 °C	30.0 (est)	1, 3
Maximum					34.1 (est)	1, 4
Typical	1000 MHz	400 MHz	1.05 V	65 °C	23.9 (est)	1, 2
Thermal				105 °C	30.0 (est)	1, 3
Maximum					34.1 (est)	1, 4

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with one core at 100% efficiency and the second core at 65% efficiency.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on both cores and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on both cores.

The estimated maximum power dissipation for individual power supplies of the MPC8641D is shown in Table 5. The (est) listed next to each number is to indicate that the number is based on an estimate.

Table 5. MPC8641D Individual Supply Maximum Power Dissipation [1]

Component Description	Supply Voltage (Volts)	Power (Watts)	Notes
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.1 V @ 1500 MHz	21.00 (est)	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.1 V @ 1500 MHz	0.13 (est)	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.05 V @ 1333 MHz	17.00 (est)	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.05 V @ 1333 MHz	0.13 (est)	
DDR Controller I/O voltage supply	D*n*_GV_{DD} = 2.5 V @ 400 MHz	0.80 (est)	2
	D*n*_GV_{DD} = 1.8 V @ 533 MHz	0.68 (est)	2
	D*n*_GV_{DD} = 1.8 V @ 600 MHz	0.77 (est)	2
16-bit FIFO @ 200 MHz eTsec 1&2/3&4 Voltage Supply	L/TV_{DD} = 3.3 V	0.11(est)	2, 3
non-FIFO eTsec*n* Voltage Supply	L/TV_{DD} = 3.3 V	0.08 (est)	2
x8 SerDes transceiver Supply	SV_{DD} = 1.1 V	0.70 (est)	2
x8 SerDes I/O Supply	XV_{DD}_SRDS*n* = 1.1 V	0.66 (est)	2
SerDes PLL voltage supply Port 1 or 2	AV_{DD}_SRDS1/AV_{DD}_SRDS2 = 1.1 V	0.10 (est)	
Platform I/O Supply	OV_{DD} = 3.3 V	0.45 (est)	4
Platform source Supply	V_{DD}_PLAT = 1.1 V @ 600 MHz	12.00 (est)	
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 400 MHz	7.70 (est)	
Platform, Local Bus PLL voltage Supply	AV_{DD}_PLAT, AV_{DD}_LB = 1.1 V	0.10 (est)	

Notes:
1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100 % bus utilisation for each component. The components listed are not expected to have 100 % bus usage simultaneously for all components. Actual numbers may vary based on activity.
2. Number is based on a per port/interface value.
3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
4. This includes Local Bus, DUART, JTAG, I^2C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.

The estimated power dissipation for the MPC8641 single core device is shown in Table 6. The (est) listed next to each number is to indicate that the number is based on an estimate.

Table 6. MPC8641 Power Dissipation (Single Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD}_Coren, V_{DD}_PLAT (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1333 MHz	533 MHz	1.05 V	65 °C	16.3 (est)	1, 2
Thermal				105 °C	20.2 (est)	1, 3
Maximum					23.2 (est)	1, 4
Typical	1250 MHz	500 MHz	1.05 V	65 °C	16.3 (est)	1, 2
Thermal				105 °C	20.2 (est)	1, 3
Maximum					23.2 (est)	1, 4
Typical	1000 MHz	400 MHz	1.05 V	65 °C	16.3 (est)	1, 2
Thermal				105 °C	20.2 (est)	1, 3
Maximum					23.2 (est)	1, 4

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.

4 Input Clocks

4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8641.

Table 7. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	150	ps	4, 5

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer toSection 18.2, “MPX to SYSCLK PLL Ratio”, and Section 18.3, “e600 to MPX clock PLL Ratio”, for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator’s cycle-to-cycle output jitter should meet the MPC8641 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8641 is compatible with spread spectrum sources if the recommendations listed in Table 8 are observed.

Table 8. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
1. Guaranteed by design
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30-33kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (MPX clock). The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the MPX clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed..

4.3 eTSEC Gigabit Reference Clock Timing

Table 9 provides the eTSEC gigabit reference clocks (EC_1_GTX_CLK125 and EC_2_GTX_CLK125) AC timing specifications for the MPC8641.

Table 9. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	
EC*n*_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications" for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8641. Table 11 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	
Minimum assertion time for $\overline{\text{SRESET}}$_0 & $\overline{\text{SRESET}}$ 1	512	—	SYSCLKs	1
Platform PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	2
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:

1. SYSCLK is the primary clock input for the MPC8641.

2 This is related to $\overline{\text{HRESET}}$ assertion time.

Table 11 provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
(Platform and E600) PLL lock times	—	100	µs	1
Local bus PLL	—	50	µs	

Notes:

1. The PLL lock time for e600 PLL requires an additional 255 MPX-Clock cycles.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8641. Note that DDR SDRAM is D*n*_GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is D*n*_GV_{DD}(typ) = 1.8 V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8641 when D*n*_GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	1.7	1.9	V	1
I/O reference voltage	D*n*_MV_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	D*n*_MV_{REF} – 0.04	D*n*_MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	D*n*_MV_{REF}+ 0.125	D*n*_GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	D*n*_MV_{REF} – 0.125	V	
Output leakage current	I_{OZ}	–9.9	9.9	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. D*n*_MV_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_MV_{REF}. This rail should track variations in the DC level of D*n*_MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 13 provides the DDR capacitance when D*n*_GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for D*n*_GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = D*n*_GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when D*n*_GV_{DD}(typ) = 2.5 V.

Table 14. DDR SDRAM DC Electrical Characteristics for D*n*_GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	2.375	2.675	V	1
I/O reference voltage	D*n*_MV_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	D*n*_MV_{REF} – 0.04	D*n*_MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	D*n*_MV_{REF} + 0.15	D*n*_GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	D*n*_MV_{REF}– 0.15	V	
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_MV_{REF}. This rail should track variations in the DC level of D*n*_MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 15 provides the DDR capacitance when D*n*_GV_{DD} (typ)=2.5 V.

Table 15. DDR SDRAM Capacitance for D*n*_GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = D*n*_GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR SDRAM when D*n*_GV_{DD}(typ)=1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	D*n*_MV_{REF} – 0.25	V	
AC input high voltage	V_{IH}	D*n*_MV_{REF} + 0.25	—	V	

Table 18 provides the input AC timing specifications for the DDR SDRAM when D*n*_GV_{DD}(typ)=2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	D*n*_MV_{REF} – 0.31	V	
AC input high voltage	V_{IH}	D*n*_MV_{REF} + 0.31	—	V	

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
600 MHz		–240	240		3
533 MHz		–300	300		3
400 MHz		–365	365		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: t_{DISKEW} =+/-(T/4 - abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Maximum DDR1 frequency is 400 MHz.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 20. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
600 MHz		450	—		7
533 MHz		538	—		7
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
600 MHz		450	—		7
533 MHz		538	—		7
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 20. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8641 Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz

NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

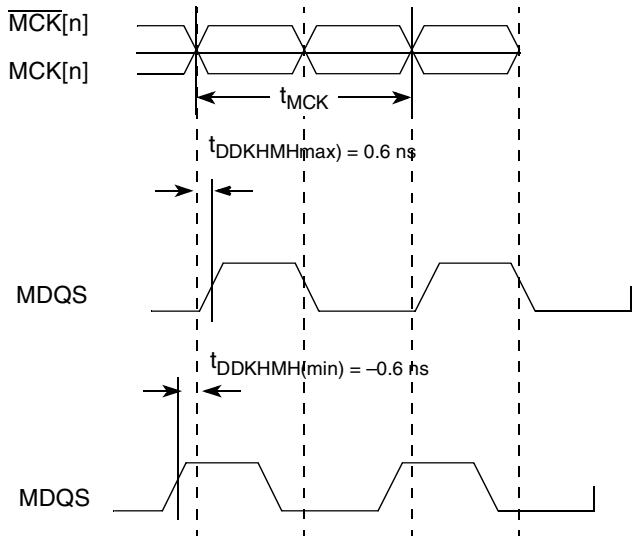


Figure 4. Timing Diagram for tDDKHMH

Figure 5 shows the DDR SDRAM output timing diagram.

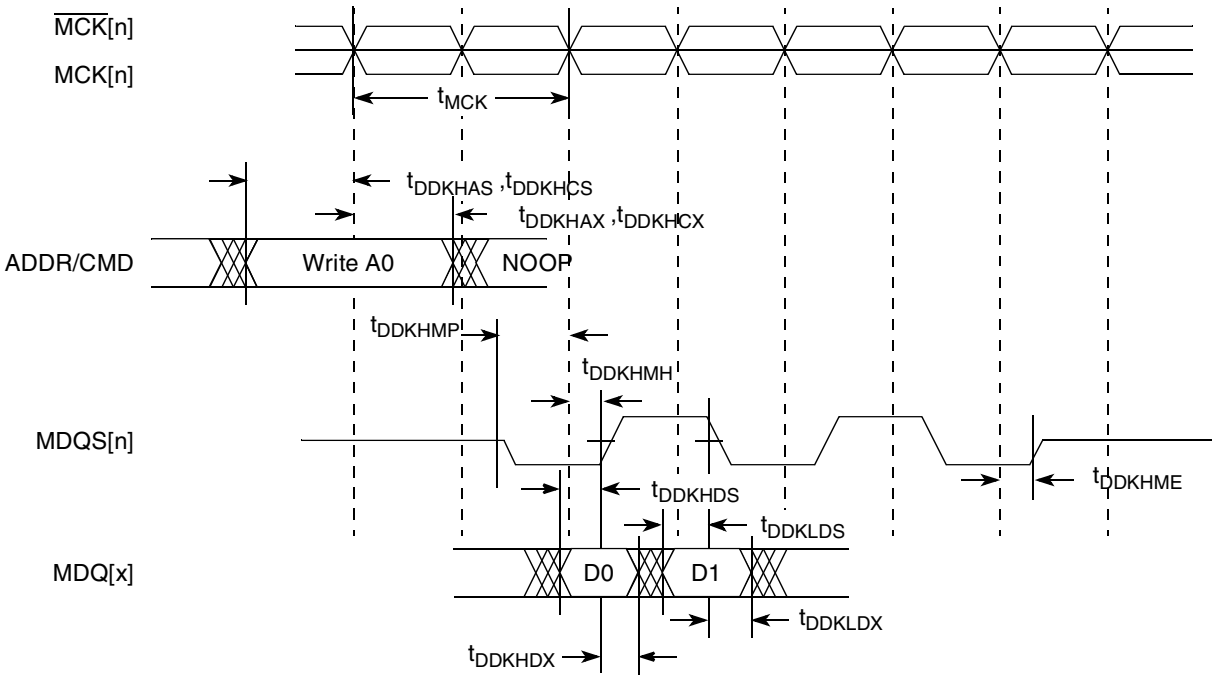


Figure 5. DDR SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

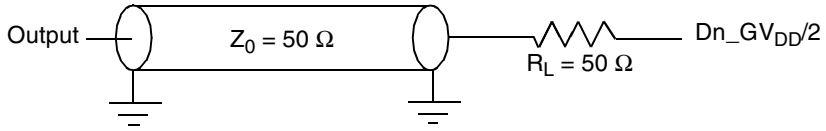


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8641.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table and Table 2.

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	MPX clock/1,048,576	baud	1,2
Maximum baud rate	MPX clock/16	baud	1,3
Oversample rate	16	—	1,4

Notes:

1. Guaranteed by design
2. MPX clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical Characteristics.”

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver’s power supply (i.e., a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –4.0 mA)	VOH	2.40	LV_{DD}/TV_{DD} + 0.3	V	
Output low voltage (LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)	VOL	GND	0.50	V	
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	0.90	V	

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4.
3 The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table and Table 2.

Table 24. GMII, MII, RMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.675	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	0.70	V	
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Note:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4.
3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like

FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 18.4.2, "Platform to FIFO restrictions"

A summary of the FIFO AC specifications appears in Table 25 and Table 26.

Table 25. FIFO Mode Transmit AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Input low voltage @ 2.5 OV_{DD}	V_{IL}	—	—	0.7	V
Input high voltage @ 2.5 OV_{DD}	V_{IH}	1.9	—	—	V
TX_CLK, GTX_CLK clock period	t_{FIT}	5.0	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns

Table 26. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Input low voltage @ 2.5 OV_{DD}	V_{IL}	—	—	0.7	V
Input high voltage @ 2.5 OV_{DD}	V_{IH}	1.9	—	—	V
RX_CLK clock period	t_{FIR}	5.0	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

Timing diagrams for FIFO appear in Figure 7 and Figure 8.

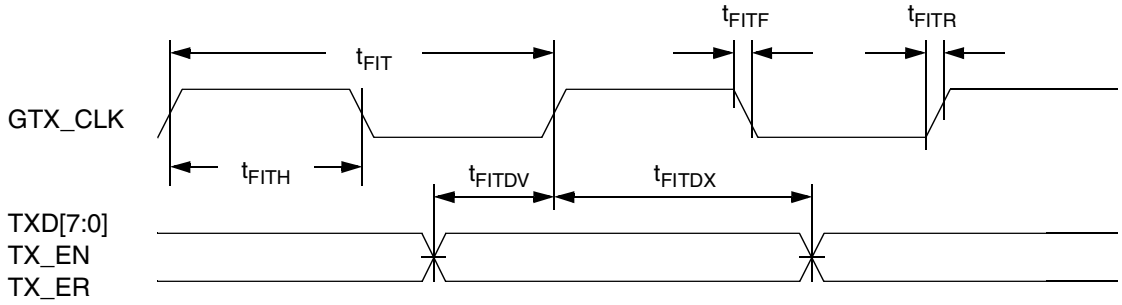


Figure 7. FIFO Transmit AC Timing Diagram

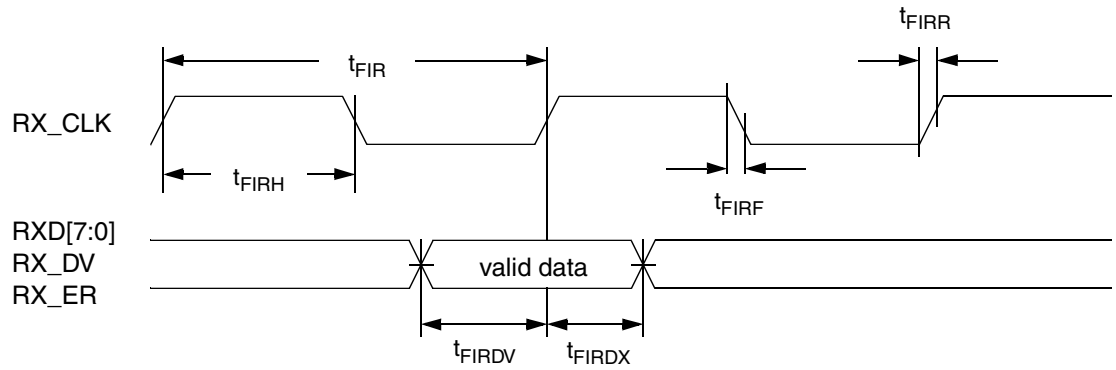


Figure 8. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

Table 27 provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage	VIL	—	—	0.7	V
Input high voltage	VIH	1.9	—	—	V
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR} [2]	—	—	1.0	ns

Table 27. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design

Figure 9 shows the GMII transmit AC timing diagram.

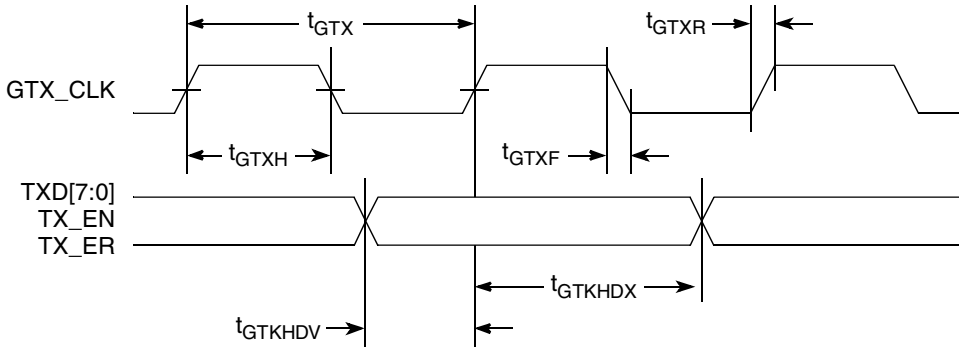


Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage	VIL	—	—	0.7	V
Input high voltage	VIH	1.9	—	—	V
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}[2]	—	—	1.0	ns

Table 28. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design

Figure 10 provides the AC test load for eTSEC.

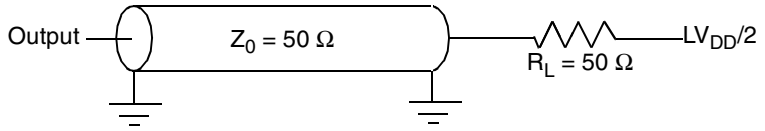


Figure 10. eTSEC AC Test Load

Figure 11 shows the GMII receive AC timing diagram.

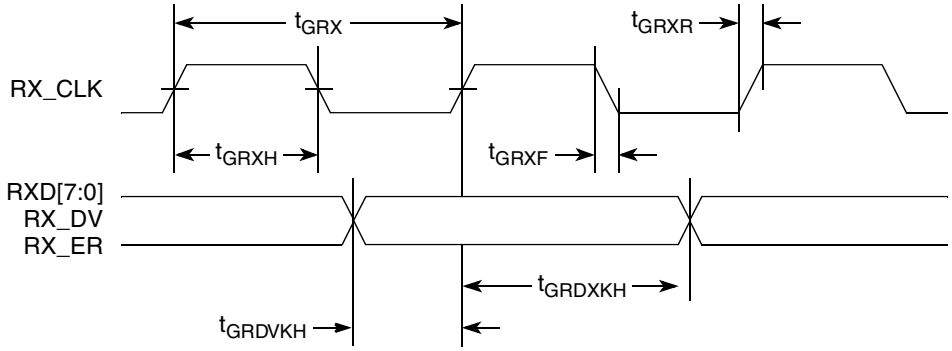


Figure 11. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage	VIL	—	—	0.7	V
Input high voltage	VIH	1.9	—	—	V
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}[2]	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}[2]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 shows the MII transmit AC timing diagram.

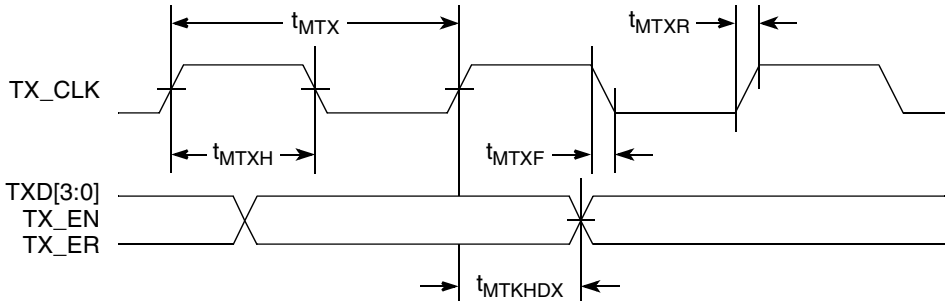


Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage	VIL	—	—	0.7	V
Input high voltage	VIH	1.9	—	—	V
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}[2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}[2]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

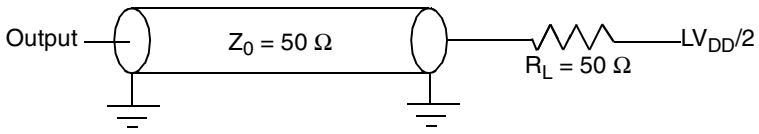


Figure 13. eTSEC AC Test Load

Figure 14 shows the MII receive AC timing diagram.

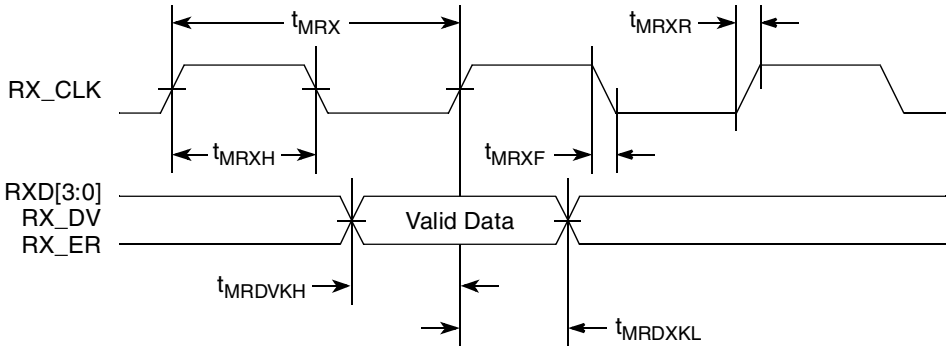


Figure 14. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 31 provides the TBI transmit AC timing specifications.

Table 31. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}[3]	1.0	—	—	ns
GTX_CLK rise (20%–80%)	t_{TTXR}[2]	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. In rev 1.0 silicon, due to errata, t_{TTKHDX} is 600 ps. Please refer to “eTSEC 13” in the device errata document.

Figure 15 shows the TBI transmit AC timing diagram.

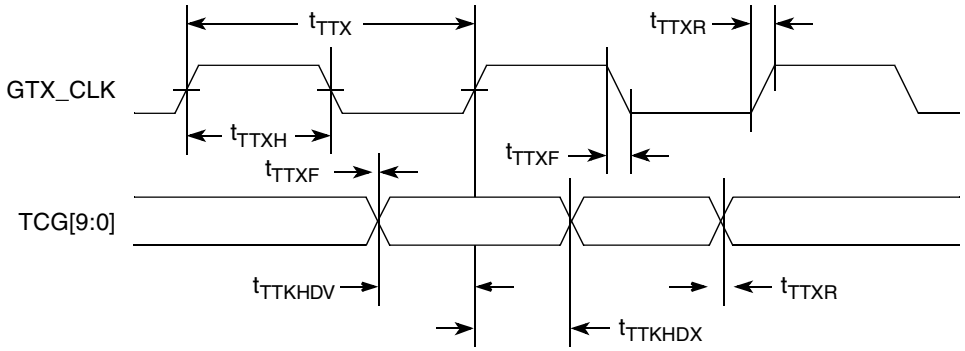


Figure 15. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 32 provides the TBI receive AC timing specifications.

Table 32. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}		16.0		ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR}[2]	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF}[2]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.

Figure 16 shows the TBI receive AC timing diagram.

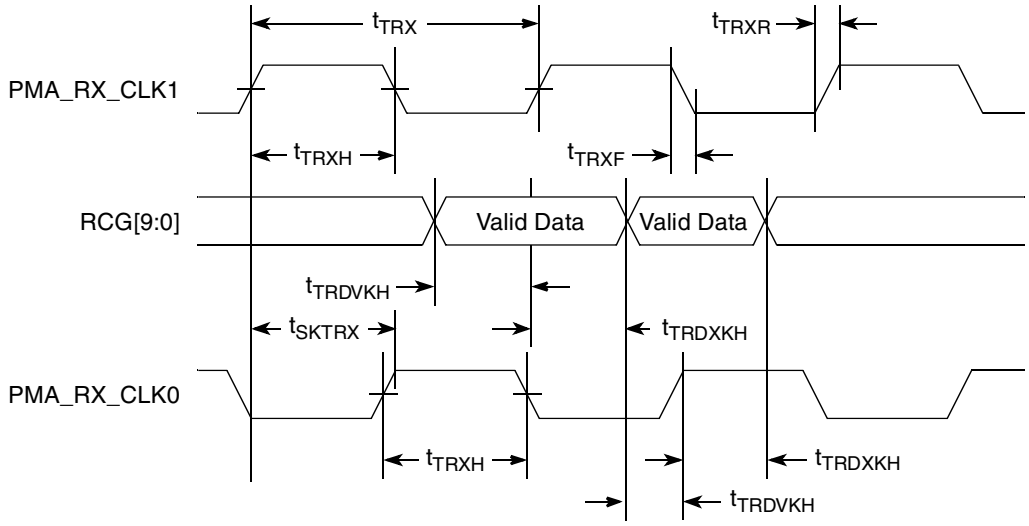


Figure 16. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSEC*n* pin (no receive clock is used on in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Input low voltage @ 3.3 OV_{DD}	V_{IL}	—	—	0.7	V
Input high voltage @ 3.3 OV_{DD}	V_{IH}	1.9	—	—	V
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns

A timing diagram for TBI receive appears in Figure 17.

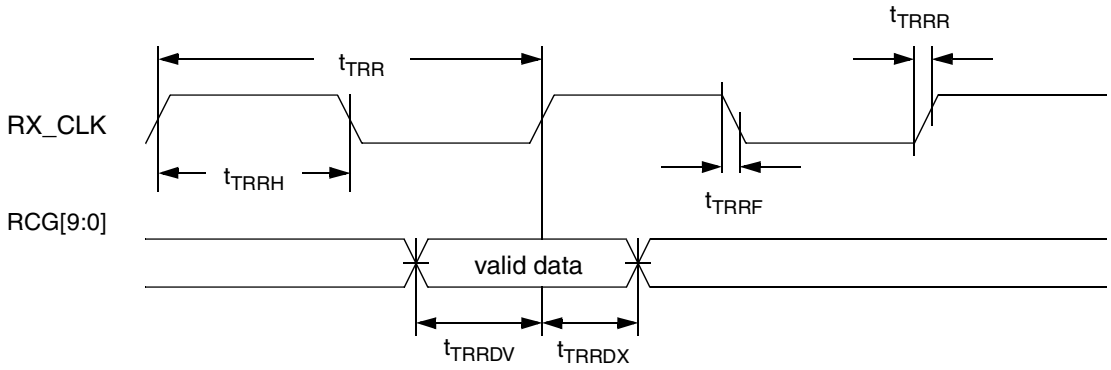


Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	–500[6]	0	500[6]	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period duration [3]	t_{RGT}[5]	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}[5]	40	50	60	%
Rise time (20%–80%)	t_{RGTR}[5]	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}[5]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization
6. In rev 1.0 silicon, due to errata, t_{SKRGT} is -650 ps (Min) and 650 ps (Max). Please refer to “eTSEC 10” in the device errata document.

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

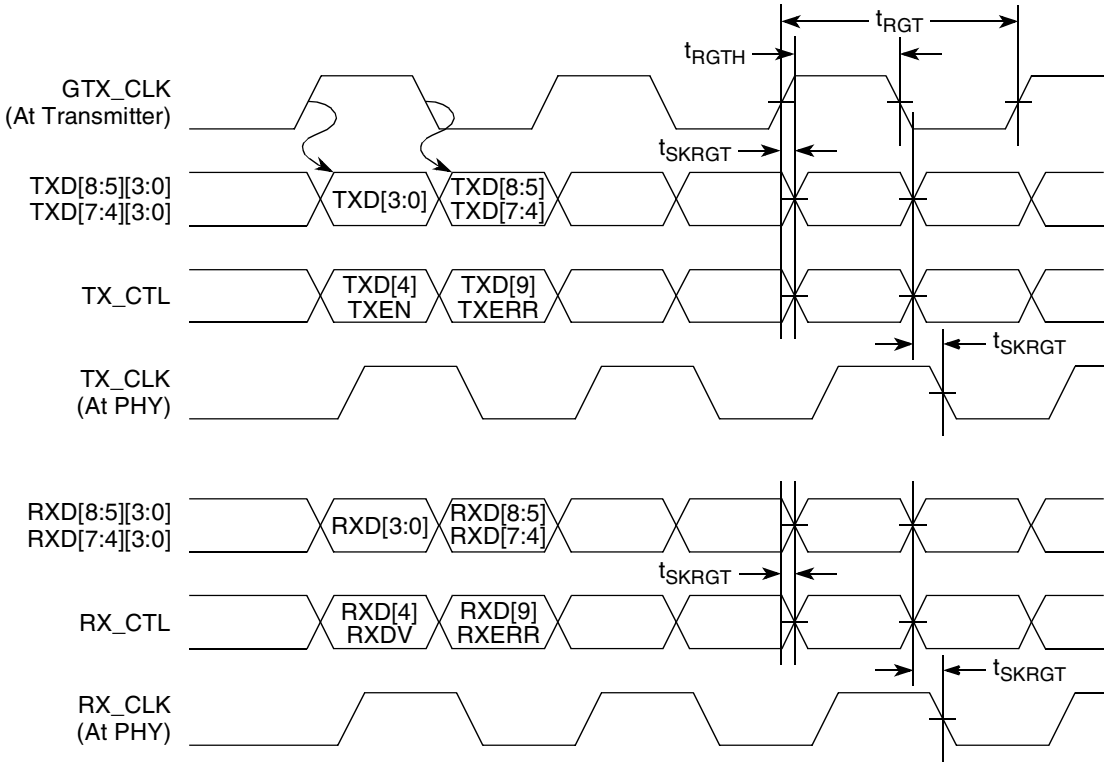


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 35.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage @ 3.3 OV_{DD}	V_{IL}	—	—	0.8	V
Input high voltage @ 3.3 OV_{DD}	V_{IH}	2.0	—	—	V
REF_CLK clock period	t_{RMT}		20.0		ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns

Table 35. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 shows the RMII transmit AC timing diagram.

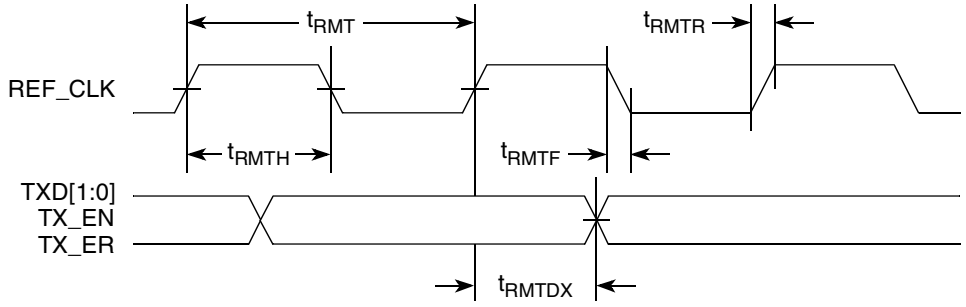


Figure 19. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 36. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage @ 3.3 OV_{DD}	V_{IL}	—	—	0.8	V
Input high voltage @ 3.3 OV_{DD}	V_{IH}	2.0	—	—	V
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns

Table 36. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 20 provides the AC test load for eTSEC.

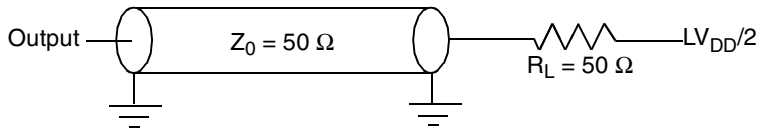


Figure 20. eTSEC AC Test Load

Figure 21 shows the RMII receive AC timing diagram.

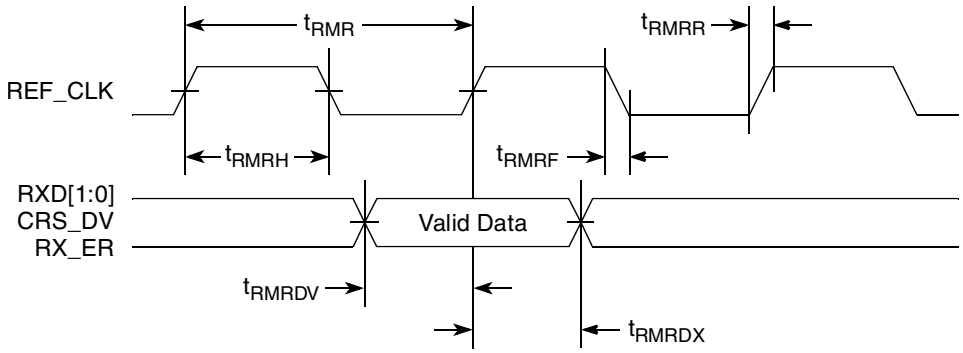


Figure 21. RMII Receive AC Timing Diagram

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 37.

Table 37. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.135	3.465	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	µA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	µA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table and Table 2.

9.2 MII Management AC Electrical Specifications

Table 38 provides the MII management AC timing specifications.

Table 38. MII Management AC Timing Specifications

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	2.5	—	9.3	MHz	2, 4
MDC period	t_{MDC}	80	—	400	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO valid	t_{MDKHDV}	$2*(t_{MPXCLK}*8)$			ns	5
MDC to MDIO delay	t_{MDKHDX}	10	—	$2*(t_{MPX}*8)$	ns	3, 5

Table 38. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	4
MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
4. Guaranteed by design
5. t_{MPXCLK} is the platform (MPX) clock

Figure 22 shows the MII management AC timing diagram.

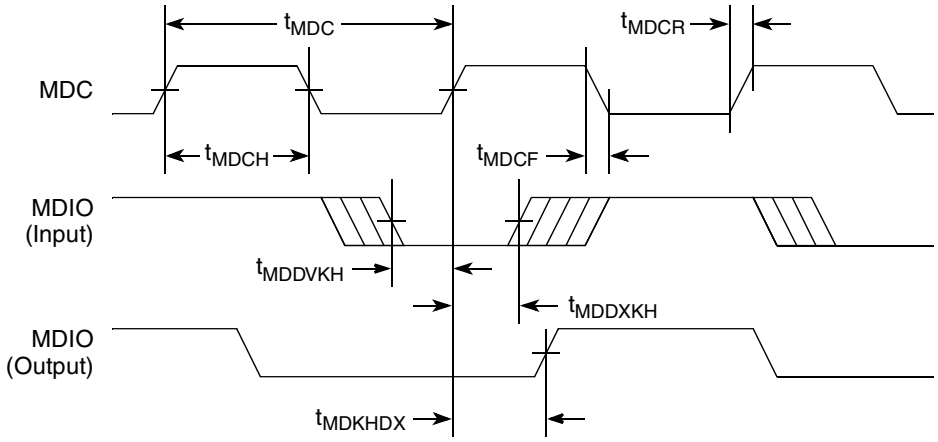


Figure 22. MII Management Interface Timing Diagram

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8641.

10.1 Local Bus DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the local bus interface operating at OV_{DD} = 3.3 V DC.

Table 39. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (OV_{IN} [1] = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:

1. Note that the symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table and Table 2.

10.2 .Local Bus AC Electrical Specifications

Table 40 describes the general timing parameters of the local bus interface at OV_{DD} = 3.3 V DC. For information about the frequency range of local bus see Section 18.1, “Clock Ranges.”

Table 40. Local Bus General Timing Parameters (OV_{DD} = 3.3 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)		t_{LBOTOT}	1.0	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)		$t_{LBKHOV1}$	—	2.0	ns	

Table 40. Local Bus General Timing Parameters (OV_{DD} = 3.3 V DC) (continued)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP		$t_{LBKHOV2}$	—	2.2	ns	
Local bus clock to address valid for LAD		$t_{LBKHOV3}$	—	2.3	ns	
Output hold from local bus clock (except LAD/LDP and LALE)		$t_{LBKHOX1}$	0.7	—	ns	
Output hold from local bus clock for LAD/LDP		$t_{LBKHOX2}$	0.7	—	ns	
Local bus clock to output high Impedance (except LAD/LDP and LALE)		$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP		$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD.

Figure 23 provides the AC test load for the local bus.

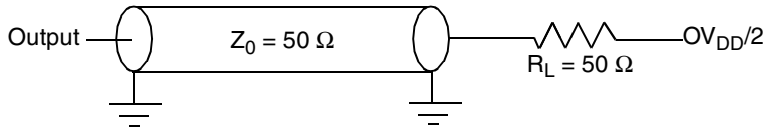
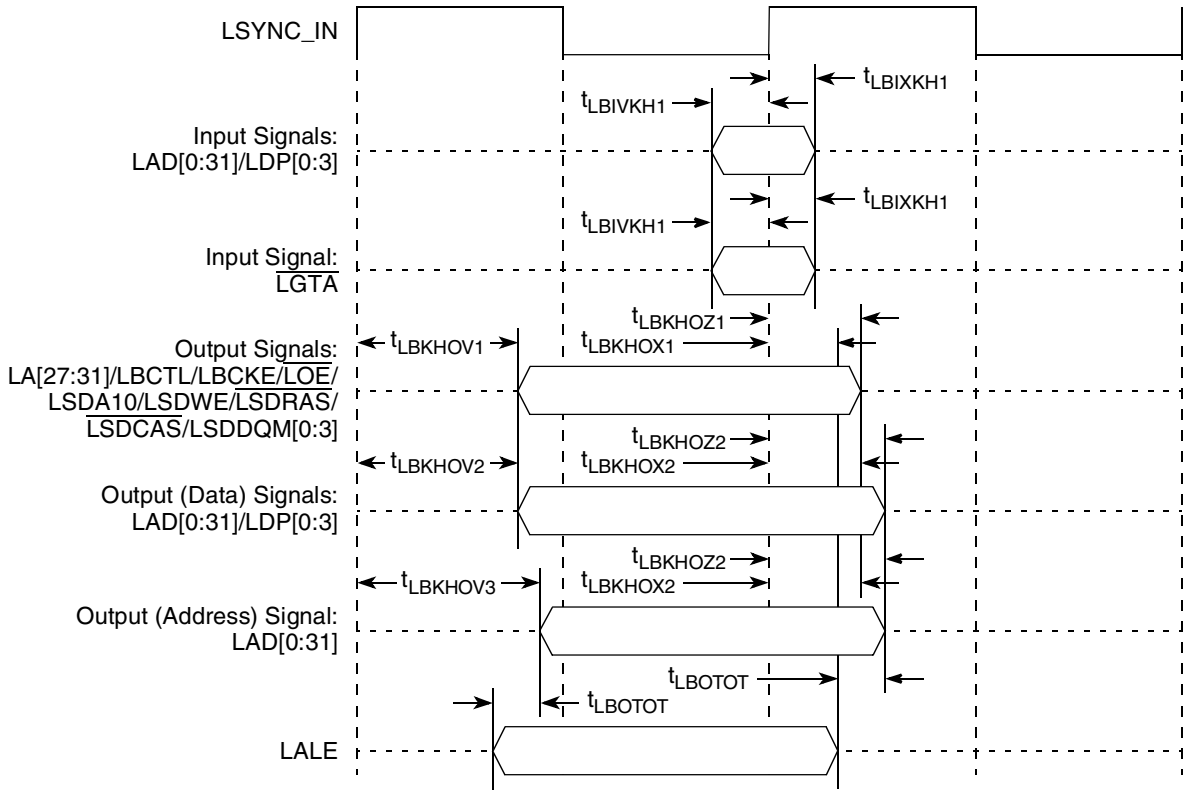


Figure 23. Local Bus AC Test Load

NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 Mhz, LBIU PLL is recommended to be enabled.

Figure 24 to Figure 29 show the local bus signals.



Note: t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. Only the falling edge of LALE matters with respect to the specification.

Figure 24. Local Bus Signals, Non-Special Signals Only (PLL Enabled)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT}. In this mode, signals are latched at the raising edge of the internal clock and are captured at falling edge of the internal clock.

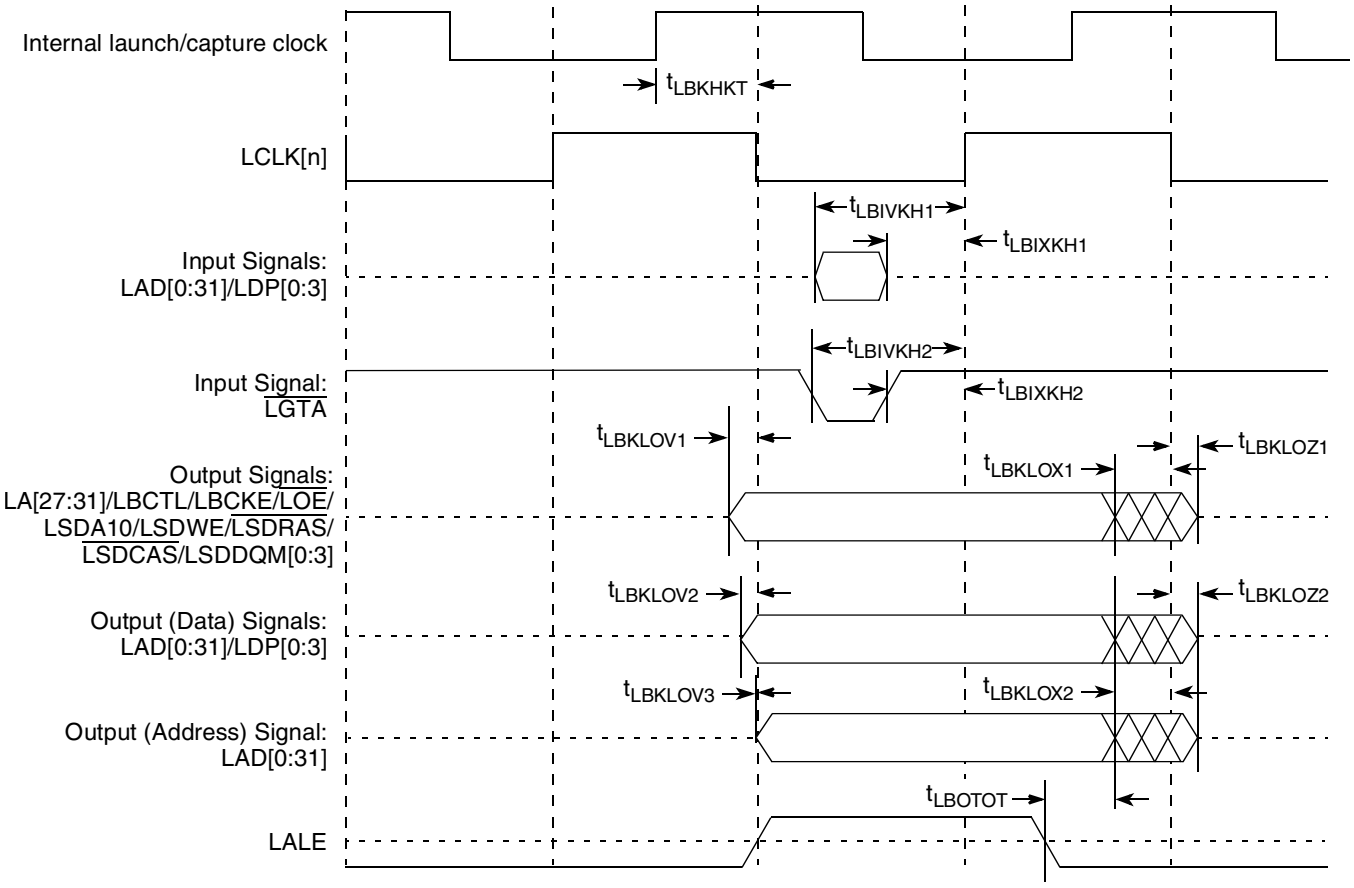


Figure 25. Local Bus Signals (PLL Bypass Mode)

Table 41 describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Table 41. Local Bus General Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	6.0	—	ns	2
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	t_{LBKHKT}(min)	t_{LBKHKT}(max)	ns	8
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.8+t_{LBKHKT}(max)	—	ns	4, 5
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7+t_{LBKHKT}(max)	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	0.5-t_{LBKHKT}(min)	—	ns	4, 5
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0-t_{LBKHKT}(min)	—	ns	4, 5

Table 41. Local Bus General Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	2.0-t_{LBKHKT}(min)	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	2.2-t_{LBKHKT}(min)	ns	4
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	2.3-t_{LBKHKT}(min)	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	0.7-t_{LBKHKT}(max)	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	0.7-t_{LBKHKT}(max)	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	2.5-t_{LBKHKT}(min)	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	2.5-t_{LBKHKT}(min)	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which preceeds LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

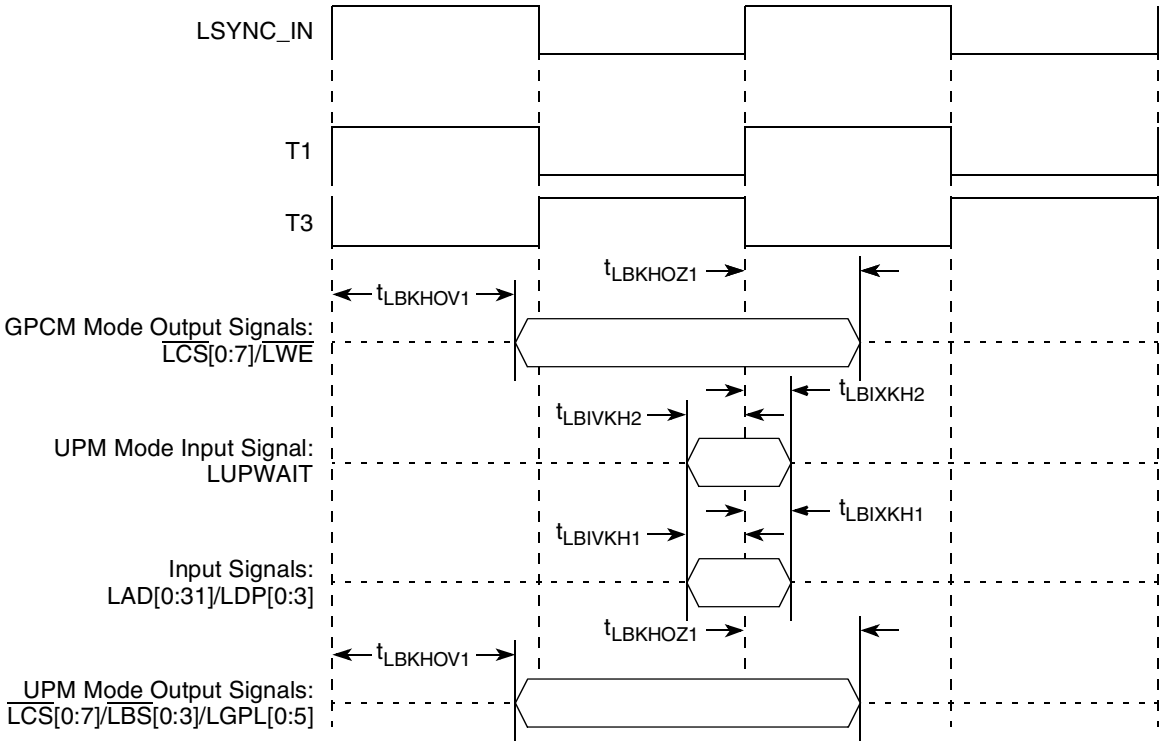


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (PLL Enabled)

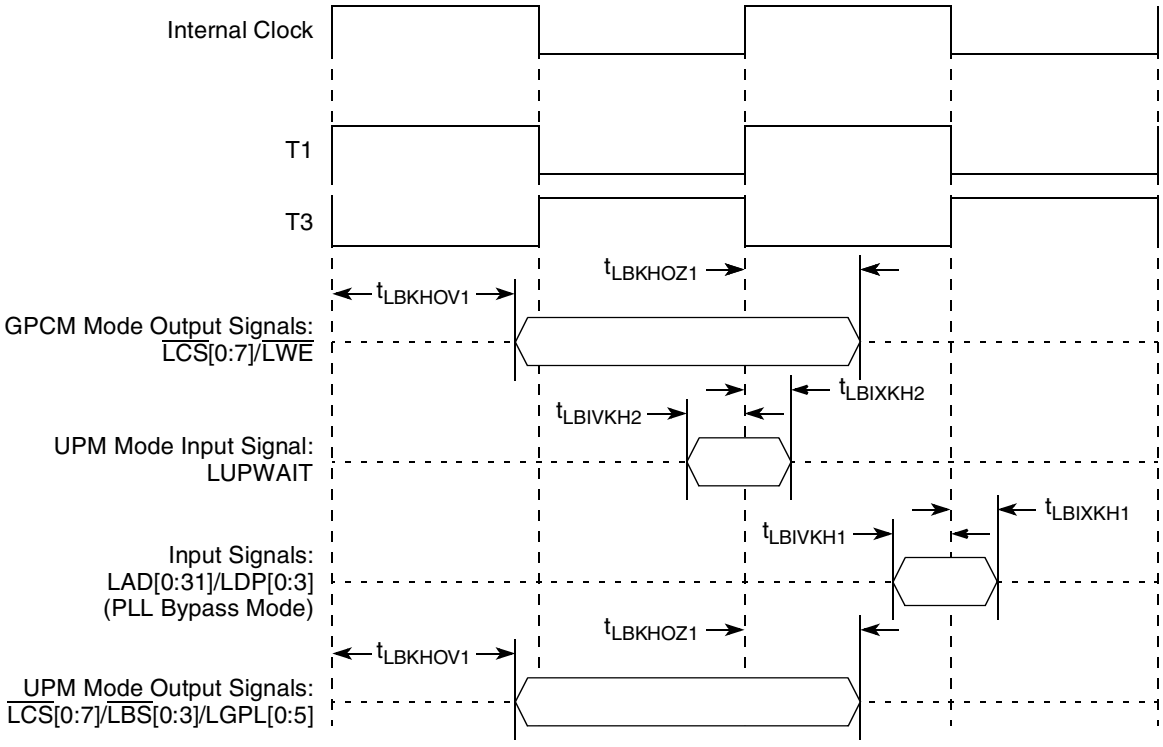


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (PLL Bypass Mode)

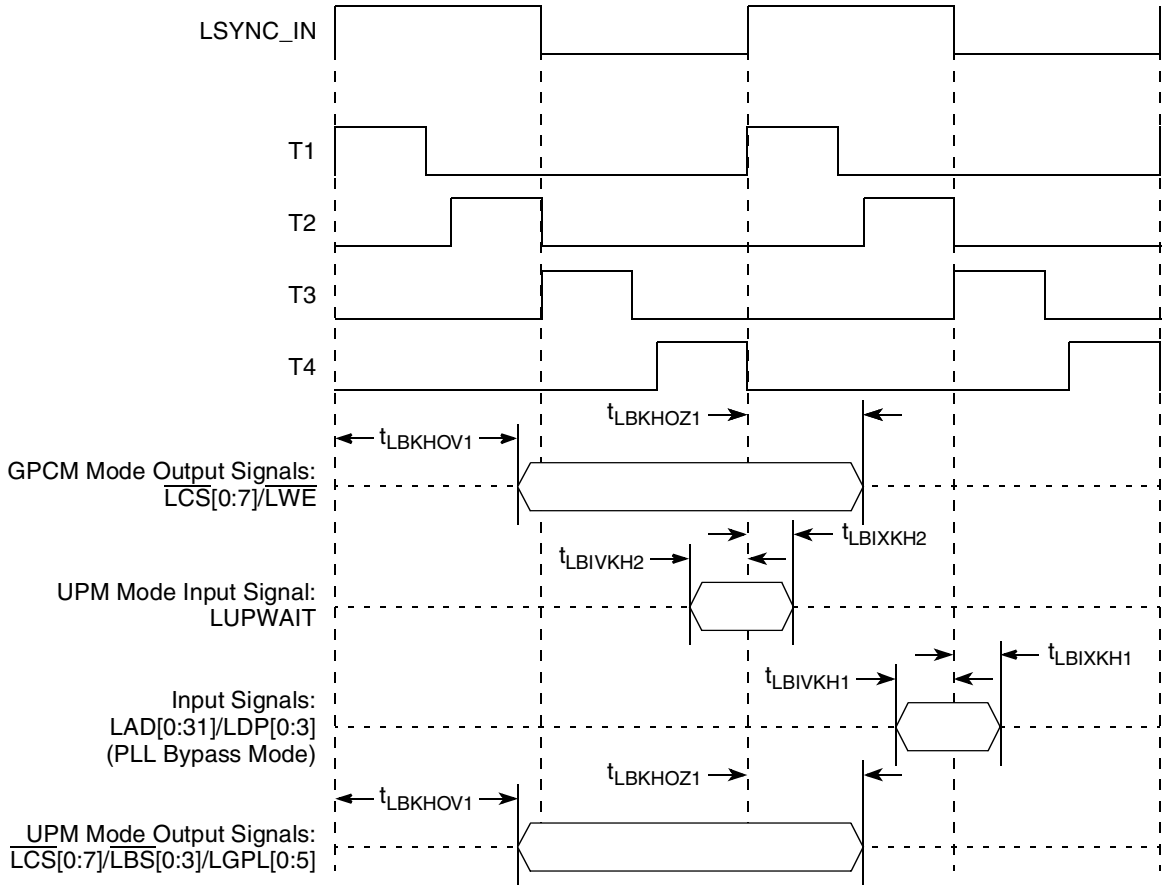


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

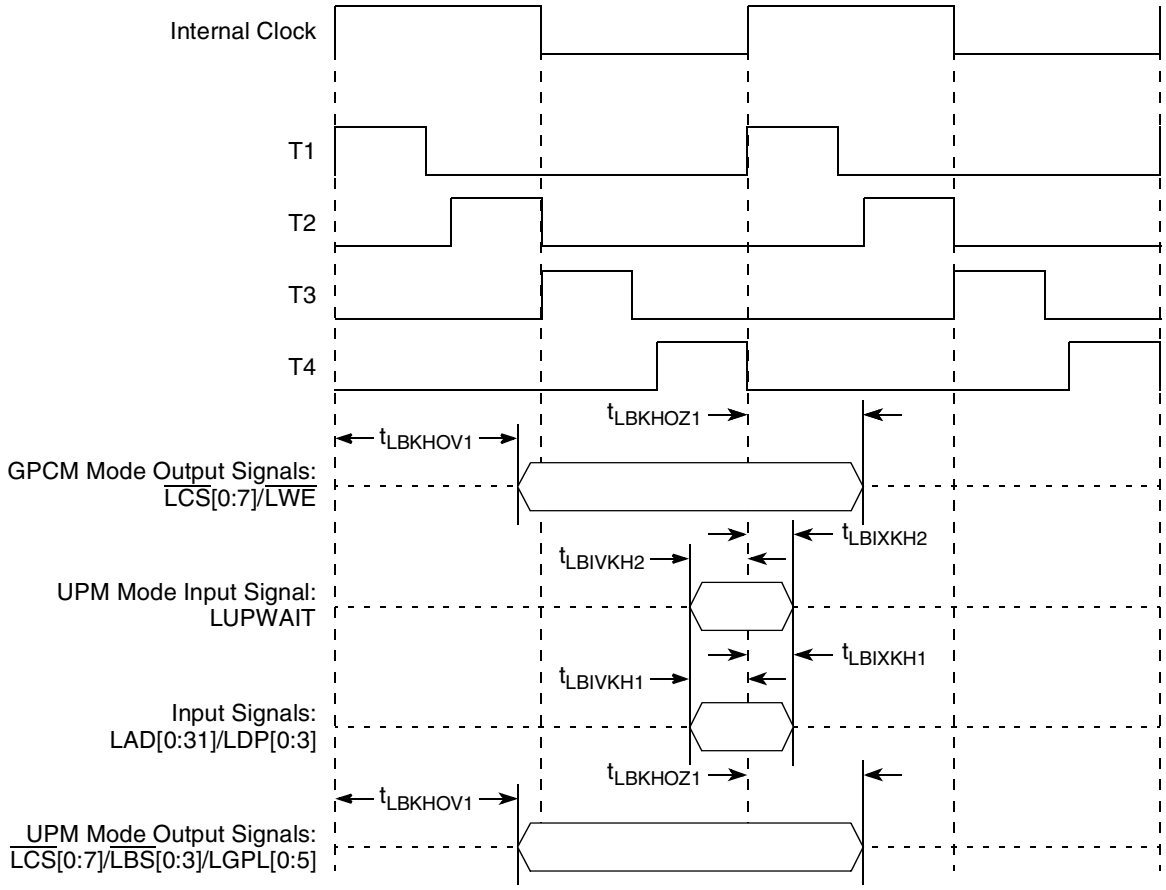


Figure 29. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

11 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8641.

Table 42 provides the JTAG AC timing specifications as defined in Figure 31 through Figure 33.

Table 42. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 30). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design

Figure 30 provides the AC test load for TDO and the boundary-scan outputs.

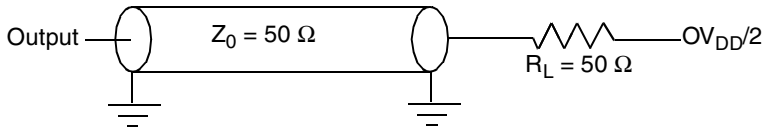


Figure 30. AC Test Load for the JTAG Interface

Figure 31 provides the JTAG clock input timing diagram.

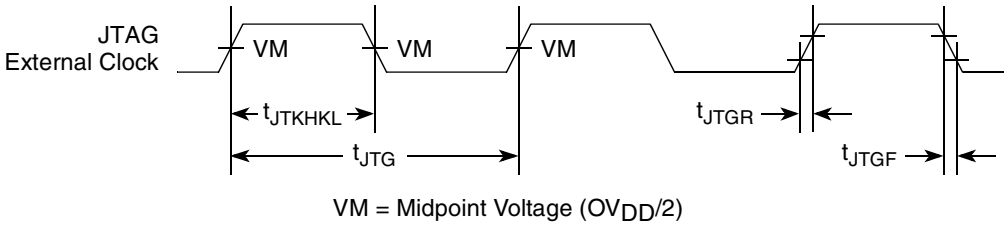


Figure 31. JTAG Clock Input Timing Diagram

Figure 32 provides the $\overline{\text{TRST}}$ timing diagram.

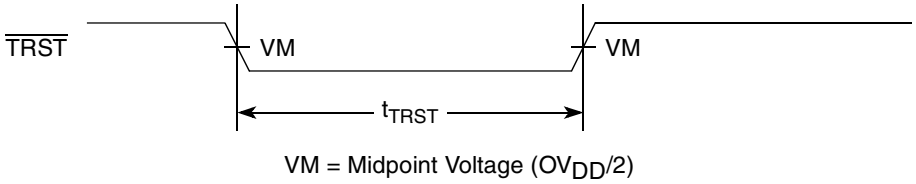


Figure 32. $\overline{\text{TRST}}$ Timing Diagram

Figure 33 provides the boundary-scan timing diagram.

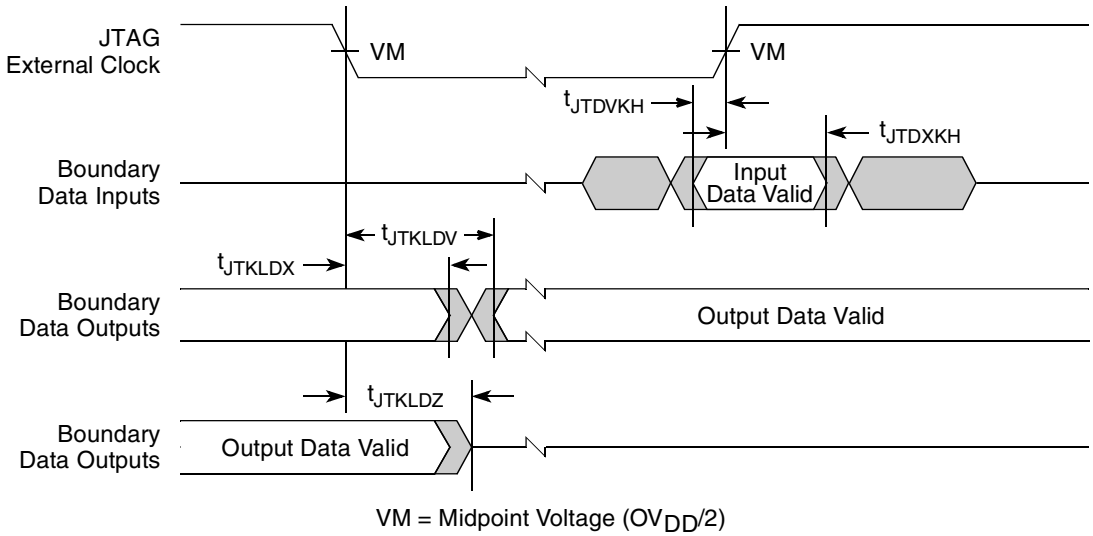


Figure 33. Boundary-Scan Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8641.

12.1 I²C DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the I²C interfaces.

Table 43. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8641 Integrated Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 44 provides the AC timing parameters for the I²C interfaces.

Table 44. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [5]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [5]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [5]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [5]	0.6	—	µs
Data setup time	t_{I2DVKH} [5]	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	µs
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs

Table 44. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol [1]	Min	Max	Unit
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8641 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. Guaranteed by design

Figure 34 provides the AC test load for the I²C.

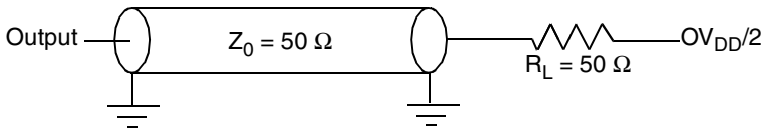


Figure 34. I²C AC Test Load

Figure 35 shows the AC timing diagram for the I²C bus.

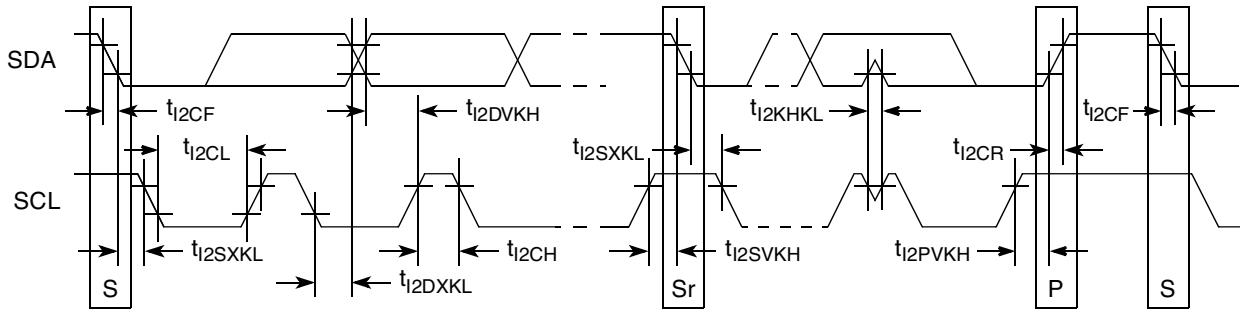


Figure 35. I²C Bus AC Timing Diagram

13 High-Speed Interfaces

This section describes the common DC electrical specifications for the interface (Serial RapidIO, and PCI Express) of the MPC8641.

13.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks are SD_1_REF_CLK, $\overline{\text{SD\_1\_REF\_CLK}}$, SD_2_REF_CLK and $\overline{\text{SD\_2\_REF\_CLK}}$.

- Recommended minimum operating voltage is –0.4 V; recommended maximum operating voltage is 1.32 V; Maximum absolute voltage is 1.72 V.
- Each differential clock input has a 50-Ω termination to GND. The reference clock must be able to drive this termination. The input is AC-coupled on chip following the termination.
- The amplitude of the clock must be at least a 400-mV differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive ±100 mV around common mode voltage.
- The differential reference clock (SD_*n*_REF_CLK/$\overline{\text{SD\_}n\text{\_REF\_CLK}}$) input is HCSL compatible DC coupled or LVDS compatible with AC coupling.

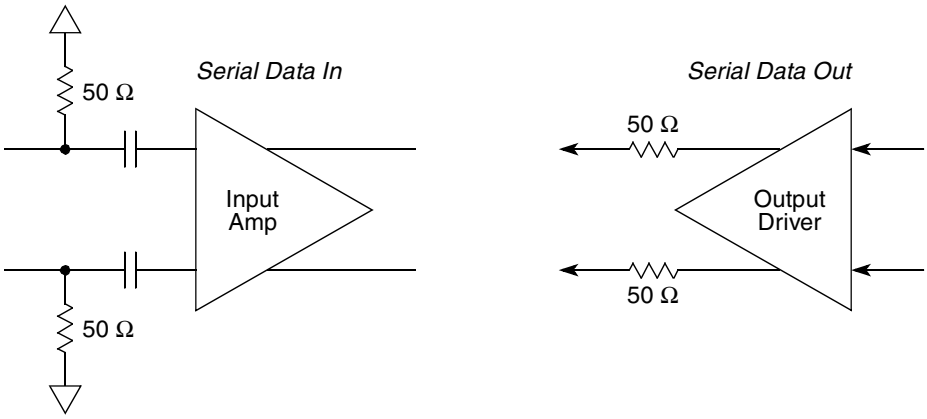


Figure 36. Driver and Receiver of SerDes (PCI Express, Serial RapidIO, and SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$

14 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8641.

14.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 13.1, "DC Requirements for SerDes Reference Clocks."

14.2 AC Requirements for PCI Express SerDes Clocks

Table 45 lists AC requirements.

Table 45. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	-	10	-	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—
Notes: 1. Typical based on PCI Express Specification 2.0.						

14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million 15 (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

14.4.1 Differential Transmitter (TX) Output

Table 46 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 46. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.8		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 2.
$V_{TX-DE-RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX Eye Width	0.70			UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125			UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage			20	mV	$V_{TX-CM-ACp} = RMS(\|V_{TXD+} - V_{TXD-}\|/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During LO and Electrical Idle	0		100	mV	$\|V_{TX-CM-DC\ (during\ LO)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\| <= 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [LO] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0		25	mV	$\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\| <= 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\|V_{TX-D-}\|$ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0		20	mV	$V_{TX-IDLE-DIFFp} = \|V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\| <= 20$ mV See Note 2.

Table 46. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX\text{-}RCV\text{-}DETECT}$	The amount of voltage change allowed during Receiver Detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX\text{-}DC\text{-}CM}$	The TX DC Common Mode Voltage	0		3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX\text{-}SHORT}$	TX Short Circuit Current Limit			90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in Electrical Idle	50			UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set			20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from LO.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX\text{-}DIFF}$	Differential Return Loss	12			dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$RL_{TX\text{-}CM}$	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
$Z_{TX\text{-}DC}$	Transmitter DC Impedance	40			Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX\text{-}SKEW}$	Lane-to-Lane Output Skew			500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75		200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Table 46. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{crosslink}$	Crosslink Random Timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1.) No test load is necessarily associated with this value.

2.) Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 39 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 37)

3.) A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4.) The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 39). Note that the series capacitors C_{TX} is optional for the return loss measurement.

5.) Measured between 20-80% at transmitter package pins into a test load as shown in Figure 39 for both V_{TX-D+} and V_{TX-D-}.

6.) See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a

7.) See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a

14.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 37 is specified using the passive compliance/test measurement load (see Figure 39) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

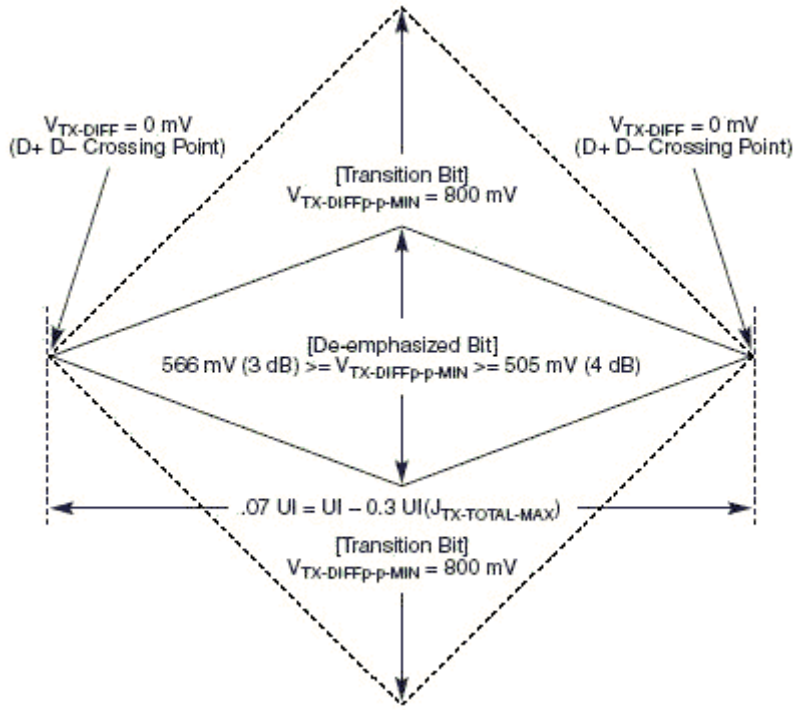


Figure 37. Minimum Transmitter Timing and Voltage Output Compliance Specifications

14.4.3 Differential Receiver (RX) Input Specifications

Table 47 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 47. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 2.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4			UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 2 and 3.

Table 47. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k			Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 47. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1.) No test load is necessarily associated with this value.

2.) Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 39 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 38). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3.) A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4.) The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 39). Note: that the series capacitors CTX is optional for the return loss measurement.

5.) Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.

6.) The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

7.) It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 38 is specified using the passive compliance/test measurement load (see Figure 39) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 39) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 38) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50. probes—see Figure 39). Note that the series capacitors, CTX, are optional for the return loss measurement.

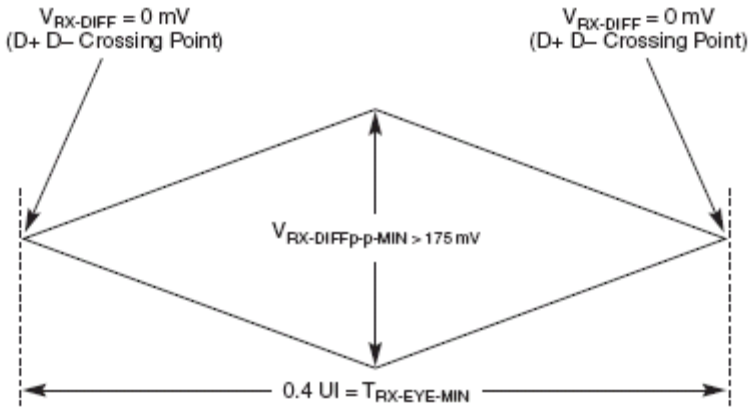


Figure 38. Minimum Receiver Eye Timing and Voltage Compliance Specification

14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 39.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

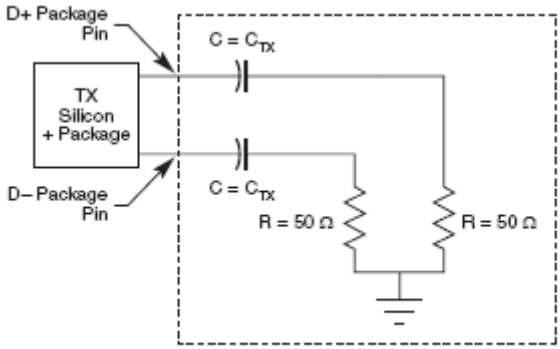


Figure 39. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8641, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

For more information, see Section 13.1, “DC Requirements for SerDes Reference Clocks.”

15.2 AC Requirements for Serial RapidIO SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	8	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	

15.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 40 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between A Volts and B Volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD and $\overline{RD}$ each have a peak-to-peak swing of A - B Volts
2. The differential output signal of the transmitter, V_{OD}, is defined as V_{TD}-$V_{\overline{TD}}$
3. The differential input signal of the receiver, V_{ID}, is defined as V_{RD}-$V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) Volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A - B Volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 * (A - B) Volts

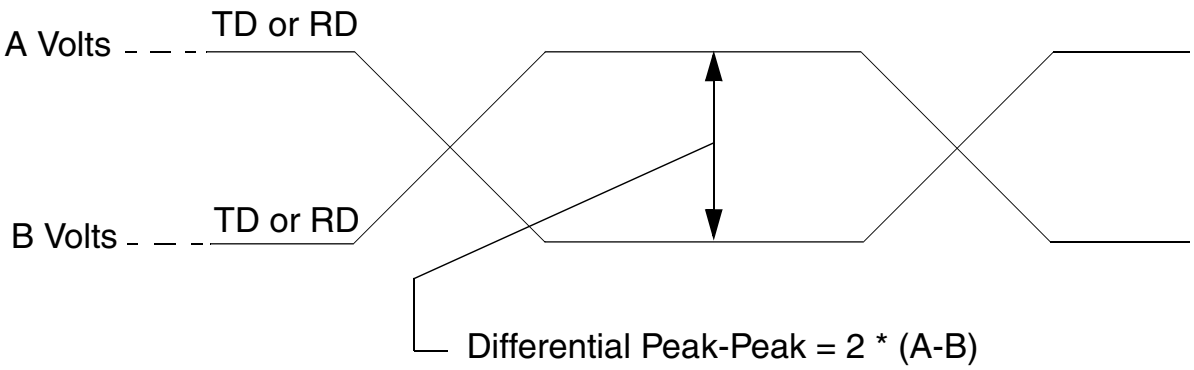


Figure 40. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

15.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 49. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 50. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple Output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 51. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	

Table 51. Short Run Transmitter AC Timing Specifications—3.125 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

Table 52. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/- 100 ppm

Table 53. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/- 100 ppm

Table 54. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 41 with the parameters specified in Table 55 when measured at the output pins of the device and the device is driving a 100 Ohm +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

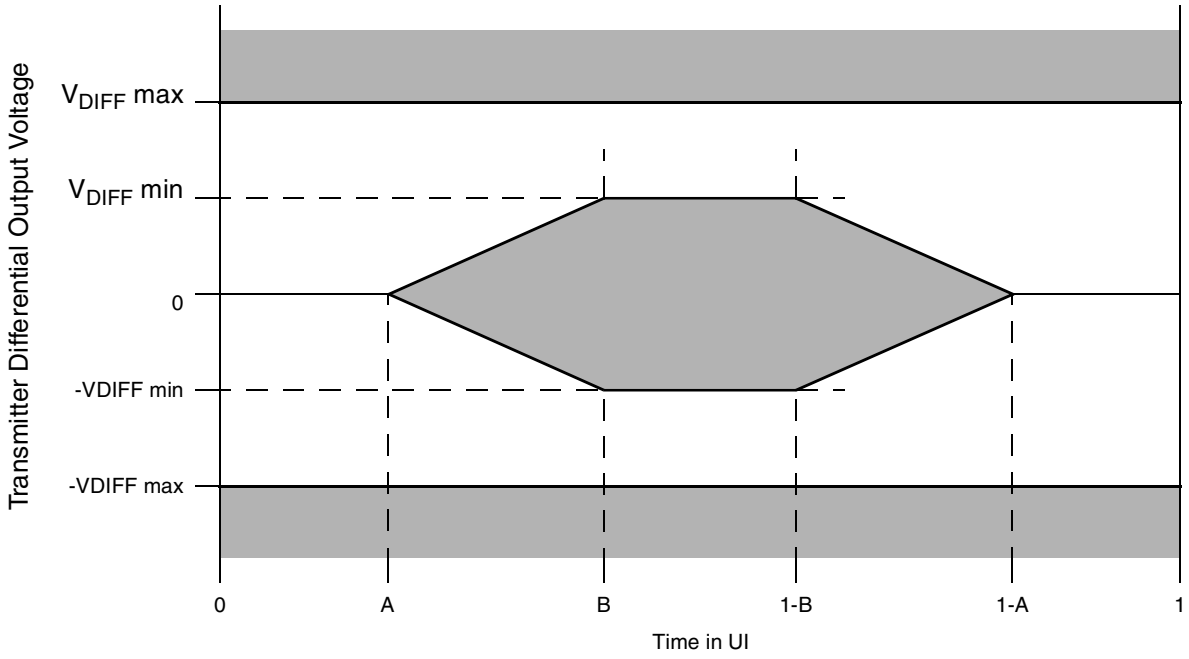


Figure 41. Transmitter Output Compliance Mask

Table 55. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

Table 56. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	800	800	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 57. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	400	400	ps	+/– 100 ppm

Note:
1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 58. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:
1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

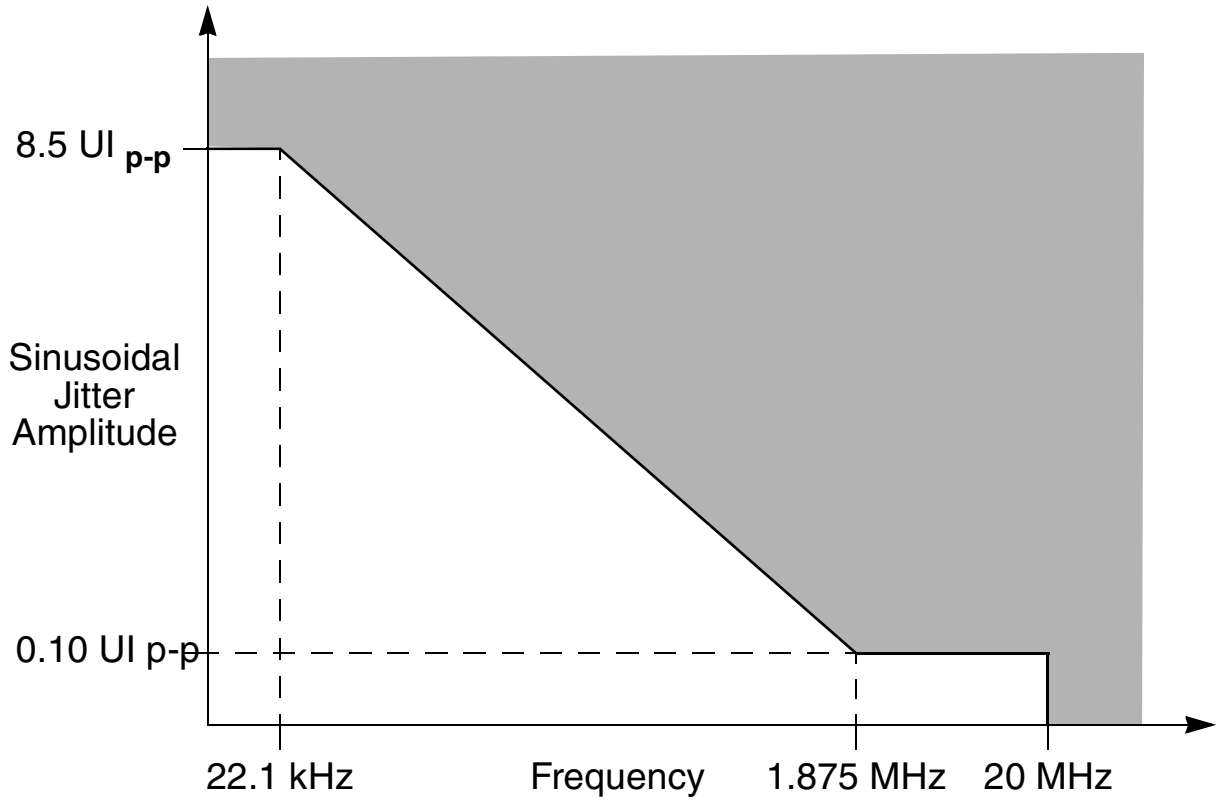


Figure 42. Single Frequency Sinusoidal Jitter Limits

15.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 56, Table 57, Table 58) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 43 with the parameters specified in Table 59. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ohm +/– 5% differential resistive load.

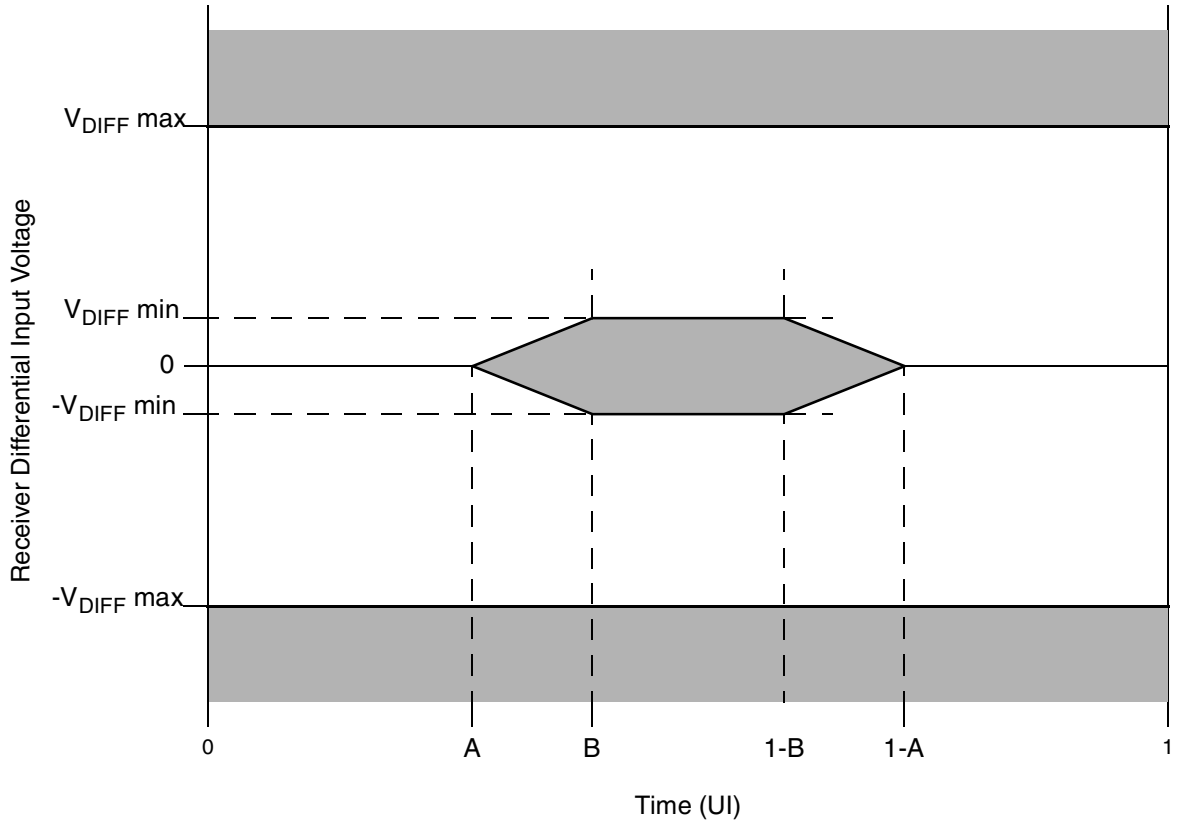


Figure 43. Receiver Input Compliance Mask

Table 59. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

15.9 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

15.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ohms resistive +/– 5% differential to 2.5 GHz.

15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE802.3ae.

15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ohms resistive +/– 5% differential to 2.5 GHz.

15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 8-4 and Table 8-11. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

16 Package

This section details package parameters and dimensions.

16.1 Package Parameters for the MPC8641

The package parameters are as provided in the following list. The package type is 33 mm x 33 mm, 1023 pins. There are two package options: Leaded Flip Chip-Ceramic Ball Grid Array (FC-CBGA), and Lead-free (FC-CBGA).

For all package types:

Die size	12.4 mm x 15.3 mm
Package outline	33 mm x 33 mm
Interconnects	1023
Pitch	1 mm
Minimum module height	1.92 mm
Total Capacitor count	43 caps; 100 nF each

For RoHS Eutetic lead FC-CBGA (package option: HCTE HU)

Maximum module height	2.72 mm
Solder Balls	62% Sn 36% Pb 2% Ag
Ball diameter (typical)	0.60 mm

For RoHS lead-free FC-CBGA (package option: HCTE VU)

Maximum module height	2.72 mm
Solder Balls	95.5% Sn 4.0% Ag 0.5% Cu
Ball diameter (typical)	0.60 mm

16.2 Mechanical Dimensions of the MPC8641 FC-CBGA

Figure 44 shows the mechanical dimensions and bottom surface nomenclature of the MPC8641 lead-free FC-CBGA (package option: HCTE VU) and Eutetic lead FC-CBGA (package option: HCTE HU).

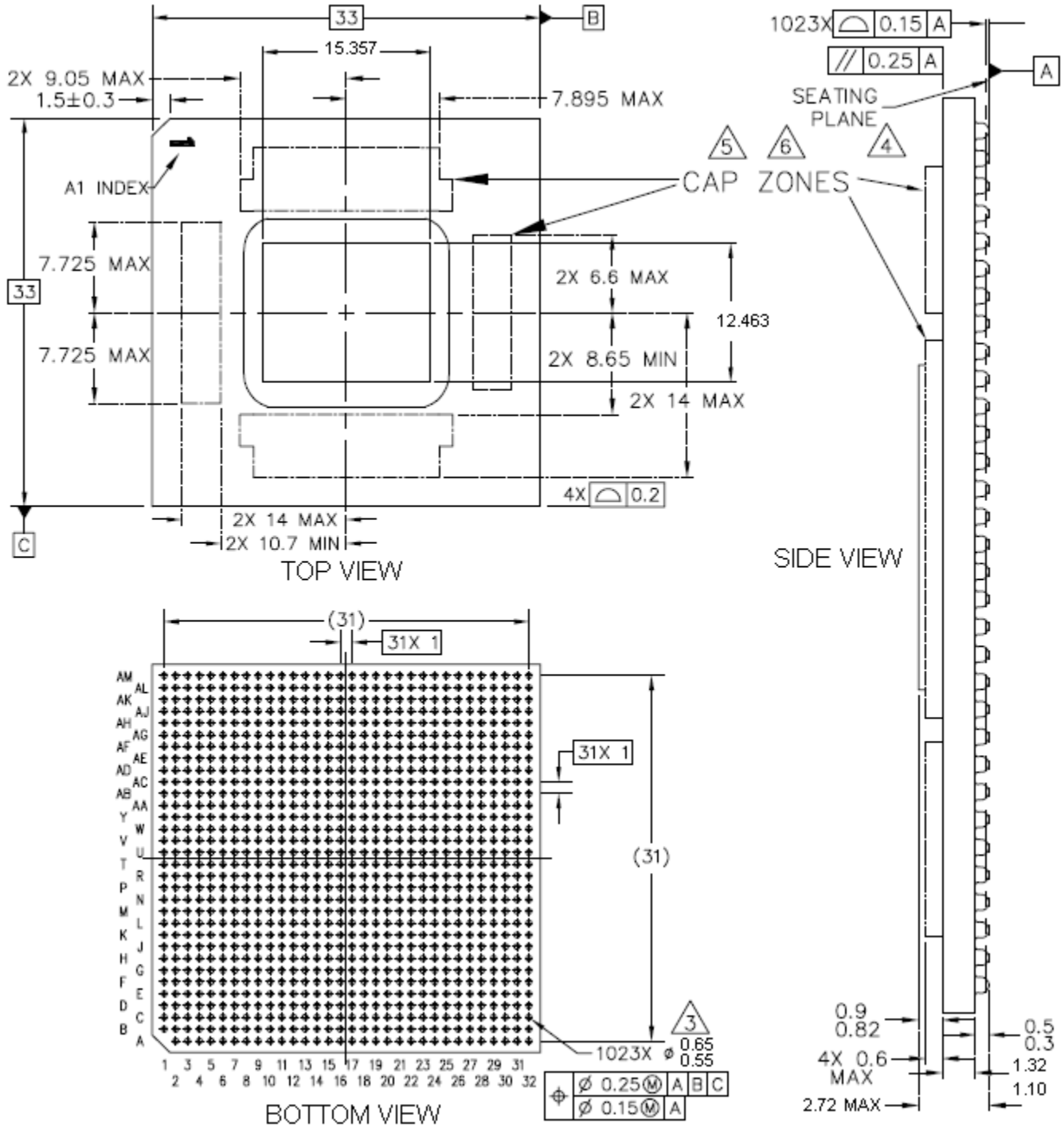


Figure 44. MPC8641 Lead-free or Eutetic Lead FC-CBGA Dimensions

NOTES for Figure 44

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.

17 Signal Listings

Table 60 provides the pin assignments for the signals.

Table 60. MPC8641 Signal Reference by Functional Block

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Interface 1 Signals[2]				
D1_MDQ[0:63]	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L9, L7, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AM14, AL11, AM11, AM13, AK14, AM15, AJ16, AK18, AL18, AJ15, AL15, AL17, AM17	I/O	$D1\_GV_{DD}$	
D1_MECC[0:7]	M8, M7, R8, T10, L11, L10, P9, R10	I/O	$D1\_GV_{DD}$	
D1_MDM[0:8]	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N10	O	$D1\_GV_{DD}$	
D1_MDQS[0:8]	A13, C10, H12, J7, AE8, AM9, AK13, AK17, N9	I/O	$D1\_GV_{DD}$	
$\overline{\text{D1\_MDQS}}$[0:8]	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	$D1\_GV_{DD}$	
D1_MBA[0:2]	AA8, AA10, T9	O	$D1\_GV_{DD}$	
D1_MA[0:15]	Y10, W8, W9, V7, V8, U6, V10, U9, U7, U10, Y9, T6, T8, AE12, R7, P6	O	$D1\_GV_{DD}$	
$\overline{\text{D1\_MWE}}$	AB11	O	$D1\_GV_{DD}$	
$\overline{\text{D1\_MRAS}}$	AB12	O	$D1\_GV_{DD}$	
$\overline{\text{D1\_MCAS}}$	AC10	O	$D1\_GV_{DD}$	
$\overline{\text{D1\_MCS}}$[0:3]	AB9, AD10, AC12, AD11	O	$D1\_GV_{DD}$	
D1_MCKE[0:3]	P7, M10, N8, M11	O	$D1\_GV_{DD}$	23
D1_MCK[0:5]	W6, E13, AH11, Y7, F14, AG10	O	$D1\_GV_{DD}$	
$\overline{\text{D1\_MCK}}$[0:5]	Y6, E12, AH12, AA7, F13, AG11	O	$D1\_GV_{DD}$	
D1_MODT[0:3]	AC9, AF12, AE11, AF10	O	$D1\_GV_{DD}$	

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDIC[0:1]	E15, G14	IO	$D1\_GV_{DD}$	27
$D1\_MV_{REF}$	AM18	DDR Port 1 reference voltage	$D1\_GV_{DD}$ /2	3
DDR Memory Interface 2 Signals[2]				
D2_MDQ[0:63]	A7, B7, C5, D5, C8, D8, D6, A5, C4, A3, D3, D2, A4, B4, C2, C1, E3, E1, H4, G1, D1, E4, G3, G2, J4, J2, L1, L3, H3, H1, K1, L4, AA4, AA2, AD1, AD2, Y1, AA1, AC1, AC3, AD5, AE1, AG1, AG2, AC4, AD4, AF3, AF4, AH3, AJ1, AM1, AM3, AH1, AH2, AL2, AL3, AK5, AL5, AK7, AM7, AK4, AM4 ,AM6, AJ7	I/O	$D2\_GV_{DD}$	
D2_MECC[0:7]	H6, J5, M5, M4, G6, H7, M2, M1	I/O	$D2\_GV_{DD}$	
D2_MDM[0:8]	C7, B3, F4, J1, AB1, AE2, AK1, AM5, K6	O	$D2\_GV_{DD}$	
D2_MDQS[0:8]	B6, B1, F1, K2, AB3, AF1, AL1, AL6, L6	I/O	$D2\_GV_{DD}$	
$\overline{\text{D2\_MDQS}}$[0:8]	A6, A2, F2, K3, AB2, AE3, AK2, AJ6, K5	I/O	$D2\_GV_{DD}$	
D2_MBA[0:2]	W5, V5, P3	O	$D2\_GV_{DD}$	
D2_MA[0:15]	W1, U4, U3, T1, T2, T3, T5, R2, R1, R5, V4, R4, P1, AH5, P4, N1	O	$D2\_GV_{DD}$	
$\overline{\text{D2\_MWE}}$	Y4	O	$D2\_GV_{DD}$	
$\overline{\text{D2\_MRAS}}$	W3	O	$D2\_GV_{DD}$	
$\overline{\text{D2\_MCAS}}$	AB5	O	$D2\_GV_{DD}$	
$\overline{\text{D2\_MCS}}$[0:3]	Y3, AF6, AA5, AF7	O	$D2\_GV_{DD}$	
D2_MCKE[0:3]	N6, N5, N2, N3	O	$D2\_GV_{DD}$	23
D2_MCK[0:5]	U1, F5, AJ3, V2, E7, AG4	O	$D2\_GV_{DD}$	
$\overline{\text{D2\_MCK}}$[0:5]	V1, G5, AJ4, W2, E6, AG5	O	$D2\_GV_{DD}$	
D2_MODT[0:3]	AE6, AG7, AE5, AH6	O	$D2\_GV_{DD}$	
D2_MDIC[0:1]	F8, F7	IO	$D2\_GV_{DD}$	27
$D2\_MV_{REF}$	A18	DDR Port 2 reference voltage	$D2\_GV_{DD}$ /2	3

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
High Speed I/O Interface 1 (SERDES 1)[4]				
SD1_TX[0:7]	L26, M24, N26, P24, R26, T24, U26, V24	O	SV_{DD}	
$\overline{\text{SD1\_TX}}$[0:7]	L27, M25, N27, P25, R27, T25, U27, V25	O	SV_{DD}	
SD1_RX[0:7]	J32, K30, L32, M30, T30, U32, V30, W32	I	SV_{DD}	
$\overline{\text{SD1\_RX}}$[0:7]	J31, K29, L31, M29, T29, U31, V29, W31	I	SV_{DD}	
SD1_REF_CLK	N32	I	SV_{DD}	
$\overline{\text{SD1\_REF\_CLK}}$	N31	I	SV_{DD}	
SD1_IMP_CAL_TX	Y26	Analog	SV_{DD}	19
SD1_IMP_CAL_RX	J28	Analog	SV_{DD}	30
SD1_PLL_TPD	U28	O	SV_{DD}	13, 17
SD1_PLL_TPA	T28	Analog	SV_{DD}	17, 18
SD1_DLL_TPD	N28	O	SV_{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV_{DD}	17, 18
High Speed I/O Interface 2 (SERDES 2)[4]				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV_{DD}	
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV_{DD}	34
$\overline{\text{SD2\_TX}}$[0:3]	Y25, AA28, AB26, AC28	O	SV_{DD}	
$\overline{\text{SD2\_TX}}$[4:7]	AE28, AG28, AJ28, AL28	O	SV_{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV_{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV_{DD}	32, 35
$\overline{\text{SD2\_RX}}$[0:3]	Y29, AA31, AB29, AC31	I	SV_{DD}	32
$\overline{\text{SD2\_RX}}$[4:7]	AH29, AJ31, AK29, AL31	I	SV_{DD}	32, 35
SD2_REF_CLK	AE32	I	SV_{DD}	
$\overline{\text{SD2\_REF\_CLK}}$	AE31	I	SV_{DD}	
SD2_IMP_CAL_TX	AM29	Analog	SV_{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV_{DD}	30
SD2_PLL_TPD	AF29	O	SV_{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV_{DD}	17, 18

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
SD2_DLL_TPD	AD29	O	SV_{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV_{DD}	17, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29	-	-	13
Reserved	H30, R32	-	-	14
Reserved	H29, R31	-	-	15
Reserved	AD24, AG26	-	-	16
Ethernet Miscellaneous Signals[5]				
EC1_GTX_CLK125	AL23	I	LV_{DD}	39
EC2_GTX_CLK125	AM23	I	TV_{DD}	39
EC_MDC	G31	O	OV_{DD}	
EC_MDIO	G32	I/O	OV_{DD}	
eTSEC Port 1 Signals[5]				
TSEC1_TXD[0:7]/ GPOUT[0:7]	AF25, AC23,AG24, AG23, AE24, AE23, AE22, AD22	O	LV_{DD}	6, 10
TSEC1_TX_EN	AB22	O	LV_{DD}	36
TSEC1_TX_ER	AH26	O	LV_{DD}	
TSEC1_TX_CLK	AC22	I	LV_{DD}	40
TSEC1_GTX_CLK	AH25	O	LV_{DD}	
TSEC1_CRS	AM24	I/O	LV_{DD}	37
TSEC1_COL	AM25	I	LV_{DD}	
TSEC1_RXD[0:7]/ GPIN[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	LV_{DD}	10
TSEC1_RX_DV	AJ24	I	LV_{DD}	
TSEC1_RX_ER	AJ25	I	LV_{DD}	
TSEC1_RX_CLK	AK24	I	LV_{DD}	40
eTSEC Port 2 Signals[5]				
TSEC2_TXD[0:3]/ GPOUT[8:15]	AB20, AJ23, AJ22, AD19	O	LV_{DD}	6, 10
TSEC2_TXD[4]/ GPOUT[12]	AH23	O	LV_{DD}	6,10, 38

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TXD[5:7]/ GPOUT[13:15]	AH21, AG22, AG21	O	LV_{DD}	6, 10
TSEC2_TX_EN	AB21	O	LV_{DD}	36
TSEC2_TX_ER	AB19	O	LV_{DD}	6, 38
TSEC2_TX_CLK	AC21	I	LV_{DD}	40
TSEC2_GTX_CLK	AD20	O	LV_{DD}	
TSEC2_CRS	AE20	I/O	LV_{DD}	37
TSEC2_COL	AE21	I	LV_{DD}	
TSEC2_RXD[0:7]/ GPIN[8:15]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	LV_{DD}	10
TSEC2_RX_DV	AC19	I	LV_{DD}	
TSEC2_RX_ER	AD21	I	LV_{DD}	
TSEC2_RX_CLK	AM22	I	LV_{DD}	40
eTSEC Port 3 Signals[5]				
TSEC3_TXD[0:3]	AL21, AJ21, AM20, AJ20	O	TV_{DD}	6
TSEC3_TXD[4]/	AM19	O	TV_{DD}	
TSEC3_TXD[5:7]	AK21, AL20, AL19	O	TV_{DD}	6
TSEC3_TX_EN	AH19	O	TV_{DD}	36
TSEC3_TX_ER	AH17	O	TV_{DD}	
TSEC3_TX_CLK	AH18	I	TV_{DD}	40
TSEC3_GTX_CLK	AG19	O	TV_{DD}	
TSEC3_CRS	AE15	I/O	TV_{DD}	37

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_COL	AF15	I	TV_{DD}	
TSEC3_RXD[0:7]	AJ17, AE16, AH16, AH14, AJ19, AH15, AG16, AE19	I	TV_{DD}	
TSEC3_RX_DV	AG15	I	TV_{DD}	
TSEC3_RX_ER	AF16	I	TV_{DD}	
TSEC3_RX_CLK	AJ18	I	TV_{DD}	40
eTSEC Port 4 Signals[5]				
TSEC4_TXD[0:3]	AC18, AC16, AD18, AD17	O	TV_{DD}	6
TSEC4_TXD[4]	AD16	O	TV_{DD}	25
TSEC4_TXD[5:7]	AB18, AB17, AB16	O	TV_{DD}	6
TSEC4_TX_EN	AF17	O	TV_{DD}	36
TSEC4_TX_ER	AF19	O	TV_{DD}	
TSEC4_TX_CLK	AF18	I	TV_{DD}	40
TSEC4_GTX_CLK	AG17	O	TV_{DD}	
TSEC4_CRS	AB14	I/O	TV_{DD}	37
TSEC4_COL	AC13	I	TV_{DD}	
TSEC4_RXD[0:7]	AG14, AD13, AF13, AD14, AE14, AB15, AC14, AE17	I	TV_{DD}	
TSEC4_RX_DV	AC15	I	TV_{DD}	
TSEC4_RX_ER	AF14	I	TV_{DD}	
TSEC4_RX_CLK	AG13	I	TV_{DD}	40
Local Bus Signals[5]				
LAD[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	I/O	OV_{DD}	6
LDP[0:3]	A24, E24, C24, B24	I/O	OV_{DD}	6, 22

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
LA[27:31]	J21, K21, G22, F24, G21	O	OV_{DD}	6, 22
$\overline{\text{LCS}}$[0:4]	A22, C22, D23, E22, A23	O	OV_{DD}	7
$\overline{\text{LCS}}$[5]/$\overline{\text{DMA\_DREQ}}$[2]	B23	O	OV_{DD}	7, 9, 10
$\overline{\text{LCS}}$[6]/$\overline{\text{DMA\_DACK}}$[2]	E23	O	OV_{DD}	7, 10
$\overline{\text{LCS}}$[7]/$\overline{\text{DMA\_DDONE}}$[2]	F23	O	OV_{DD}	7, 10
$\overline{\text{LWE}}$[0:3]/ LSDDQM[0:3]/ $\overline{\text{LBS}}$[0:3]	E21, F21, D22, E20	O	OV_{DD}	6
LBCTL	D21	O	OV_{DD}	
LALE	E19	O	OV_{DD}	
LGPL0/LSDA10	F20	O	OV_{DD}	25
LGPL1/$\overline{\text{LSDWE}}$	H20	O	OV_{DD}	25
LGPL2/$\overline{\text{LOE}}$/ $\overline{\text{LSDRAS}}$	J20	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$	K20	O	OV_{DD}	6
LGPL4/$\overline{\text{LGTA}}$/ LUPWAIT/LPBSE	L21	I/O	OV_{DD}	
LGPL5	J19	O	OV_{DD}	6
LCKE	H19	O	OV_{DD}	
LCLK[0:2]	G19, L19, M20	O	OV_{DD}	
LSYNC_IN	M19	I	OV_{DD}	
LSYNC_OUT	D20	O	OV_{DD}	
DMA Signals[5]				
$\overline{\text{DMA\_DREQ}}$[0:1]	E31, E32	I	OV_{DD}	
$\overline{\text{DMA\_DREQ}}$[2]/$\overline{\text{LCS}}$[5]	B23	I	OV_{DD}	9, 10
$\overline{\text{DMA\_DREQ}}$[3]/IRQ[9]	B30	I	OV_{DD}	10
$\overline{\text{DMA\_DACK}}$[0:1]	D32, F30	O	OV_{DD}	

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
DMA_DACK[2]/LCS[6]	E23	O	OV_{DD}	10
DMA_DACK[3]/IRQ[10]	C30	O	OV_{DD}	9, 10
DMA_DDONE[0:1]	F31, F32	O	OV_{DD}	
DMA_DDONE[2]/LCS[7]	F23	O	OV_{DD}	10
DMA_DDONE[3]/IRQ[11]	D30	O	OV_{DD}	9, 10
Programmable Interrupt Controller Signals[5]				
MCP_0	F17	I	OV_{DD}	
MCP _1	H17	I	OV_{DD}	12
IRQ[0:8]	G28, G29, H27, J23, M23, J27, F28, J24, L23	I	OV_{DD}	
IRQ[9]/DMA_DREQ[3]	B30	I	OV_{DD}	10
IRQ[10]/DMA_DACK[3]	C30	I	OV_{DD}	9, 10
IRQ[11]/DMA_DDONE[3]	D30	I	OV_{DD}	9, 10
IRQ_OUT	J26	O	OV_{DD}	7, 11
DUART Signals[5]				
UART_SIN[0:1]	B32, C32	I	OV_{DD}	
UART_SOUT[0:1]	D31, A32	O	OV_{DD}	
UART_CTS[0:1]	A31, B31	I	OV_{DD}	
UART_RTS[0:1]	C31, E30	O	OV_{DD}	
I^2C Signals				
IIC1_SDA	A16	I/O	OV_{DD}	7, 11
IIC1_SCL	B17	I/O	OV_{DD}	7, 11
IIC2_SDA	A21	I/O	OV_{DD}	7, 11
IIC2_SCL	B21	I/O	OV_{DD}	7, 11

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
System Control Signals[5]				
$\overline{\text{HRESET}}$	B18	I	OV_{DD}	
$\overline{\text{HRESET\_REQ}}$	K18	O	OV_{DD}	
$\overline{\text{SMI\_0}}$	L15	I	OV_{DD}	
$\overline{\text{SMI\_1}}$	L16	I	OV_{DD}	12
$\overline{\text{SRESET\_0}}$	C20	I	OV_{DD}	
$\overline{\text{SRESET\_1}}$	C21	I	OV_{DD}	12
$\overline{\text{CKSTP\_IN}}$	L18	I	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	L17	O	OV_{DD}	7, 11
READY/TRIG_OUT	J13	O	OV_{DD}	10, 25
Debug Signals[5]				
TRIG_IN	J14	I	OV_{DD}	
TRIG_OUT/READY	J13	O	OV_{DD}	10, 25
D1_MSRCID[0:1]/ LB_SRCID[0:1]	F15, K15	O	OV_{DD}	6, 10
D1_MSRCID[2]/ LB_SRCID[2]	K14	O	OV_{DD}	10, 25
D1_MSRCID[3:4]/ LB_SRCID[3:4]	H15, G15	O	OV_{DD}	10
D2_MSRCID[0:4]	E16, C17, F16, H16, K16	O	OV_{DD}	
D1_MDVAL/LB_DVAL	J16	O	OV_{DD}	10
D2_MDVAL	D19	O	OV_{DD}	
Power Management Signals[5]				
ASLEEP	C19	O	OV_{DD}	
System Clocking Signals[5]				
SYSCLK	G16	I	OV_{DD}	
RTC	K17	I	OV_{DD}	32
CLK_OUT	B16	O	OV_{DD}	23
Test Signals[5]				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV_{DD}	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV_{DD}	26

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
JTAG Signals[5]				
TCK	H18	I	OV_{DD}	
TDI	J18	I	OV_{DD}	24
TDO	G18	O	OV_{DD}	23
TMS	F18	I	OV_{DD}	24
$\overline{\text{TRST}}$	A17	I	OV_{DD}	24
Miscellaneous[5]				
Spare	J17	-	-	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV_{DD}	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV_{DD}	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV_{DD}	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV_{DD}	10
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	-	
TEMP_CATHODE	Y11	Thermal	-	
Sense, Power and GND Signals				
$SENSEV_{DD}$_Core0	M14	V_{DD}_Core0 sensing pin		31
$SENSEV_{DD}$_Core1	U20	V_{DD}_Core1 sensing pin		12,31
$SENSEV_{SS}$_Core0	P14	Core0 GND sensing pin		31
$SENSEV_{SS}$_Core1	V20	Core1 GND sensing pin		12, 31
D1_GV_{DD}	B11, B14, D10, D13, F9, F12, H8, H11, H14, K10, K13, L8, P8, R6, U8, V6, W10, Y8, AA6, AB10, AC8, AD12, AE10, AF8, AG12, AH10, AJ8, AJ14, AK12, AL10, AL16	SDRAM 1 I/O supply	D1_GV_{DD} 2.5 - DDR 1.8 DDR2	
D2_GV_{DD}	B2, B5, B8, D4, D7, E2, F6, G4, H2, J6, K4, L2, M6, N4, P2, T4, U2, W4, Y2, AB4, AC2, AD6, AE4, AF2, AG6, AH4, AJ2, AK6, AL4, AM2	SDRAM 2 I/O supply	D2_GV_{DD} 2.5 V - DDR 1.8 V - DDR2	

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
OV_{DD}	B22, B25, B28, D17, D24, D27, F19, F22, F26, F29, G17, H21, H24, K19, K23, M21, AM30	DUART, Local Bus, DMA , Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD} 3.3 V	
LV_{DD}	AC20, AD23, AH22	TSEC1 and TSEC2 I/O voltage	LV_{DD} 2.5/3.3 V	
TV_{DD}	AC17, AG18, AK20	TSEC3 and TSEC4 I/O voltage	TV_{DD} 2.5/3.3 V	
SV_{DD}	H31, J29, K28, K32, L30, M28, M31, N29, R30, T31, U29, V32, W30, Y31, AA29, AB32, AC30, AD31, AE29, AG30, AH31, AJ29, AK32, AL30, AM31	Trasceiver Power Supply Serdes	SV_{DD}	
XV_{DD}_SRDS1	K26, L24 , M27, N25, P26, R24, R28, T27, U25, V26	Serial I/O Power Supply for Serdes Port 1	XV_{DD}_SRDS1 1.05/1.1 V	42
XV_{DD}_SRDS2	AA25, AB28, AC26, AD27, AE25, AF28, AH27, AK28, AM27, W24, Y27	Serial I/O Power Supply for Serdes Port 2	XV_{DD}_SRDS2 1.05/1.1 V	
V_{DD}_Core0	L12, L13, L14, M13, M15, N12, N14, P11, P13, P15, R12, R14, T11, T13, T15, U12, U14, V11, V13, V15, W12, W14, Y12, Y13, Y15, AA12, AA14, AB13	Core 0 voltage supply	V_{DD}_Core0 1.05/1.1 V	
V_{DD}_Core1	R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, ,Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24	Core 1 voltage supply	V_{DD}_Core1 1.05/1.1 V	12
V_{DD}_PLAT	M16, M17, M18, N16, **N18**, N20, N22, P17, P19, P21, P23, R22	Platform supply voltage	V_{DD}_PLAT 1.05/1.1 V	28
AV_{DD}_Core0	B20	Core 0 PLL Supply	AV_{DD}_Core0 1.05/1.1 V	
AV_{DD}_Core1	A19	Core 1 PLL Supply	AV_{DD}_Core1 1.05/1.1 V	12
AV_{DD}_PLAT	B19	Platform PLL supply voltage	AV_{DD}_PLAT 1.05/1.1 V	

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
AV_{DD}_LB	A20	Local Bus PLL supply voltage	AV_{DD}_LB 1.05/1.1 V	
AV_{DD}_SRDS1	P32	Serdes Port 1 PLL & DLL Power Supply	AV_{DD}_SRDS1 1.05/1.1 V	
AV_{DD}_SRDS2	AF32	Serdes Port 2 PLL & DLL Power Supply	AV_{DD}_SRDS2 1.05/1.1 V	
GND	C3, C6, C9, C12, C15, C23, C26, E5, E8, E11, E14, E18, E25, E28, F3, G7, G10, G13, G20, G23, G27, G30, H5, J3, J9, J12, J15, J22, J25, K7, L5, L20, M3, M9, M12, N7, N11, N13, N15, N17, N19, N21, N23, P5, P12, P16, **P18,** P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, T7, T12, T14, T16, T18, T20, T22, U5, U11,U13, U15, U17, U19, U21, U23, V3, V9, V12, V14, V16, V18, V22, W7, W11, W13, W15, W17, W19, W21, W23,Y5, Y14, Y16, Y18, Y20, Y22, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA23, AB7, AB24, AC5, AC11, AD3, AD9, AD15, AE7, AE13, AE18, AF5, AF11, AF21, AF24, AG3, AG9, AH7, AH13, AJ5, AJ11, AK3, AK9, AK15, AK19, AK23, AL7, AL13	GND	-	29
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV_{DD}_SRDS1	-	
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV_{DD}_SRDS2	-	
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29,Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV_{DD}		
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV_{DD}_SRDS*n*		
Reset Configuration Signals[20]				
TSEC1_TXD[0] / $\overline{\text{cfg\_alt\_boot\_vec}}$	AF25	-	LV_{DD}	
TSEC1_TXD[1]/ cfg_platform_freq	AC23	-	LV_{DD}	21
TSEC1_TXD[2:4]/ cfg_device_id[5:7]	AG24, AG23, AE24	-	LV_{DD}	

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[5]/ cfg_tsec1_reduce	AE23	-	LV_{DD}	
TSEC1_TXD[6:7]/ cfg_tsec1_prtcl[0:1]	AE22, AD22	-	LV_{DD}	
TSEC2_TXD[0:3]/ cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	-	LV_{DD}	
TSEC2_TXD[4], TSEC2_TX_ER/ cfg_dram_type[0:1]	AH23, AB19	-	LV_{DD}	38
TSEC2_TXD[5]/ cfg_tsec2_reduce	AH21	-	LV_{DD}	
TSEC2_TXD[6:7]/ cfg_tsec2_prtcl[0:1]	AG22, AG21	-	LV_{DD}	
TSEC3_TXD[0:1]/ cfg_spare[0:1]	AL21, AJ21	O	TV_{DD}	33
TSEC3_TXD[2]/ cfg_core1_enable	AM20	O	TV_{DD}	
TSEC3_TXD[3]/ cfg_core1_lm_offset	AJ20	-	LV_{DD}	
TSEC3_TXD[5]/ cfg_tsec3_reduce	AK21	-	LV_{DD}	
TSEC3_TXD[6:7]/ cfg_tsec3_prtcl[0:1]	AL20, AL19	-	LV_{DD}	
TSEC4_TXD[0:3]/ cfg_io_ports[0:3]	AC18, AC16, AD18, AD17	-	LV_{DD}	
TSEC4_TXD[5]/ cfg_tsec4_reduce	AB18	-	LV_{DD}	
TSEC4_TXD[6:7]/ cfg_tsec4_prtcl[0:1]	AB17, AB16	-	LV_{DD}	
LAD[0:31]/ cfg_gpporcr[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	-	OV_{DD}	
$\overline{\text{LWE[0]}}$/ cfg_cpu_boot	E21	-	OV_{DD}	
$\overline{\text{LWE[1]}}$/ cfg_rio_sys_size	F21	-	OV_{DD}	
$\overline{\text{LWE[2:3]}}$/ cfg_host_agt[0:1]	D22, E20	-	OV_{DD}	
LDP[0:3], LA[27] / cfg_core_pll[0:4]	A24, E24, C24, B24, J21	-	OV_{DD}	22

Table 60. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
LA[28:31]/ cfg_sys_pll[0:3]	K21, G22, F24, G21	-	OV_{DD}	22
LGPL[3], LGPL[5]/ cfg_boot_seq[0:1]	K20, J19	-	OV_{DD}	
D1_MSRCID[0]/ cfg_mem_debug	F15	-	OV_{DD}	
D1_MSRCID[1]/ cfg_ddr_debug	K15	-	OV_{DD}	

Note:

1. Multi-pin signals such as D1_MDQ[0:63] and D2_MDQ[0:63] have their physical package pin numbers listed in order corresponding to the signal names.
2. Stub Series Terminated Logic (SSTL-18 and SSTL-25) type pins.

4. Low Voltage Differential Signaling (LVDS) type pins.
5. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
6. This pin is a reset configuration pin and appears again in the Reset Configuration Signals section of this table. See the Reset Configuration Signals section of this table for config name and connection details.
7. Recommend a weak pull-up resistor (2–10 kΩ) be placed from this pin to its power supply.
8. Recommend a weak pull-down resistor (2–10 kΩ) be placed from this pin to ground.
9. This multiplexed pin has input status in one mode and output in another
10. This pin is a multiplexed signal for different functional blocks and appears more than once in this table.
11. This pin is open drain signal.
12. Functional only on the MPC8641D.
13. These pins should be left floating.
14. These pins should be connected to SVDD.
15. These pins should be pulled to ground with a strong resistor (270-Ω to 330-Ω) .
16. These pins should be connected to OVDD.
17. This is a digital test signal from the SerDes PLL/DLL. It will allow observability of various digital outputs during PLL/DLL Testing.
18. Should be pulled to ground.
19. This pin should be pulled to ground with a 100-Ω resistor.
20. The pins in this section are reset configuration pins. Each pin has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
21. Should be pulled down at reset if platform frequency is at 400 MHz.
22. These pins require 4.7-kΩ pull-up or pull-down resistors and must be driven as they are used to determine PLL configuration ratios at reset.
23. This output is actively driven during reset rather than being tri-stated during reset.
24 These JTAG pins have weak internal pull-up P-FETs that are always enabled.
25. This pin should NOT be pulled down (or driven low) during reset.
26. These are test signals for factory use only and must be pulled up (100-Ω to 1- kΩ.) to OVDD for normal machine operation.
27. Dn_MDIC[0] should be connected to ground with an 18-Ω resistor +/- 1-Ω and Dn_MDIC[1] should be connected Dn_GVDD with an 18-Ω resistor +/- 1-Ω . These pins are used for automatic calibration of the DDR IOs.

28. Pin N18 will possibly be used in later silicon revisions as a sense pin for VDD_PLAT and in that case will be called SENSEVDD_PLAT. We recommend using an optional 0-Ω resistor connection from this pin to VDD_PLAT to allow for this possible change in the future. In that case this pin will be considered as the central observation point for verifying the voltage of VDD_PLAT.
29. Pin P18 is intended to be possibly used in later silicon revisions as a ground sense pin for the platform and in that case will be called SENSEVSS_PLAT. We recommend using an optional 0-Ω resistor connection from this pin to GND to allow for this possible change in the future. In that case this pin will be considered as the central ground observation point for verifying the voltage of VDD_PLAT
30. This pin should be pulled to ground with a 200-Ω resistor.
31. These pins are connected to the power/ground planes internally and may be used by the core power supply to improve tracking and regulation.
32. Must be tied low if unused
33. These pins may be used as defined functional reset configuration pins in the future. Please include a resistor pull up/down option to allow flexibility of future designs.
34. Used as serial data output for SRIO 1x/4x link.
35. Used as serial data input for SRIO 1x/4x link.
36. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
37. This pin is only an output in FIFO mode when used as Rx Flow Control.
38. This pin functions as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION in sleep mode.
39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).
40. See Section 18.4.2, “Platform to FIFO restrictions” for clock speed limitations for this pin when used in FIFO mode.

18 Clocking

This section describes the PLL configuration of the MPC8641. Note that the platform clock is identical to the MPX clock.

18.1 Clock Ranges

Table 62 provides the clocking specifications for the processor cores and Table 63 provides the clocking specifications for the memory bus.

Table 61. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1000 MHz		1250MHz		1333MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	800	1000	800	1250	800	1333	800	1500	MHz	1, 2

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

Table 62. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1000 MHz		1250MHz		1333MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	800	1000	800	1250	800	1333	800	1500	MHz	1, 2

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

Table 63. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1200, 1333, 1500 MHz			
	Min	Max		
Memory bus clock frequency	200	300	MHz	1, 2

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio.
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

Table 64. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1200, 1333, 1500MHz			
	Min	Max		
Local bus clock speed (for Local Bus Controller)	25	166	MHz	1

Notes:

1. The Local bus clock speed on LCLK[0:2] is determined by MPX clock divided by the Local Bus PLL ratio programmed in LCCR[CLKDIV]. See the reference manual for the MPC8641D for more information on this..

18.2 MPX to SYSCLK PLL Ratio

The MPX clock is the clock that drives the MPX bus, and is also called the platform clock. The frequency of the MPX is set using the following reset signals, as shown in Table 65:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting theMPX bus frequency, since the MPX frequency must equal the DDR data rate.

Table 65. MPX Clock Ratio

Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio	Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio
0000	Reserved	1000	8:1
0001	Reserved	1001	9:1

Table 65. MPX Clock Ratio

Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio	Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio
0010	2:1	1010	Reserved
0011	3:1	1011	Reserved
0100	4:1	1100	Reserved
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

18.3 e600 to MPX clock PLL Ratio

Table 66 describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg_core_pll[0:4] - reset config name) at power up, as shown in Table 66.

Table 66. e600 Core to MPX Clock Ratio

Binary Value of LDP[0:3], LA[27] Signals	e600 core: MPX Clock Ratio
01000	2:1
01100	2.5:1
10000	3:1
11100	3.5:1
10100	4:1
01110	4.5:1

18.4 Frequency Options

18.4.1 Sysclk to Platform Frequency Options

Table 67 shows some SYSCLK frequencies and the expected MPX frequency values fbased on the MPX clock to SYSCLK ratio. Note that frequencies between 400 MHz and 500 MHz are NOT supported on the

platform. See note regarding *cfg_platform_freq* in Section 17, "Signal Listings" since it is a reset configuration pin that is related to platform frequency.

Table 67. Frequency Options of SYSCLK with Respect to Platform/MPX Clock Speed

MPX to SYSCLK Ratio	SYSCLK (MHz)					
	66	83	100	111	133	167
	Platform/MPX Frequency (MHz) [1]					
2						333
3					400	500
4			400		533	
5			500	555		
6	400	500	600			
8	533					
9	600					

1 SYSCLK frequency range is 66-167 MHz. Platform clock/ MPX frequency range is 400 MHz, 500-600 MHz.

18.4.2 Platform to FIFO restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency / 4.2

For example, if the platform frequency is 533MHz, the FIFO TX/RX clock frequency should be no than 127MHz

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency / 3.2

For example, if the platform frequency is 533MHz, the FIFO TX/RX clock frequency should be no than 167MHz

19 Thermal

This section describes the thermal specifications of the MPC8641.

19.1 Thermal Characteristics

Table 68 provides the package thermal characteristics for the MPC8641.

Table 68. Package Thermal Characteristics[1]

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	18	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JA}$	13	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	13	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-board thermal resistance	$R_{\theta JB}$	5	°C/W	4
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	°C/W	5

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W.

NOTE

The thermal performance of the LGA and the BGA versions of the package are the same. For the thermal model, the only difference is the height of the solder layer under the substrate.

19.2 Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8641 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 19.2.4, “Temperature Diode,” for more information.

To reduce the die-junction temperature, heat sinks are required; due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds force (45 newtons). Figure 45 and Figure 46

show a spring clip through the board. Occasionally the spring clip is attached to soldered hooks or to a plastic backing structure. Screw and spring arrangements are also frequently used.

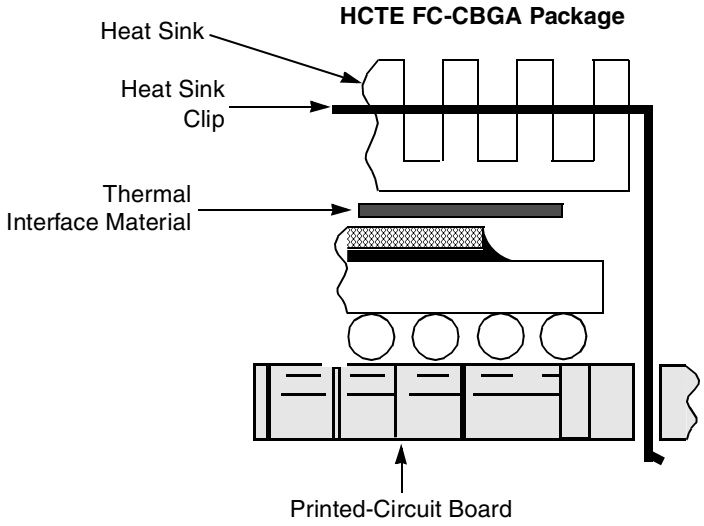


Figure 45. FC-CBGA Package Exploded Cross-Sectional View with Several Heat Sink Options

NOTE

A clip-on-chip heat sink solution will NOT work with the FC-CLGA part.
A through-hole solution is recommended, as shown in Figure 46 below.

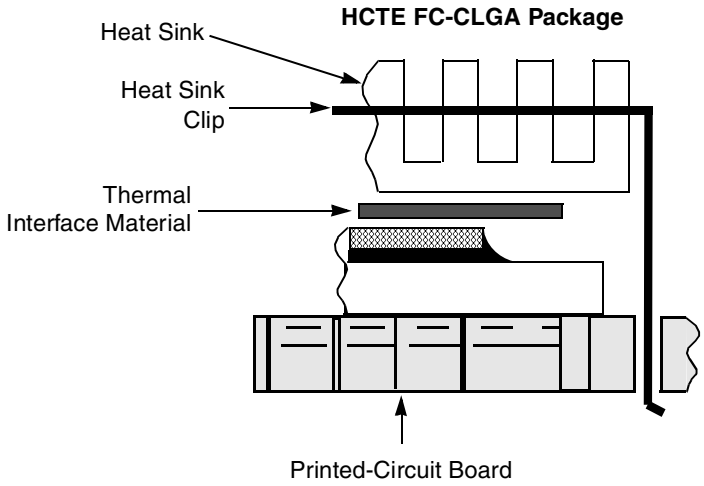


Figure 46. FC-CLGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC8641 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27.	781-769-2800

Norwood, MA02062 Internet: www.qats.com	
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgreg.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

19.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 68, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 47 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

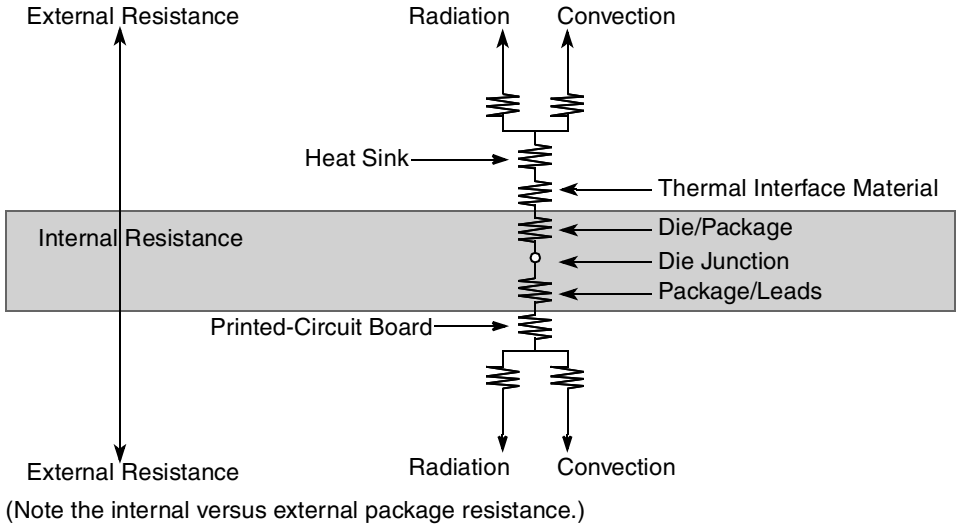


Figure 47. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

19.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 48 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 45). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the MPC8641. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

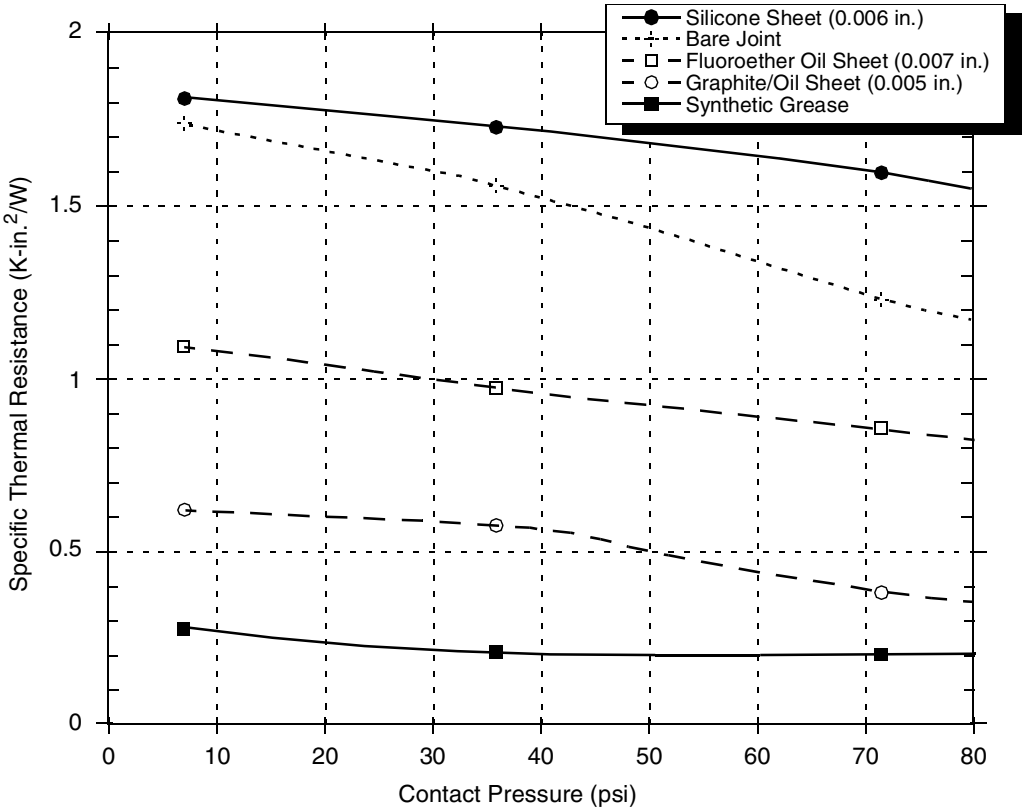


Figure 48. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO Box 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481

Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

19.2.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_i is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 43.4 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 0.2°C/W + \theta_{sa}) \times 43.4\ W$

For this example, a $R_{\theta sa}$ value of 1.32 °C/W or less is required to maintain the die junction temperature below the maximum value of Table 2.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local

heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC8641 thermal model is shown in Figure 49. Four cuboids are used to represent this device. The die is modeled as 12.4x15.3 mm at a thickness of 0.86 mm. See Section 3, "Power Characteristics" for power dissipation details. The substrate is modeled as a single block 33x33x1.2 mm with orthotropic conductivity: 13.5 W/(m • K) in the xy-plane and 5.3 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 5.3 W/(m • K) in the thickness dimension of 0.07 mm. The C5 solder layer is modeled as a cuboid with dimensions 33x33x0.4 mm and orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 9.6 W/(m • K) in the z-direction. An LGA solder layer would be modeled as a collapsed thermal resistance with thermal conductivity of 9.6W/(m • K) and an effective height of 0.1 mm.

Conductivity	Value	Unit
Die (12.4x15.3x0.86 mm)		
Silicon	Temperature dependent	
Bump and Underfill (12.4 × 15.3 × 0.070 mm)		
k_z	5.3	W/(m • K)
Substrate (33 × 33 × 1.2 mm)		
k_x	13.5	W/(m • K)
k_y	13.5	
k_z	5.3	
C5 Solder layer (33 × 33 × 0.4 mm)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	9.6	

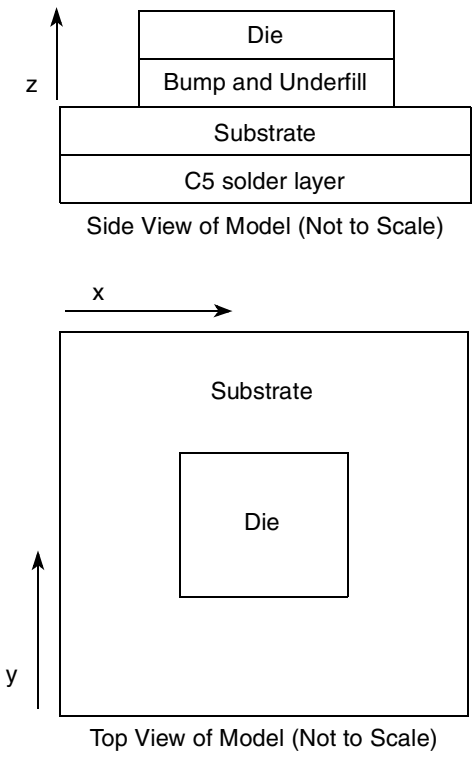


Figure 49. Recommended Thermal Model of MPC8641

19.2.4 Temperature Diode

The MPC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of

the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each MPC8641's internal diode.

The following are the specifications of the MPC8641 on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

Operating range 2–300 µA

Diode leakage < 10 nA @ 125°C

Ideality factor over 5–150 µA at 60°C: n = 1.0275 ± 0.9%

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ln\frac{I_H}{I_L} \right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

20 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8641.

20.1 System Clocking

This device includes six PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 18.2, “MPX to SYSCLK PLL Ratio.”
2. The dual e600 Core PLLs generate the MPX clock from the externally supplied input.
3. The local bus PLL generates the clock for the local bus.
4. There are two PLLs for the SerDes block.

20.2 Power Supply Design and Sequencing

20.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins .

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 51, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 50 and Figure 51 show the PLL power supply filter circuits for the platform and cores, respectively.

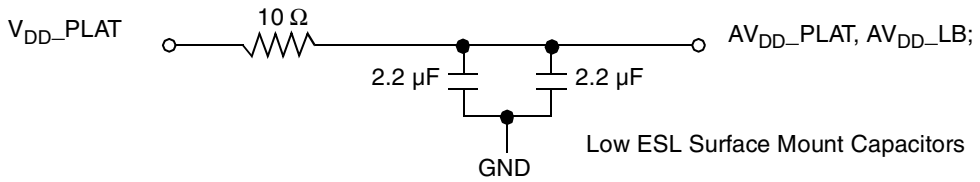


Figure 50. MPC8641 PLL Power Supply Filter Circuit (for platform)

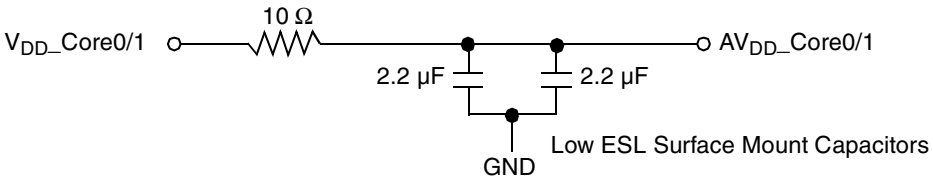
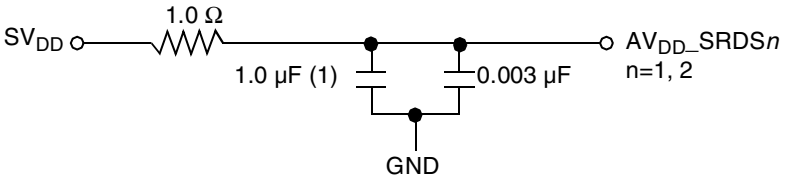


Figure 51. MPC8641 PLL Power Supply Filter Circuit (for cores)

The AV_{DD}_SRDS*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 52. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS*n* should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the SV_{DD} power plan.

20.2.2 PLL Power Supply Sequencing

Figure 3 illustrates the order of power up. The order of power up is as follows:

1. $O/L/T/HV_{DD}$
2. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core*n*, AV_{DD}_Core*n*, AV_{DD}_LB, SV_{DD}, XV_{DD}_SRDS*n*, AV_{DD}_SRDS*n* (This rail must reach 90% of its value before the rail for D*n*_GV_{DD}, and Dn_MV_{REF} reaches 10% of its value)
3. D*n*_GV_{DD}, D*n*_MV_{REF}
4. SYSCLK

The order of power down is as follows:

1. SYSCLK (Not sure if SYSCLK matters during power down)
2. D*n*_GV_{DD}, D*n*_MV_{REF}
3. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core*n*, AV_{DD}_Core*n*, AV_{DD}_LB, SV_{DD}, XV_{DD}_SRDS*n*, AV_{DD}_SRDS*n*

4. O/L/T/HV_{DD}

NOTE

The power supplies may power down simultaneously, if the preservation of DDR*n* memory is not a concern.

AV_{DD} type supplies must be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 20.2.1, "PLL Power Supply Filtering".

20.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8641 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each OV_{DD}, D*n*_GV_{DD}, LV_{DD}, TV_{DD}, V_{DD}_Core*n*, and V_{DD}_PLAT pin of the device. These decoupling capacitors should receive their power from separate OV_{DD}, D*n*_GV_{DD}, LV_{DD}, TV_{DD}, V_{DD}_Core*n*, and V_{DD}_PLAT and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the OV_{DD}, D*n*_GV_{DD}, LV_{DD}, TV_{DD}, V_{DD}_Core*n*, and V_{DD}_PLAT planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

20.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}_SRDS*n*) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.

- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

20.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to OV_{DD}, D*n*_GV_{DD}, LV_{DD}, TV_{DD}, V_{DD}_Core*n*, and V_{DD}_PLAT, XV_{DD}_SRDS*n*, and SV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. The exception for this is in the case of PCI Express, unused inputs may be left floating. Power and ground connections must be made to all external OV_{DD}, D*n*_GV_{DD}, LV_{DD}, TV_{DD}, V_{DD}_Core*n*, and V_{DD}_PLAT, XV_{DD}_SRDS*n*, and SV_{DD} and GND pins of the device.

20.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8641 requires weak pull-up resistors (2–10 kΩ is recommended) on all open drain type pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 54. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/$\overline{\text{LSDWE}}$, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull up resistors (100Ω –1 kΩ) to OV_{DD}: $\overline{\text{LSSD\_MODE}}$, TEST_MODE[0:3].

The following pins require weak pull up resistors (2–10 kΩ) to their specific power supplies: $\overline{\text{LCS}}$[0:4], $\overline{\text{LCS}}$[5]/$\overline{\text{DMA_DREQ}}$2, $\overline{\text{LCS}}$[6]/$\overline{\text{DMA\_DACK}}$[2], $\overline{\text{LCS}}$[7]/$\overline{\text{DMA\_DDONE}}$[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground: SD1_PLL_TPA, SD1_DLL_TPA, SD2_PLL_TPA, SD2_DLL_TPA. The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

TSEC*n*_TX_EN signals require an external 4.7-kΩ resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset. TSEC2_TXD[4] and TSEC2_TX_ER pins function as cfg_dram_type[0 or 1] at reset and MUST BE VALID AT POWER-UP, EVEN BEFORE HRESET ASSERTION.

For other pin pull-up or pull-down recommendations of signals, please see Section 17, “Signal Listings.”

20.7 Output Buffer DC Impedance

The MPC8641 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 53). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

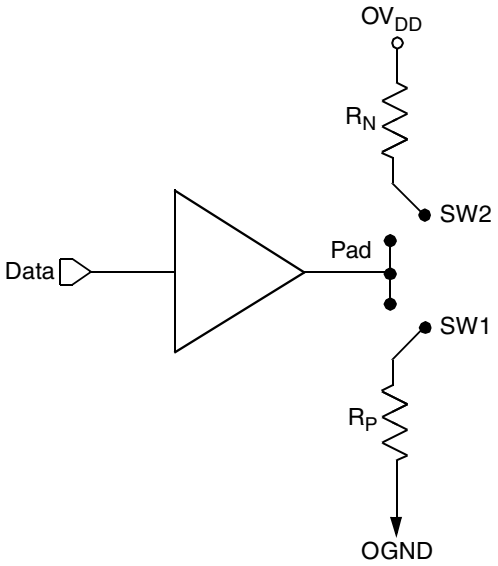


Figure 53. Driver Impedance Measurement

Table 69 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 69. Impedance Characteristics

Impedance	DUART, Control, Configuration, Power Management	PCI Express	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table , T_j = 105°C.

20.8 Configuration Pin Muxing

The MPC8641 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET (and for platform /system clocks after HRESET deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

20.9 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert TRST during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

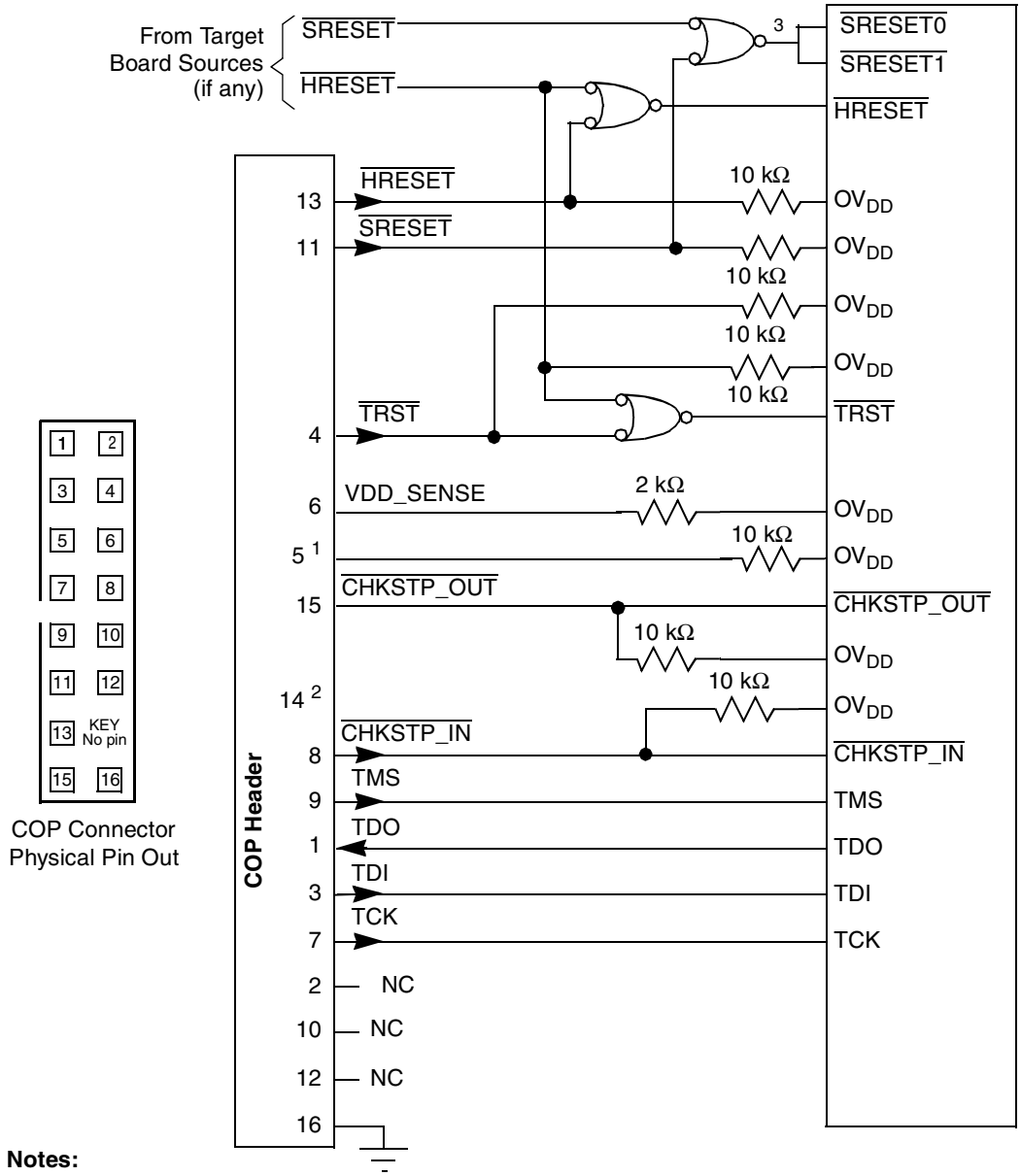
The arrangement shown in Figure 54 allows the COP to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well. If the JTAG interface and COP header will not be used, TRST should be tied to HRESET so that it is asserted when the system reset signal (HRESET) is asserted.

The COP header shown in Figure 54 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 54; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then

left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 54 is common to all known emulators.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Use a NOR gate with sufficient drive strength to drive two inputs.

Figure 54. JTAG Interface Connection

20.10 Guideline for LBIU Parity Temination

In LBIU parity pins are not used. Here is the termination recommendation:

For LDP[0:3]: tie them to ground or the power supply rail via a 4.7K resistor.

For LPBSE: tie it to the power supply rail via a 4.7K resistor (pull-up resistor).

21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, “Part Numbers Fully Addressed by This Document.”

21.1 Part Numbers Fully Addressed by This Document

Table 70 provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 70. Part Numbering Nomenclature

MC	nnnn	x	xx	nnnn	x	x
Product Code	**Part Identifier**	**Core Count**	**Package [1]**	**Core Processor Frequency [2] (MHz)**	**DDR speed (MHz)**	**Product Revision Level**
MC	8641	Blank = Single Core D = Dual Core	HU = HCTE FC-CBGA VU = RoHS HCTE FC-CBGA	1000, 1250, 1333, 1500	K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision C = 2.1 System version ID for Rev C: 0x8090_0021 - MPC8641 0x8090_0121 - MPC8641D

Notes:

1. See Section 16, “Package,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies. Note that core processor speed of 1500 MHz is only available for the MPC8641D (dual core).
3. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes

Table 71 shows the parts that are available for ordering and their operating conditions.

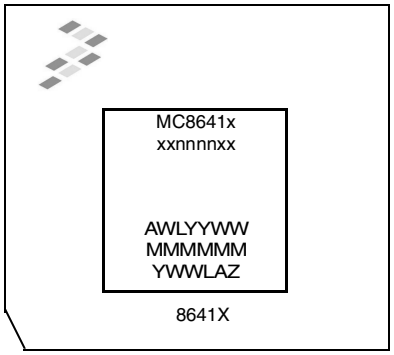
Table 71. Part Offerings and Operating Conditions

Part Offerings [1]	Operating Conditions
MC8641Dxx1500KX	Dual core Max CPU speed = 1500 MHz, Max DDR = 600 MHz Core Voltage = 1.1 volts
MC8641Dxx1333JX	Dual core Max CPU speed = 1333 MHz, Max DDR = 533 MHz Core Voltage = 1.05 volts
MC8641Dxx1250HX	Dual core Max CPU speed = 1250 MHz, Max DDR = 500 MHz Core Voltage = 1.05 volts
MC8641Dxx1000GX	Dual core Max CPU speed = 1000 MHz, Max DDR = 400 MHz Core Voltage = 1.05 volts
MC8641xx1333JX	Single core Max CPU speed = 1333 MHz, Max DDR = 533 MHz Core Voltage = 1.05 volts
MC8641xx1250HX	Single core Max CPU speed = 1250 MHz, Max DDR = 500 MHz Core Voltage = 1.05 volts
MC8641xx1000HX	Single core Max CPU speed = 1000 MHz, Max DDR = 400 MHz Core Voltage = 1.05 volts

1 Note that the xx in the part marking represents the package option. The upper case “X” represents the revision letter. For more information see Table 70.

21.2 Part Marking

Parts are marked as the example shown in Figure 55.



NOTE:
AWLYYWWV is the test code
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

Figure 55. Part Marking for FC-CBGA Device

22 Document Revision History

Table 72 provides a revision history for the MPC8641Dhardware specification.

Table 72. Document Revision History

Revision	Date	Substantive Change(s)
G	3/06	• Section 2.1, "Overall DC Electrical Characteristics" • - Added D*n*_ prefix to MV_{IN} in absolute maximum ratings and recommended operating condition • tables • - Added notes to distinguish voltage differences for DDR1 and DDR2. • - Added notes to distinguish voltage differences for various eTsec protocols. • - Lowered the minimum value from GND to -0.3 for D*n*_MV_{IN} and D*n*_MV_{REF}. • - Increased the range of D*n*_MV_{REF} for absolute ratings table. • - Change the recommended operating conidiotn value for D*n*_MV_{REF}. • - Added power characteristics information for the driver impedance section. • Section 2.2, "Power Sequencing" • - Updated Note regarding power down sequence regarding possible simultaneous power down. • Section 3, "Power Characteristics" • - Included power numbers and updated relevant notes. • - Added (est) statement next to every number to emphasize numbers are estimates. • Section 8.2.1, "FIFO AC Specifications" • - Added sentence regarding FIFO to platform frequency limitation. • Section 17, "Signal Listings" • - Added note for EC*n*_GTX_CLK125. Changed power supply for EC2_GTX_CLK125 from LV_{DD} • to TV_{DD}. • - Added note for platform to FIFO speed limitation. • Section 18.4.2, "Platform to FIFO restrictions" • - Added section on platform to FIFO frequency limitation. • Section 20, "System Design Information • - Added clarity on unused inputs left floating for PCI Express.

Table 72. Document Revision History

Revision	Date	Substantive Change(s)
F	2/1/2006	• Section 2, “Electrical Characteristics” - Updated Power data to “TBD,” pending more data • Section 4, “Input Clocks” • Table 9 - Updated RMII and RTBI duty cycle information to be 1000Base-T specific. Added sentence to note 2 regarding the 10Base-T and 100Base-T duty cycles. Added note 2 to Table 9 (was in Table 34) • Section 8, “Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management” • - Removed duty cycle information for GMII, TBI transmit and 1000Base -T GTX_CLK specifications since they are covered in Section 4.3, “eTSEC Gigabit Reference Clock Timing” • - Moved note 4 superscript to row on 10base and 100 base duty cycle. • - Table 20: changed RX_CLK duty cycle symbol from t_{FIRH} to t_{FIRH}/t_{FIRH} • - Figure 17: modified t_{SKTRX} start point • - Table 30 moved note 7 to be note 2 of Table 9 • Section 10, “Local Bus” • - Table 42: Changed Max value of $t_{LBKHOV2}$ from 2.0 to 2.2 • - Table 43: Changed Max value of $t_{LBKHOV2}$ from 2.1 to 2.3 • - Figure 25: Added note before figure • - Figure 25: Replaced figure • - Added Table 45 • Section 13, “High-Speed Interfaces” • - Added Figure 36, “Driver and Receiver of SerDes SD_REF_CLK/SD_REF_CLK” • - Added Section 13.2, “Spread Spectrum Clock,”“ subsection.
E	11/2005	• Updated all TBDs in document • Section 2, “Electrical Characteristics” - Removed Note preceding Tables 1 and 2. Updated DC voltage numbers for core, platform, and SerDes. Separated XV_{DD} to XV_{DD}_SRDS1 and XV_{DD}_SRDS2. Updated notes in Tables 1 and 2. Updated impedance drive strength info for various functional blocks. Added a Power Sequencing section. • - Added Power data. • Section 4, “Input Clocks” - Renamed section and updated relevant input clock sections. • Section 5, “RESET Initialization” - Removed row for e600 PLL as the specification applies to PLL lock time. The PLL lock times table has been defined to apply to platform and e600 PLL. Section 6, “DDR and DDR2 SDRAM” Replaced specifications for 667 MHz characteristics with that of the specifications for 600 MHz since maximum DDR frequency supported is changed to 600 MHz. Removed following sentence from first paragraph of section since it is not a true statement as specs vary for DDR1 and DDR2: “The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.” Changed (n) to [n] throughout document. Pulled out note from Table 20 and highlighted it as note so that customers are aware of 1/2 clock requirement for spec.

Table 72. Document Revision History

Revision	Date	Substantive Change(s)
E	11/2005	• Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management" - Added reference about FIFO to platform frequency restriction info. • Section 9.2, "MII Management AC Electrical Specifications" - Changed t_{plbclk} to t_{MPX} since the latter name is more applicable to MPX clock. • Section 10, "Local Bus" - Added sentence to reference clocking section on frequency range of local bus. • Section 14, "PCI Express" Added note refarding REFCLK and PCI Express specification. • Section 16, "Package" Updated Packaging information and Mechanical drawings. Note that CLGA package will no longer be supported. • Section 17, "Signal Listings" - Updated note contents and numbering. Added new reset configuration signals. Main changes include: • - Changed "I/O" pin status to "O" only for MDM[0:7] since FCRAM memory will not be supported. • - Increased resistor range for MDIC[0] resist requirements. • - Removed note regarding ECC on FCRAM for MDM signals since FCRAM is no longer • supported. • - Moved note regarding LVDS type pins to heading of section instead of next to each signal row. • - Added notes regarding TPD and TPA type pin definitions and resistor requirements. • - Added notes to highlight SRIO data transmit and receive pins • - Increased resistor range for some SerDes reserved pins with 300 ohm pull down resistor requirement. • - Removed pull down requirement on TSEC*n*_GTX_CLK signals. • - Changed note pull up requirement for TSEC*n*_TX_EN to a pull down with explanation. • - Added note to TSEC*n*_CRS signals regarding FIFO mode • - Added reset warning note for LGPL[0:1] signals • - Removed note concerning thermal anode and cathode signals in Rev 1.0 silicon since it is addressed in the chip errata document. • - Changed signal name from AUX_CLK_OUT/IRQ[8] to IRQ[8] and kept it only in the PIC section instead of both Clocking and PIC sections. • - Moved $\overline{\text{SMI\_0}}$ and $\overline{\text{SMI\_1}}$ from the PIC section to the System Control section, • - Added the following signals as new reset configuration signals: TSEC1_TXD[0], • TSEC3_TXD[0:2], and TSEC4_TXD[4]. • - Added requirement for cfg_dram_type[0:1] pins. • - Changed name of *cfg_port_div* reset signal to cfg_platform_freq and updated note description • - Updated note contents and numbering. Added new reset configuration signals. • - Removed reset warning notes for D1_MSRCID[0:1, 3:4], D2_MSRCID[0:4], MDVAL_1/LB_DVAL, and ASLEEP. • - Rearranged order of reset configuration signals. • - Changed reset config name from *cfg_core1_trans_enbl* to $\overline{\text{cfg\_core1\_lm\_offset}}$. • - Separated XVDD to XVDD_SRDS1 and XVDD_SRDS2 pin groups. • - Changed config name from cfg_core1_trans_enbl to cfg_core1_lm_offset • Section 18, "Clocking" - Added a section on local bus frequency range. Added a section on FIFO to platform frequency restrictions. removed references to 1667 MHz, since it is not supported. Added note regarding platform range not working between 400 and 500 MHz. • Section 19, "Thermal" - Updated data in Heat Sink Example. Removed the "-1" from equation for Ideality factor (V_H-V_L). Added number for Ideality factor. • Section 20, "System Design Information" - Updated Connection, Pull-up and Pull down recommendations sections to be consistent with notes of Signals Listings section. Removed jumper from JTAG Cop connection drawing. Removed references to SV_{DD} and XV_{DD} in the decoupling recommendations sections since they are being addressed in the SerDes Power section. • Section 21, "Ordering Information" Updated ordering information to reflect new part numbering scheme and packaging information. Updated Part marking drawing.

Table 72. Document Revision History

Revision	Date	Substantive Change(s)
D	9/15/05	Major updates were made to the content of the following sections including changes in nomenclature and values of some characteristics: Section 1, "Overview," Combined figures 1 and 2 to one figure for the block diagram of both MPC8641 and MPC8641D. Section 2, "Electrical Characteristics," Updated wording for some characterictics of Tables 1 & 2. Removed 1.0 volt rail from the SV_{DD} supply list. Added cautions to the notes section of Table 2. Added some minor wording changes through remainder of section. Power-Up sequencing information Section 2.2 has been updated as well. Section 3, "Power Characteristics. " Removed row for core at 1800 MHz for the 400 MHz platform. As this is not an option offered currently. Section 4, "Input Clocks," Updated the SYCLK jitter spec from +/- 150 ps for maximum to 150 ps. Section 5, "RESET Initialization," Added row for e600 PLLs for Reset initilization table. Added note to table. Section 6, "DDR and DDR2 SDRAM, " Updated wording relevant to DDR verses DDR2 throughput document. Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management," Corrected relevant voltage supplies throughout section. Section 8.2.7, "RMII AC Timing Specifications," Removed minimum and maximum specs for REF_CLK period in table for RMII Transmit AC Timing. Section 9, "Ethernet Management Interface Electrical Characteristics," Updated voltage specs to be correct value. Section 15, "Serial RapidIO," Removed 10 ns from typical listing for REFCLK cycle time. Section 16, "Package" Updated packaging specs and mechanical drawings. Section 17, "Signal Listings," Added pin assignments and notes for signals. Updated SerDes Reserved pins section. Section 18.3, "e600 to MPX clock PLL Ratio," Updated signals used for PLL ratios in table for e600 core to MPX Clock ratio. Updated Table for SYSCLK to Platform/MPX clock speed. Section 19, "Thermal," Added values to table on Package Thermal Characteristics. Updated and Added listing for Heat Sink vendors. Added entries into table for Recommended Thermal Model. Section 20, "System Design Information," Updated and added Power Supply Filter Circuits. Added "*n*" to $\overline{\text{SRESET}}$ on part in Figure 54 show availability of multiple $\overline{\text{SRESET}}$s on the part. Section 21, "Ordering Information" - Updated Part Marking information and drawing. Added section on part number specifications document for N-spec part.
C	5/31/05	Major updates were made to the content of the following sections including changes in nomenclature and values of some characteristics: Section 1, "Overview" Section 2, "Electrical Characteristics" Section 10, "Local Bus" Section 14, "PCI Express" Section 16, "Package" Section 17, "Signal Listings" Section 18, "Clocking" Section 19, "Thermal" Section 20, "System Design Information" Minor edits were made to other sections.
B	12/22/04	Preliminary revision, updated Table , Table 2, and Table 5.
A	11/07/04	Initial document.

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