

74LVT162245 • 74LVTH162245

Low Voltage 16-Bit Transceiver with 3-STATE Outputs and 25Ω Series Resistors in A Port Outputs

General Description

The LVT162245 and LVTH162245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The T/R inputs determine the direction of data flow through the device. The OE inputs disable both the A and B ports by placing them in a high impedance state.

The LVT162245 and LVTH162245 are designed with equivalent 25Ω series resistance in both the HIGH and LOW states on the A Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162245 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These non-inverting transceivers are designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162245 and LVTH162245 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH162245), also available without bushold feature (74LVT162245).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- A Port outputs include equivalent series resistance of 25Ω making external termination resistors unnecessary and reducing overshoot and undershoot
- A Port outputs source/sink ±12 mA.
B Port outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 162245
- Latch-up performance exceeds 500 mA
- ESD performance:
Human-body model > 2000V
Machine model > 200V
Charged-device model > 1000V
- Also packaged in plastic Fine Pitch Ball Grid Array (FBGA)

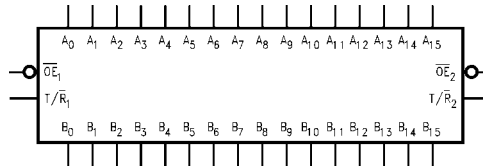
Ordering Code:

Order Number	Package Number	Package Description
74LVT162245G (Note 1)(Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVT162245MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT162245MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH162245G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH162245MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TUBE]
74LVTH162245MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LVTH162245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBE]
74LVTH162245MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

Note 1: Ordering code "G" indicates Trays.

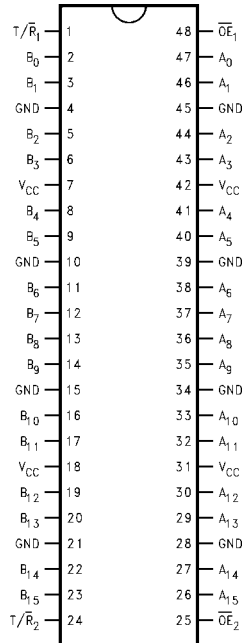
Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

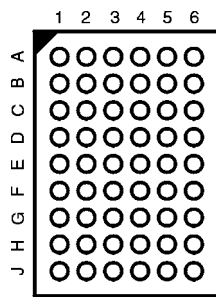


Connection Diagrams

Pin Assignments for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
T/\overline{R}_n	Transmit/Receive Input
A ₀ -A ₁₅	Side A Inputs/3-STATE Outputs
B ₀ -B ₁₅	Side B Inputs/3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	B ₀	NC	T/\overline{R}_1	\overline{OE}_1	NC	A ₀
B	B ₂	B ₁	NC	NC	A ₁	A ₂
C	B ₄	B ₃	V _{CC}	V _{CC}	A ₃	A ₄
D	B ₆	B ₅	GND	GND	A ₅	A ₆
E	B ₈	B ₇	GND	GND	A ₇	A ₈
F	B ₁₀	B ₉	GND	GND	A ₉	A ₁₀
G	B ₁₂	B ₁₁	V _{CC}	V _{CC}	A ₁₁	A ₁₂
H	B ₁₄	B ₁₃	NC	NC	A ₁₃	A ₁₄
J	B ₁₅	NC	T/\overline{R}_2	\overline{OE}_2	NC	A ₁₅

Truth Tables

Inputs		Outputs
\overline{OE}_1	T/\overline{R}_1	
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	H	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
H	X	HIGH-Z State on A ₀ -A ₇ , B ₀ -B ₇

Inputs		Outputs
\overline{OE}_2	T/\overline{R}_2	
L	L	Bus B ₈ -B ₁₅ Data to Bus A ₈ -A ₁₅
L	H	Bus A ₈ -A ₁₅ Data to Bus B ₈ -B ₁₅
H	X	HIGH-Z State on A ₈ -A ₁₅ , B ₈ -B ₁₅

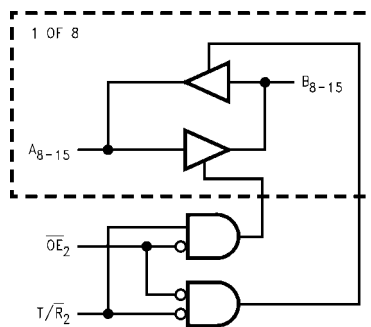
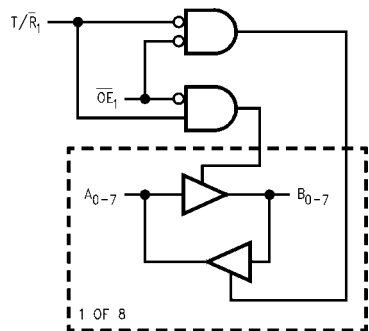
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Functional Description

The LVT162245 and LVTH162245 contain sixteen non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identi-

cally, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	-0.5 to +4.6		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	-50	$V_I < \text{GND}$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	± 64		mA
I_{GND}	DC Ground Current per Ground Pin	± 128		mA
T_{STG}	Storage Temperature	-65 to +150		$^{\circ}\text{C}$

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current	B Port	-32	mA
		A Port	-12	
I_{OL}	LOW-Level Output Current	B Port	64	mA
		A Port	12	
T_A	Free Air Operating Temperature	-40	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8\text{V}-2.0\text{V}$, $V_{CC} = 3.0\text{V}$	0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		Units	Conditions
			Min	Max		
V_{IK}	Input Clamp Diode Voltage	2.7		-1.2	V	$I_I = -18\text{ mA}$
V_{IH}	Input HIGH Voltage	2.7-3.6	2.0		V	$V_O \leq 0.1\text{V}$ or $V_O \geq V_{CC} - 0.1\text{V}$
V_{IL}	Input LOW Voltage	2.7-3.6		0.8	V	
V_{OH}	Output HIGH Voltage	A Port	3.0	2.0	V	$I_{OH} = -12\text{ mA}$
			2.7-3.6	$V_{CC}-0.2$	V	$I_{OH} = -100\ \mu\text{A}$
		B Port	2.7	2.4	V	$I_{OH} = -8\text{ mA}$
			3.0	2.0	V	$I_{OH} = -32\text{ mA}$
V_{OL}	Output LOW Voltage	A Port	3.0	0.8	V	$I_{OL} = 12\text{ mA}$
			2.7	0.2	V	$I_{OL} = 100\ \mu\text{A}$
		B Port	2.7	0.5	V	$I_{OL} = 24\text{ mA}$
			3.0	0.4		$I_{OL} = 16\text{ mA}$
			3.0	0.5		$I_{OL} = 32\text{ mA}$
			3.0	0.55		$I_{OL} = 64\text{ mA}$
$I_{I(HOLD)}$ (Note 5)	Bushold Input Minimum Drive	3.0	75		μA	$V_I = 0.8\text{V}$
			-75			$V_I = 2.0\text{V}$
$I_{I(OD)}$ (Note 5)	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 6)
			-500			(Note 7)
I_I	Input Current	3.6		10	μA	$V_I = 5.5\text{V}$
		Control Pins	3.6	± 1		$V_I = 0\text{V}$ or V_{CC}
		Data Pins	3.6	-5		$V_I = 0\text{V}$
I_{OFF}	Power Off Leakage Current	0		1	μA	$V_I = V_{CC}$
				± 100		$0\text{V} \leq V_I$ or $V_O \leq 5.5\text{V}$

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions
			Min	Max		
I _{PU/PD}	Power Up/Down 3-STATE Current	0–1.5V		±100	μA	V _O = 0.5V to 3.0V V _I = GND to V _{CC}
I _{OZL}	3-STATE Output Leakage Current	3.6		-5	μA	V _O = 0.5V
I _{OZL} (Note 5)	3-STATE Output Leakage Current	3.6		-5	μA	V _O = 0.0V
I _{OZH}	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.0V
I _{OZH} (Note 5)	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.6V
I _{OZH} ⁺	3-STATE Output Leakage Current	3.6		10	μA	V _{CC} < V _O ≤ 5.5V
I _{CCH}	Power Supply Current	3.6		0.19	mA	Outputs HIGH
I _{CCL}	Power Supply Current	3.6		5	mA	Outputs LOW
I _{CCZ}	Power Supply Current	3.6		0.19	mA	Outputs Disabled
I _{CCZ} ⁺	Power Supply Current	3.6		0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled
ΔI _{CC}	Increase in Power Supply Current (Note 8)	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND

Note 5: Applies to Bushold versions only (74LVTH162245).

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 8: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 9)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 10)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 10)

Note 9: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 10: Max number of outputs defined as (n), n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C C _L = 50 pF, R _L = 500Ω				Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Data to A Port Output	1.0	4.0	1.0	4.6	ns
t _{PHL}		1.0	3.7	1.0	4.1	
t _{PLH}	Propagation Delay Data to B Port Output	1.0	3.5	1.0	3.9	ns
t _{PHL}		1.0	3.5	1.0	3.9	
t _{PZH}	Output Enable Time for A Port Output	1.0	5.3	1.0	6.3	ns
t _{PZL}		1.0	5.6	1.0	7.2	
t _{PZH}	Output Enable Time for B Port Output	1.0	4.6	1.0	5.4	ns
t _{PZL}		1.0	5.3	1.0	6.9	
t _{PHZ}	Output Disable Time for A Port Output	1.5	5.6	1.5	6.3	ns
t _{PLZ}		1.5	5.5	1.5	5.5	
t _{PHZ}	Output Disable Time for B Port Output	1.5	5.4	1.5	6.1	ns
t _{PLZ}		1.5	5.1	1.5	5.4	
t _{OSSL}	A Port Output to Output Skew (Note 11)		1.0		1.0	ns
t _{OSLH}						
t _{OSSL}	B Port Output to Output Skew (Note 11)		1.0		1.0	ns
t _{OSLH}						

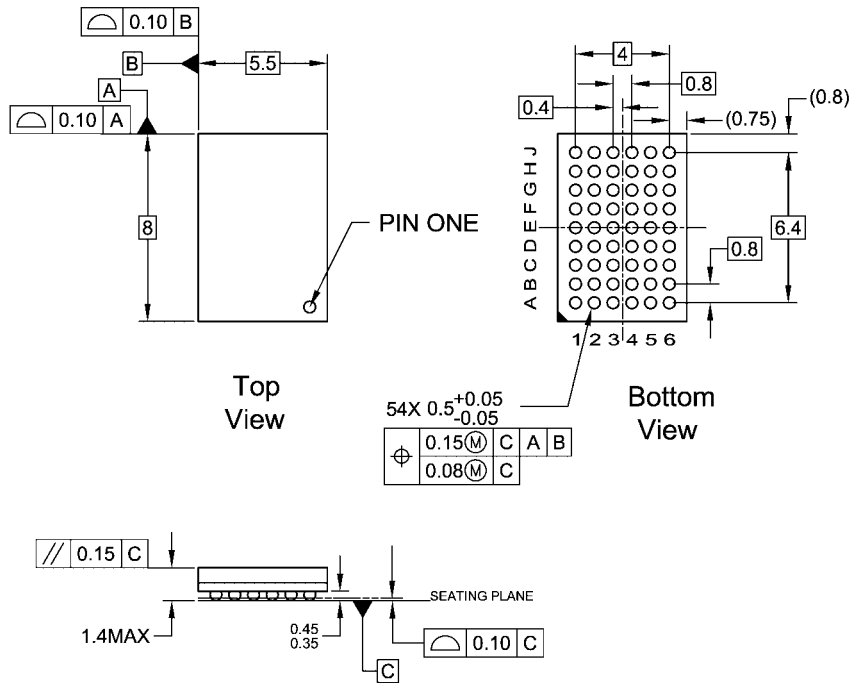
Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 12)

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 0V, V _I = 0V or V _{CC}	4	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



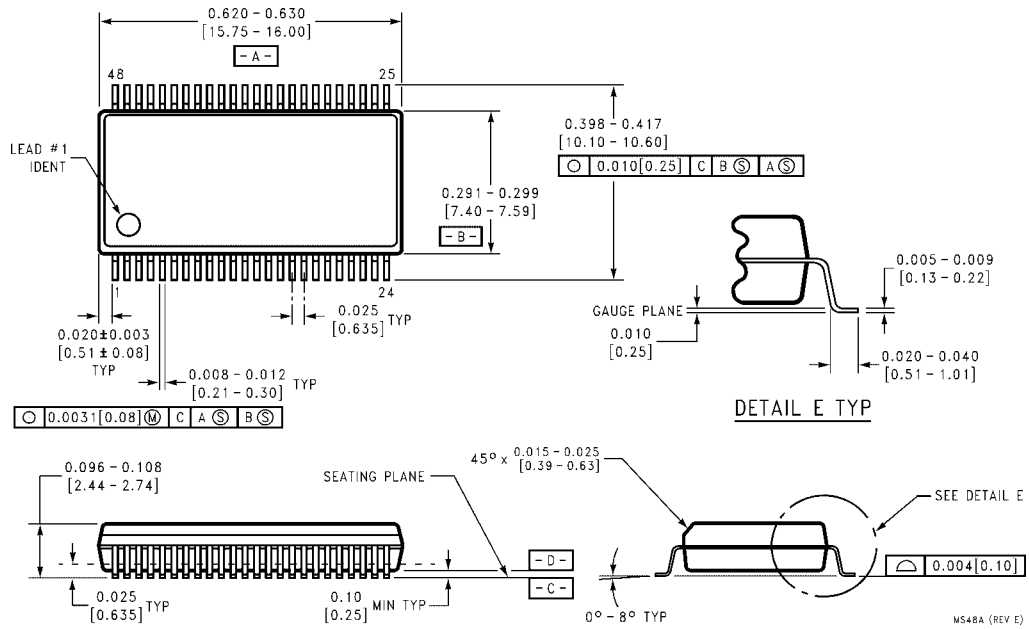
NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

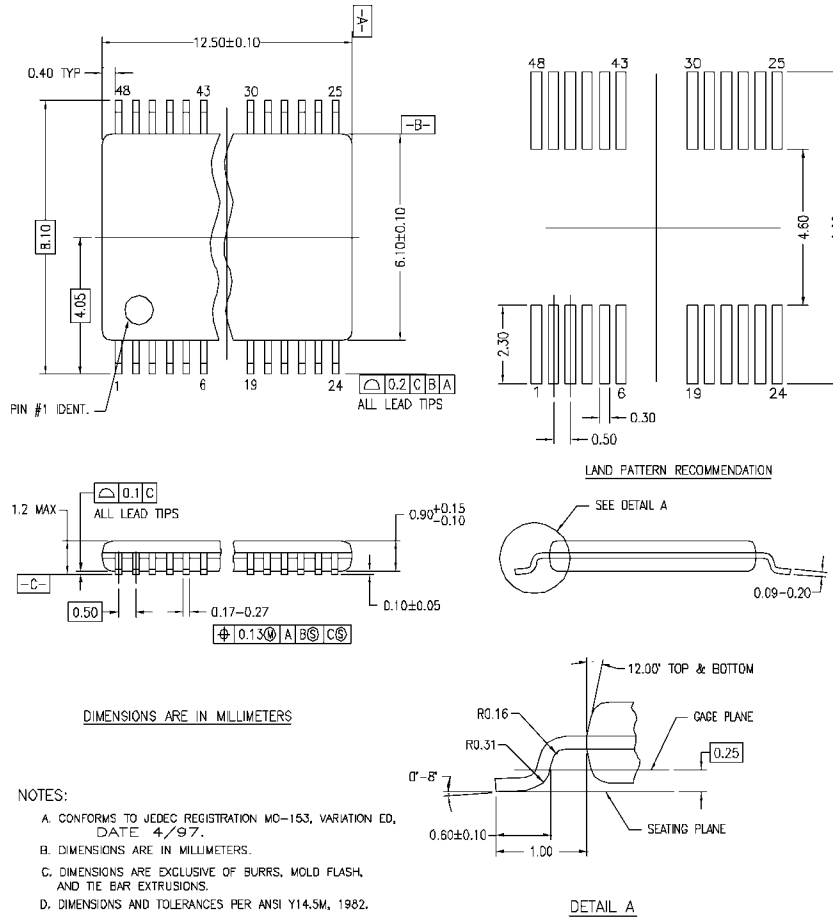
**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide
Package Number BGA54A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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