

74F564 Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The 'F564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}). The information presented to the D inputs is sorted in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'F574, but has inverted outputs.

Features

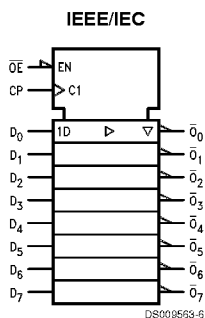
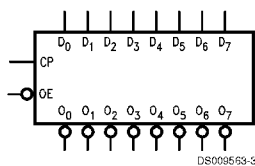
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'F574
- 3-STATE outputs for bus-oriented applications

Ordering Code:

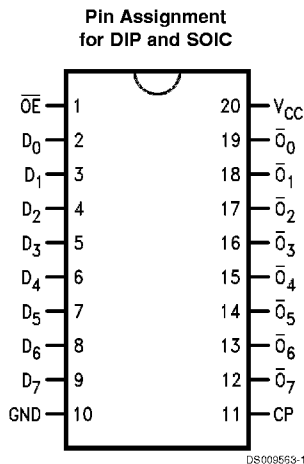
Commercial	Package Number	Package Description
74F564PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F564SJ (Note 1)	M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SJX.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_7	Data Inputs	1.0/1.0	20 μA /-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA /-0.6 mA
\overline{OE}	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA /-0.6 mA
$\overline{O}_0-\overline{O}_7$	3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

Functional Description

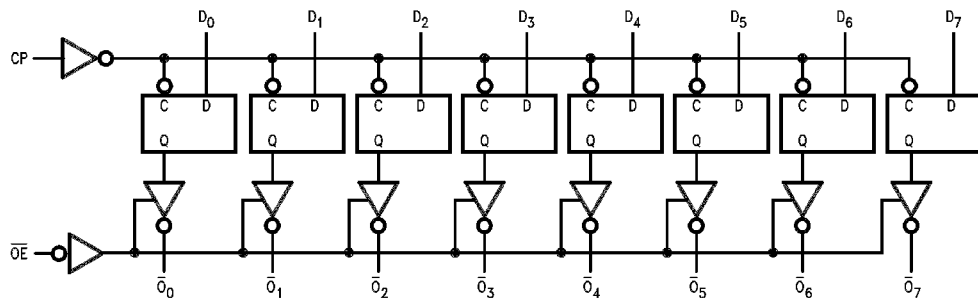
The 'F564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H		L	H	Z	Load
H		H	L	Z	Load
L		L	H	H	Data Available
L		H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	

in LOW State (Max)

twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage					V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage					V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC}	2.5		V	Min		I _{OH} = -1 mA
		74F 10% V _{CC}	2.4					I _{OH} = -3 mA
		74F% 5% V _{CC}	2.7					I _{OH} = -1 mA
		74F% 5% V _{CC}	2.7					I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	74F 10% V _{CC}			V	Min	I _{OL} = 24 mA	
I _{IH}	Input HIGH Current	74F			μA	Max	V _{IN} = 2.7V	
I _{BVI}	Input HIGH Current Breakdown Test	74F			μA	Max	V _{IN} = 7.0V	
I _{CEX}	Output HIGH Leakage Current	74F			μA	Max	V _{OUT} = V _{CC}	
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded	
I _{OD}	Output Leakage Circuit Current	74F			μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded	
I _{IL}	Input LOW Current				mA	Max	V _{IN} = 0.5V	
I _{OZH}	Output Leakage Current		50		μA	Max	V _{OUT} = 2.7V	
I _{OZL}	Output Leakage Current		-50		μA	Max	V _{OUT} = 0.5V	
I _{OS}	Output Short-Circuit Current		-60 -150		mA	Max	V _{OUT} = 0V	
I _{ZZ}	Bus Drainage Test		500		μA	0.0V	V _{OUT} = 5.25V	
I _{CCZ}	Power Supply Current		55 86		mA	Max	V _O = HIGH Z	

AC Electrical Characteristics

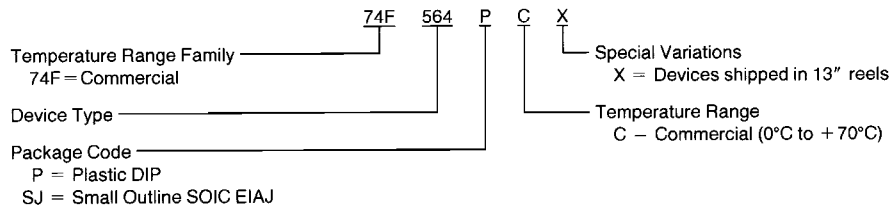
Symbol	Parameter	74F			74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100			70		MHz
t_{PLH}	Propagation Delay	2.5	5.2	8.5	2.5	8.5	ns
t_{PHL}	CP to \overline{O}_n	2.5	5.9	8.5	2.5	8.5	
t_{PZH}	Output Enable Time	3.0	5.6	9.0	2.5	10.0	ns
t_{PZL}		3.0	6.2	9.0	2.5	10.0	
t_{PHZ}	Output Disable Time	1.5	3.4	5.5	1.5	6.5	
t_{PLZ}		1.5	2.7	5.5	1.5	6.5	

AC Operating Requirements

Symbol	Parameter	74F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	
$t_{\text{s}}(\text{H})$	Setup Time, HIGH or LOW	2.0		2.0		ns
$t_{\text{s}}(\text{L})$	D_n to CP	2.5		2.5		
$t_{\text{h}}(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		ns
$t_{\text{h}}(\text{L})$	D_n to CP	2.0		2.0		
$t_{\text{w}}(\text{H})$	CP Pulse Width	5.0		5.0		ns
$t_{\text{w}}(\text{L})$	HIGH or LOW	5.0		5.0		

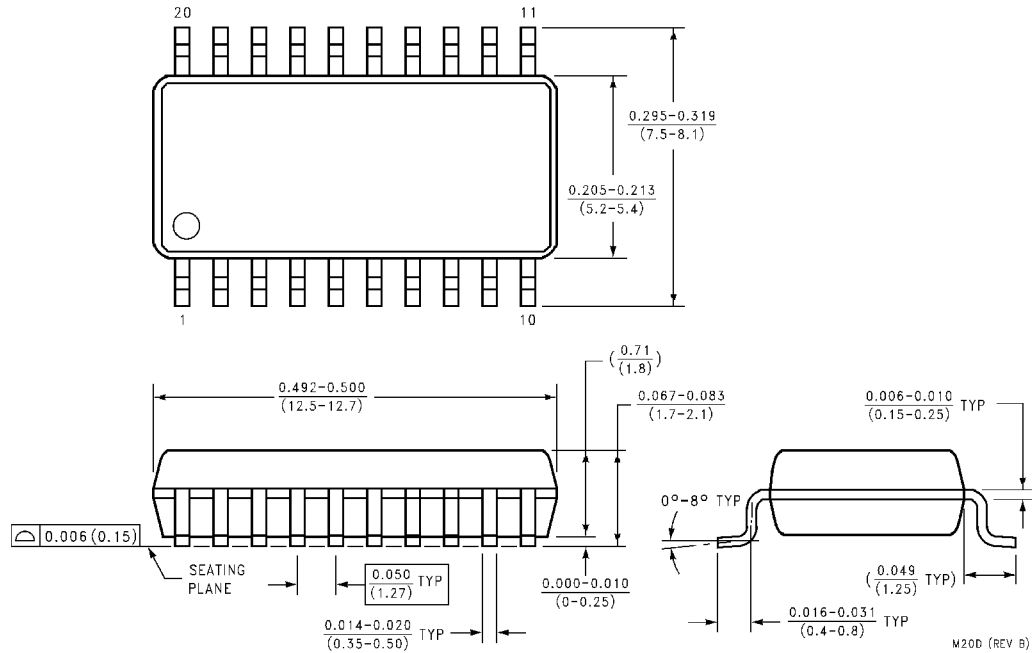
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

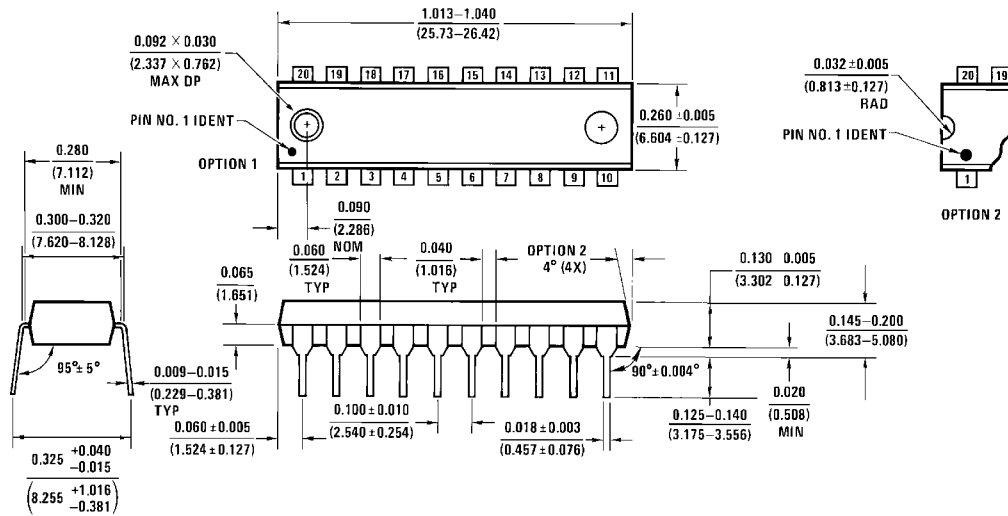


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Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number M20D**



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N20A**

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Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

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