3 to 5 Serial Cell Li-Ion or Li-Polymer Battery Protection IC

NO.EA-322-190422

OUTLINE

The R5436T is an overcharge, overdischarge and overcurrent protection IC for Li-ion or Li-polymer secondary battery. Overcharge, Overdischarge, Charge Overcurrent and Discharge Overcurrent for 3 to 5 serial cells can be detected. By cascade connection using the R5436T, it is also possible to protect 6-serial or more cells rechargeable battery pack. The R5436T provides a cell-balancing function to equalize imbalance between cells, and it provides an open-wire detection to detect a broken wire between a battery and the circuit board. The open-wire detection is optionally selectable.

FEATURES

- High Voltage Tolerant Process
  - Absolute Maximum Ratings ·····30 V
- Low Supply Current
  - Normal operation with using 5 cells ·····Typ. 12.0 µA
  - Standby ·····Typ. 6.0 µA
- High-accuracy Voltage Detection
  - Overcharge detection voltage (V_{DET1n}[(1)]) ·····3.6 V to 4.5 V (in 5 mV steps)
  - Overcharge detection voltage accuracy·····± 0.025 V (Ta = 25°C)
  - Overdischarge detection voltage (V_{DET2n}[(1)]) ·····2.0 V to 3.2 V (in 5 mV steps)
  - Overdischarge detection voltage accuracy·····± 2.5%
  - Discharge overcurrent detection voltage1 (V_{DET31}) [(2)] ·····0.05 V to 0.25 V (in 10 mV steps)
  - Discharge overcurrent detection voltage accuracy·····± 20mV
  - Discharge overcurrent detection voltage2 ·····Three times V_{DET31}
  - Short-circuit detection voltage[(3)]·····0.25 V to 1.0 V (in 20 mV steps)
  - Charge overcurrent detection voltage ·····-0.05 V / -0.1 V / -0.2 V
  - Charge overcurrent detection voltage accuracy·····± 30 mV
  - Overcharge release voltage·····V_{DET1n}–0.1V to V_{DET1n}–0.4V (in 10mV steps)
  - Overdischarge release voltage·····V_{DET2n}+0.0V to V_{DET2n}+0.7V (in 50mV steps) –provided, max.value is 3.2V.
  - Cell-balancing detection voltage (V_{CBDn}[(1)])·····3.45V to 4.45V (in 5 mV steps)
  - Cell-balancing release voltage ·····V_{CBDn}–0.0V to V_{CBDn}–0.4V (in 10mV steps)
- Each Detection DelayTime
  - Overcharge detection delay time ·····1.0 sec
  - Overdischarge detection delay time settable by external capacitor
  - Discharge overcurrent detection delay time 1/2 settable by external capacitor
  - Charge overcurrent detection delay time ·····8 ms
  - Short-circuit detection delay time ·····330 µs
- Zero Voltage Charging·····Available

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(1) V_{DET1n}, V_{CBDn} : n =1, 2, 3, 4, 5

(2) Set to meet the following equation: ($3\times V_{DET31}+0.05<0.8\times V_{SHORT}$).

(3) V_{DET32} is not detected when V_{DET32} is higher than V_{SHORT}.

- Overcharge Release Voltage Condition ····· Voltage release type
- Overdischarge Release Voltage Condition ····· Latch type / Voltage release type
- 3 to 5 Cells Selectable Battery Protection
- Delay Time Shortening Function
- Selectable Broken-wire Detection ····· Typ.1.25 s
- External NTC temperature protection function
- Package ····· TSSOP-28 (JEDEC: 173 MIL)

APPLICATIONS

■ Li-ion/Li-polymer battery protection for electric tool and electric bicycle, etc.

SELECTION GUIDE

In the R5436T, the set voltage, the delay time, and the optional function can be designated.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5436Txxx∗$-E2-FF	TSSOP-28	3,000 pcs	Yes	Yes

xxx: Specify a combination of the following set output voltages. Refer to *Product Code List* for details.

V_{DET1n}[(1)] : 3.6 V to 4.5 V in 5 mV steps
V_{REL1n}[(1)] : V_{DET1n} – 0.1 V to V_{DET1n} – 0.4 V in 10 mV steps
V_{CBDn}[(1)] : 3.45 V to 4.45 V in 5mV steps
V_{CBRn}[(1)] : V_{CBDn} – 0.0 V to V_{CBDn} –0.4 V in 10 mV steps
V_{DET2n}[(1)] : 2.0 V to 3.2 V in 5 mV steps
V_{REL2n}[(1)] : V_{DET2n} + 0.0 V to V_{DET2n} + 0.7 V in 50 mV steps (Max. 3.2 V)
V_{DET31} : 0.05 V to 0.25 V in 10 mV steps
V_{DET32} : Fixed to three times V_{DET31}
V_{SHORT} : 0.25 V to 1.0 V in 20 mV steps
V_{DET4} : -0.05V (±30mV), -0.1V (±30mV), or -0.2V (±30mV)

∗: Specify a combination of the following each detection delay time.

Code	t_{VDET1} (s)	t_{VDET2} (s)	t_{VDET31} (ms)	t_{VDET32} (ms)	t_{VDET4} (ms)	t_{SHORT} (µs)
B	1.0	3.60×C_{CT1} (nF)	3.00×C_{CT2} (nF)	t_{VDET31}/6	8	330

$: Specify a combination of the optional functions.

Code	Overcharge Released Type	Overdischarge Released Type	0 V Charging	Open-wire Detection
A	Voltage Release	Latch	Available	Available
B	Voltage Release	Voltage Release	Available	Unavailable

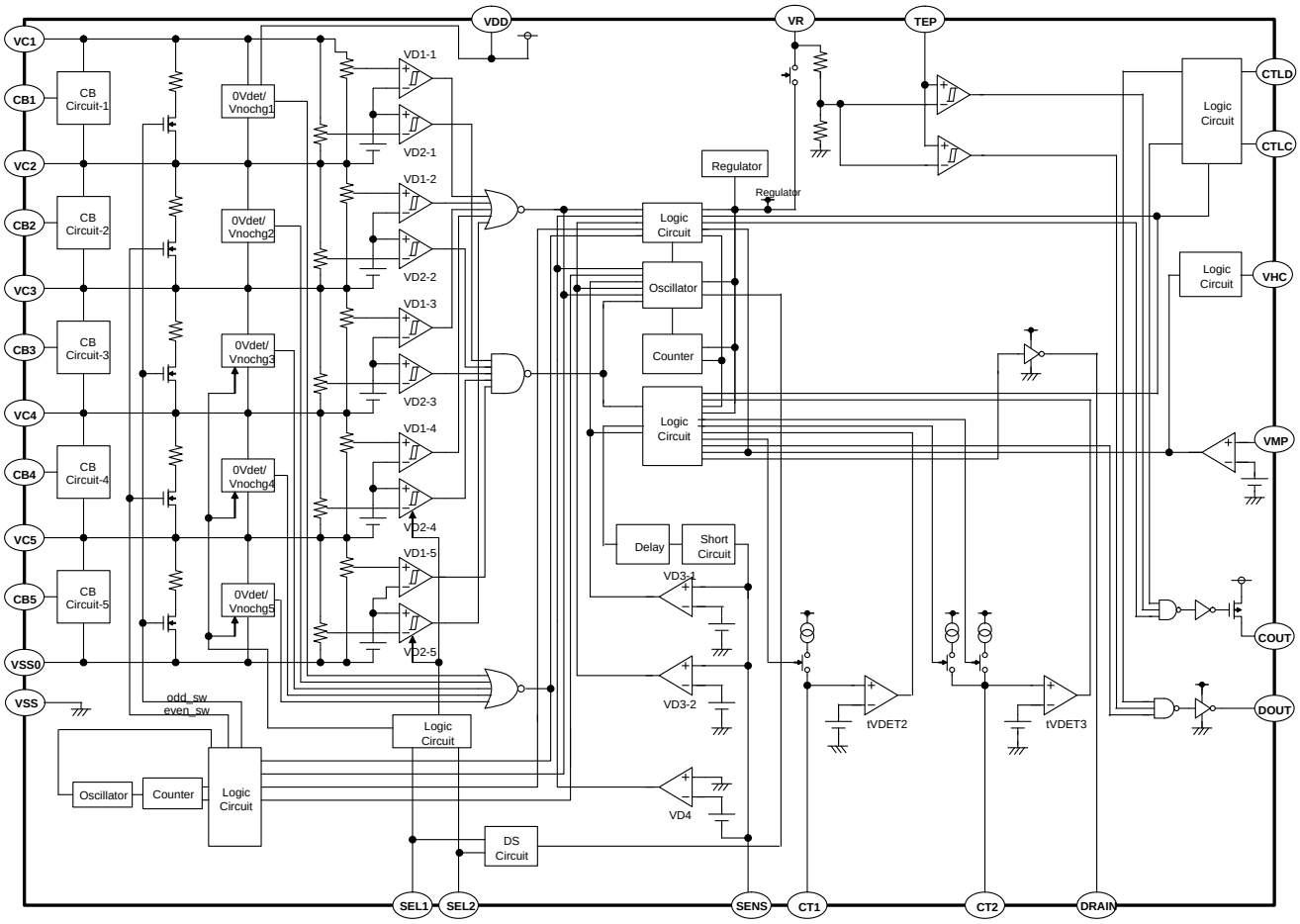
(1) V_{DET1n}, V_{REL1n}, V_{CBDn}, V_{CBRn}, V_{DET2n}, V_{REL2n} : n =1, 2, 3, 4, 5

Product Code List

The product code is determined by the combination of the set output voltages (Overcharge Detection Voltage: V_{DET1n}, Overcharge Release Voltage: V_{REL1n}, Cell-balancing Detection Voltage: V_{CBDn}, Cell-balancing Release Voltage: V_{CBRn}, Overdischarge Detection Voltage: V_{DET2n}, Overdischarge Release Voltage: V_{REL2n}, Discharge Overcurrent Detection Voltage 1/2: V_{DET31} / V_{DET32}, Short-circuit Detection Voltage: V_{SHORT}, Charge Overcurrent Detection Voltage: V_{DET4}), the delay time code, and the optional function code.

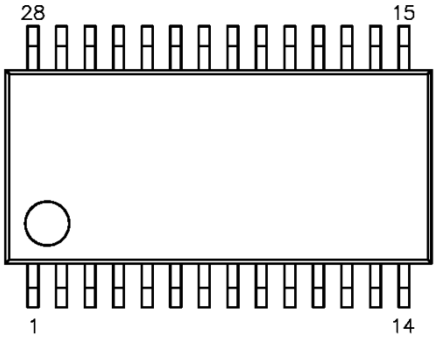
Product Name (Product Code)	Set Output Voltage (V)									
	V_{DET1n}	V_{REL1n}	V_{CBDn}	V_{CBRn}	V_{DET2n}	V_{REL2n}	V_{DET31}	V_{DET32}	V_{SHORT}	V_{DET4}
R5436T**502**BA	4.250	4.100	4.200	4.190	2.500	3.000	0.100	0.300	0.420	-0.050
R5436T**502**BB										
R5436T**503**BA	4.250	4.150	4.200	4.190	2.800	3.200	0.100	0.300	0.420	-0.050
R5436T**503**BB										
R5436T**504**BA	4.280	4.220	4.180	4.170	2.500	3.000	0.100	0.300	0.420	-0.050
R5436T**504**BB										
R5436T**505**BA	3.800	3.500	3.550	3.540	2.200	2.500	0.080	0.240	0.300	–0.050
R5436T**505**BB										
R5436T**506**BA	3.800	3.600	3.600	3.550	2.750	3.000	0.150	0.450	0.450	–0.050
R5436T**507**BA	4.200	4.170	4.160	4.150	2.800	3.000	0.100	0.300	0.420	–0.050
R5436T**508**BA	3.650	3.450	3.550	3.530	2.000	2.500	0.100	0.300	0.420	–0.050
R5436T**508**BB										
R5436T**509**BA	4.350	4.150	4.300	4.290	2.700	3.000	0.100	0.300	0.420	–0.050
R5436T**510**BA	4.250	4.100	4.225	4.215	2.500	3.000	0.100	0.300	0.420	–0.050
R5436T**511**BA	4.250	4.150	4.200	4.190	2.750	3.000	0.080	0.240	0.300	–0.050
R5436T**511**BB										
R5436T**513**BB	4.400	4.250	4.350	4.340	2.700	3.000	0.100	0.300	0.420	-0.050
R5436T**514**BB	4.250	4.150	4.200	4.190	2.150	2.250	0.250	0.750	1.000	-0.200
R5436T**515**BB	3.650	3.450	3.550	3.530	2.300	3.000	0.100	0.300	0.420	-0.050

BLOCK DIAGRAM



R5436T Block Diagram

PIN DESCRIPTIONS



R5436T (TSSOP-28) Pin Configuration

R5436T Pin Description

Pin No.	Symbol	Description
1	CTLC	COUT control pin
2	CTLD	DOUT control pin
3	COUT	Overcharge detection output pin, Pch. open-drain output
4	VMP	Charger negative input pin
5	DRAIN	FET's gate connection pin for discharge overcurrent release voltage
6	DOUT	Overdischarge detection output pin, CMOS output
7	VHC	Transmission pin for VMP input signal
8	SENS	Current sense pin
9	VR	Internal VR output pin
10	TEP	Temperature protection input pin
11	VSS	Ground pin for the IC
12	CT1	Capacitor (C_{CT1}) connection pin for setting t_{VDET2}
13	CT2	Capacitor (C_{CT2}) connection pin for setting t_{VDET3}
14	SEL1	3- / 4- / 5-cell selectable pins
15	SEL2	
16	VSS0	Negative terminal for CELL5
17	CB5	Cell balance control pin for CELL5
18	VC5	Positive terminal for CELL5
19	CB4	Cell balance control pin for CELL4
20	VC4	Positive terminal for CELL4
21	CB3	Cell balance control pin for CELL3
22	VC3	Positive terminal for CELL3
23	CB2	Cell balance control pin for CELL2
24	VC2	Positive terminal for CELL2
25	CB1	Cell balance control pin for CELL1
26	NC	No Connection
27	VC1	Positive terminal for CELL1
28	VDD	VDD pin

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, V_{SS} = 0 V)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply voltage	−0.3 to 30	V
V_{C1}	CELL1 positive input pin voltage	V_{C2}−0.3 to V_{C2}+6.5	V
V_{C2}	CELL2 positive input pin voltage	V_{C3}−0.3 to V_{C3}+6.5	V
V_{C3}	CELL3 positive input pin voltage	V_{C4}−0.3 to V_{C4}+6.5	V
V_{C4}	CELL4 positive input pin voltage	V_{C5}−0.3 to V_{C5}+6.5	V
V_{C5}	CELL5 positive input pin voltage	V_{SS0}−0.3 to V_{SS0}+6.5	V
V_{SS0}	CELL5 negative input pin voltage	−0.3 to V_{C5}+0.3	V
V_{MP}	Charger negative input pin voltage	V_{DD}−30 to V_{DD}+0.3	V
V_{SEL1}	SEL1 pin input voltage	−0.3 to V_{DD}+0.3	V
V_{SEL2}	SEL2 pin input voltage	−0.3 to V_{DD}+0.3	V
V_{CTLC}	COUT control pin voltage	−0.3 to V_{DD}+25 < 48	V
V_{CTLD}	DOUT control pin voltage	−0.3 to V_{DD}+25 < 48	V
V_{SENS}	Current sense pin voltage	V_{VR}−6.5 to V_{VR}+0.3	V
V_{CT1}	Delay time setting 1 pin voltage	−0.3 to V_{VR}+0.3	V
V_{CT2}	Delay time setting 2 pin voltage	−0.3 to V_{VR}+0.3	V
V_{TEP}	Temperature protection input pin voltage	−0.3 to V_{VR}+0.3	V
V_{COUT}	COUT pin output voltage	V_{DD}−30 to V_{DD}+0.3	V
V_{DOUT}	DOUT pin output voltage	−0.3 to V_{OH2}+0.3	V
V_{DRAIN}	DRAIN pin output voltage	−0.3 to V_{OH3}+0.3	V
V_{CB1}	CB1 pin output voltage	V_{C2}−0.3 to V_{C2}+6.5	V
V_{CB2}	CB2 pin output voltage	V_{C3}−0.3 to V_{C3}+6.5	V
V_{CB3}	CB3 pin output voltage	V_{C4}−0.3 to V_{C4}+6.5	V
V_{CB4}	CB4 pin output voltage	V_{C5}−0.3 to V_{C5}+6.5	V
V_{CB5}	CB5 pin output voltage	−0.3 to 6.5	V
V_{VHC}	VHC pin output voltage	V_{DD}-3 to V_{DD}+5	V
V_{VR}	VR pin output voltage	−0.3 to V_{VR}+0.3	V
P_D	Power Dissipation [1] (TSSOP-28, JEDEC STD.51-7 Test Land Pattern)	1250	mW
Tj	Junction Temperature Range	−40 ~ 125	°C
Tstg	Storage Temperature Range	−55 ~ 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

[1] Refer to *POWER DISSIPATION* in *SUPPLEMENTSRY ITEMS* for detail information.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Rating	Unit
V_{DD}	Operating Input Voltage	2.5 to 25	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{CELLn} = CELLn (Ex. V_{CELL1} is a voltage difference between VC1 and VC2)
n = 1, 2, 3, 4, 5, unless otherwise noted.

R5436TxxxBA / R5436TxxxBB Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Circuit (1)
V_{DET1n}	CELLn overcharge detection voltage	At rising edge detection of supply voltage	V_{DET1n} -0.025V	V_{DET1n}	V_{DET1n} +0.025V	V	A
V_{REL1n}	CELLn overcharge release voltage	At falling edge detection of supply voltage	V_{REL1n} -0.050V	V_{REL1n}	V_{REL1n} +0.050V	V	A
t_{VDET1}	Overcharge detection delay time	VDD=VC1, V_{CELLn}=3.5V (n=2,3,4,5) V_{CELL1}=3.5V → 4.5V	0.7	1.0	1.3	s	B
t_{VREL1}	Overcharge release delay time	VDD=VC1, V_{CELLn}=3.5V (n=2,3,4,5) V_{CELL1}=4.5V → 3.0V	11	16	21	ms	B
V_{CBDn}	CELLn cell balance detection voltage	At rising edge detection of supply voltage	V_{CBDn} -0.025V	V_{CBDn}	V_{CBDn} +0.025V	V	C
V_{CBRn}	CELLn cell balance release voltage (2)	At falling edge detection of supply voltage	V_{CBRn} -0.050V	V_{CBRn}	V_{CBRn} +0.050V or V_{CBDn} +0.025V	V	C
t_{VCBD}	CELLn cell balance detection delay time	VDD=VC1,V_{CELLn}=3.5V (n=2,3,4,5) V_{CELL1}=3.5V → V_{CBDn}	11	16	21	ms	C
V_{DET2n}	CELLn overdischarge detection voltage	At falling edge detection of supply voltage	V_{DET2n} x 0.975V	V_{DET2n}	V_{DET2n} x1.025V	V	D
V_{REL2n}	CELLn overdischarge release voltage	At rising edge detection of supply voltage	V_{REL2n} x 0.975V	V_{REN2n}	V_{REN2n} x1.025V	V	D
I_{CT1}	CT1 charging current	VDD=VC1,V_{CELLn}=3.5V (n=2,3,4,5) V_{CELL1}=3.5V → 1.5V	350	500	650	nA	E
V_{DCT1}	CT1 detection voltage	VDD=VC1,V_{CELLn}=3.5V (n=2,3,4,5), V_{CELL1}=1.5V	1.44	1.80	2.16	V	F
t_{VDET2}	Overdischarge detection delay time	t_{VDET2}=C_{CT1}xV_{DCT1}/I_{CT1}, C_{CT1}=3.3nF	83	119	155	ms	-
t_{VREL2}	Overdischarge release delay time	VDD=VC1,V_{CELLn}=3.5V (n=2,3,4,5) V_{CELL1}=1.5V → 3.5V	0.7	1.2	1.7	ms	G
V_{DET31}	Discharge overcurrent detection voltage 1	VDD=VC1,V_{CELLn}=3.5V, V_{MP}=4.0V, At rising edge detection of SENS pin	V_{DET31} -0.020V	V_{DET31}	V_{DET31} +0.020V	V	H
V_{DET32}	Discharge overcurrent detection voltage 2	VDD=VC1,V_{CELLn}=3.5V, V_{MP}=4.0V, At rising edge detection of SENS pin	V_{DET32} -0.050V	V_{DET32}	V_{DET32} +0.050V	V	I
V_{REL3}	Discharge overcurrent release voltage	VDD=VC1, V_{CELLn}=3.5V, SENS=0.0V, At falling edge detection of VMP pin	0.8	1.0	1.2	V	H
I_{CT231}	CT2 charge current 1	VDD=VC1, V_{CELLn}=3.5V, SENS=V_{SS}→0.4V	350	500	650	nA	I

(1) Refer to *TEST CIRCUITS* for detail information.
(2) Max.value is equal to the lower value of V_{CBRn}+0.050V or V_{CBDn}+0.025V.

V_{CELLn} = CELLn (Ex. V_{CELL1} is a voltage difference between VC1 and VC2)
n = 1, 2, 3, 4, 5, unless otherwise noted.

R5436TxxxBA / R5436TxxxBB Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Circuit (1)
I_{CT232}	CT2 charge current 2	VDD=VC1, V_{CELLn}=3.5V SENS=V_{SS}→0.7V	2.0	3.0	4.0	µA	I
V_{DCT2}	CT2 detection voltage	VDD=VC1, V_{CELLn}=3.5V SENS=0.4V, VMP=4.0V	1.20	1.50	1.80	V	J
t_{VDET31}	Discharge overcurrent detection delay time 1	t_{VDET31} = C_{CT2}×V_{DCT2}/I_{CT231} C_{CT2}=3.3nF	6.9	9.9	12.9	ms	-
t_{VDET32}	Discharge overcurrent detection delay time 2	t_{VDET32} = C_{CT2}×V_{DCT2}/I_{CT232} C_{CT2}=3.3nF	1.1	1.65	2.2	ms	-
t_{VREL3}	Discharge overcurrent release delay time	VDD=VC1, V_{CELLn}=3.5V, SENS=V_{SS}, V_{MP}= 4.0V→V_{SS}	0.7	1.2	1.7	ms	H
V_{SHORT}	Short-circuit detection voltage	VDD=VC1, V_{CELLn}=3.5V, V_{MP}=4.0V, At rising edge detection of SENS pin	V_{SHORT} x 0.8	V_{SHORT}	V_{SHORT} x 1.2	V	K
t_{SHORT}	Short-circuit detection delay time	VDD=VC1, V_{CELLn}=3.5V, SENS=0.0V→2.0V, V_{MP}=4.0V	230	330	430	µs	K
V_{DET4}	Charge overcurrent detection voltage	VDD=VC1, V_{CELLn}=3.5V, V_{MP}= -1.0V, At falling edge detection of SENS pin	V_{DET4} -0.030V	V_{DET4}	V_{DET4} +0.030V	V	L
V_{REL4}	Charge overcurrent release voltage	VDD=VC1, V_{CELLn}=3.5V At rising edge detection of VMP pin	0.05	0.1	0.15	V	L
t_{VDET4}	Charge overcurrent detection delay time	VDD=VC1, V_{CELLn}=3.5V, SENS=0.0V→-1.0V	5	8	11	ms	L
t_{VREL4}	Charge overcurrent release delay time	VDD=VC1, V_{CELLn} =3.5V, SENS=V_{SS}, V_{MP}=-1.0V→1.0V	0.7	1.2	1.7	ms	L
V_{IH1}	SEL1 pin ”High” input voltage	VDD=VC1, V_{CELLn} =3.4V	V_{DD}-0.3V		V_{DD}+0.3V	V	M
V_{IM1}	SEL1 pin ”Middle” input voltage	VDD=VC1, V_{CELLn} =3.4V	4.0		V_{DD}/2-0.5V	V	M
V_{IL1}	SEL1 pin ”Low” input voltage	VDD=VC1, V_{CELLn} =3.4V	V_{SS}-0.3V		V_{SS}+0.3V	V	M
V_{IH2}	SEL2 pin ”High” input voltage	VDD=VC1, V_{CELLn} =3.4V	V_{DD}-0.3V		V_{DD}+0.3V	V	N
V_{IM2}	SEL2 pin ”Middle” input voltage	VDD=VC1, V_{CELLn} =3.4V	4.0		V_{DD}/2-0.5V	V	N
V_{IL2}	SEL2 pin “Low” input voltage	VDD=VC1, V_{CELLn} =3.4V	V_{SS}-0.3V		V_{SS}+0.3V	V	N
V_{CTLC1H}	CTLC pin ”High” threshold voltage 1	VDD=VC1, V_{CELLn} =3.4V	17.5	18.1	18.7	V	O
V_{CTLC2H}	CTLC pin ”High” threshold voltage 2	VDD=VC1, V_{CELLn} =3.4V	15.1	16.1	16.6	V	O
V_{CTLD1H}	CTLD pin ”High” threshold voltage 1	VDD=VC1, V_{CELLn} =3.4V	17.5	18.1	18.7	V	P
V_{CTLD2H}	CTLD pin ”High” threshold voltage 2	VDD=VC1, V_{CELLn} =3.4V	15.1	16.1	16.6	V	P

(1) Refer to *TEST CIRCUITS* for detail information.

V_{CELLn} = CELLn (Ex. V_{CELL1} is a voltage difference between VC1 and VC2)
n = 1, 2, 3, 4, 5, unless otherwise noted.

R5436TxxxBA / R5436TxxxBB Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit	Circuit (1)
t_{CTLD1}	CTLD pin input delay time 1	VDD=VC1, V_{CELLn} =3.4V CTLD=V_{DD}+0.5V →V_{DD}+1.7V	R5436TxxxBB only		1.5	6	ms	P
t_{CTLD2}	CTLD pin input delay time 2	VDD=VC1, V_{CELLn} =3.4V CTLD=V_{DD}+1.7V →V_{DD}+0.5V	R5436TxxxBB only		1.5	6	ms	P
V_{OL2}	DOUT pin Nch. ON voltage	I_{OL}=50μA, V_{DD}=V_{C1}, CTLD=V_{DD} V_{CELLn} =3.4V			0.1	0.5	V	Q
V_{OL3}	DRAIN pin Nch. ON voltage	I_{OL}=50μA, VDD=VC1, V_{CELLn} =3.4V			0.1	0.5	V	R
V_{OL4}	CB1 pin Nch. ON voltage	I_{OL}=50μA, VDD=VC1, V_{CELLn} =3.4V			V_{C2}+0.2V	V_{C2}+0.5V	V	S
V_{OL5}	CB2 pin Nch. ON voltage	I_{OL}=50μA, VDD=VC1, V_{CELLn} =3.4V			V_{C3}+0.2V	V_{C3}+0.5V	V	S
V_{OL6}	CB3 pin Nch. ON voltage	I_{OL}=50μA, VDD=VC1, V_{CELLn} =3.4V			V_{C4}+0.2V	V_{C4}+0.5V	V	S
V_{OL7}	CB4 pin Nch. ON voltage	I_{OL}=50μA, VDD=VC1, V_{CELLn} =3.4V			V_{C5}+0.2V	V_{C5}+0.5V	V	S
V_{OL8}	CB5 pin Nch. ON voltage	I_{OL}=50μA, VDD=VC1, V_{CELLn} =3.4V			0.2V	0.5V	V	S
V_{OH1}	COUT pin Pch. ON voltage	I_{OH}=-50μA, VDD=VC1, CTLC=V_{SS}, V_{CELLn}=3.4V		V_{DD}-0.5V	V_{DD}-0.1V		V	T
V_{VR12}	VR12V output voltage	I_{OH}=-5μA, VDD=VC1,CTLD= V_{SS} V_{CELLn} =3.4V The measured value by pulling current through DOUT pin.		9.5	12	14	V	U
V_{OH2}(2)	DOUT pin Pch. ON voltage	I_{OH}= -50μA, VDD=VC1, CTLD= V_{SS}, V_{CELLn} =3.2V		V_{VR12}-0.5V	V_{VR12}-0.1V		V	U
V_{OH3}(2)	DRAIN pin Pch. ON voltage	I_{OH}= -50μA, VDD=VC1, V_{CELL} = 3.2V, SENS=VMP=4.0V		V_{VR12}-0.5V	V_{VR12}-0.1V		V	V
V_{OH4}	CB1 pin Pch. ON voltage	I_{OH}= -50μA, VDD=VC1,V_{C1}=4.5V, V_{CELLn}=3.2V(n=2,3,4,5)		V_{C1}-0.5V	V_{C1}-0.3V		V	W
V_{OH5}	CB2 pin Pch. ON voltage	I_{OH}= -50μA, VDD=VC1,V_{C2}=4.5V, V_{CELLn}=3.2V (n=1,3,4,5)		V_{C2}-0.5V	V_{C2}-0.3V		V	W
V_{OH6}	CB3 pin Pch. ON voltage	I_{OH}= -50μA, VDD=VC1,V_{C3}=4.5V, V_{CELLn}=3.2V (n=1,2,4,5)		V_{C3}-0.5V	V_{C3}-0.3V		V	W
V_{OH7}	CB4 pin Pch. ON voltage	I_{OH}= -50μA, VDD=VC1,V_{C4}=4.5V, V_{CELLn}=3.2V (n=1,2,3,5)		V_{C4}-0.5V	V_{C4}-0.3V		V	W
V_{OH8}	CB5 pin Pch. ON voltage	I_{OH}= -50μA, VDD=VC1,V_{C5}=4.5V, V_{CELLn}=3.2V (n=1,2,3,4)		V_{C5}-0.5V	V_{C5}-0.3V		V	W

(1) Refer to *TEST CIRCUITS* for detail information.
(2) When V_{DD} < V_{VR12}-0.1V, DOUT / DRAIN pin voltage (V_{OH2}/V_{OH3}) becomes almost equal to V_{DD}.

V_{CELLn} = CELLn (Ex. V_{CELL1} is a voltage difference between VC1 and VC2)
n = 1, 2, 3, 4, 5, unless otherwise noted.

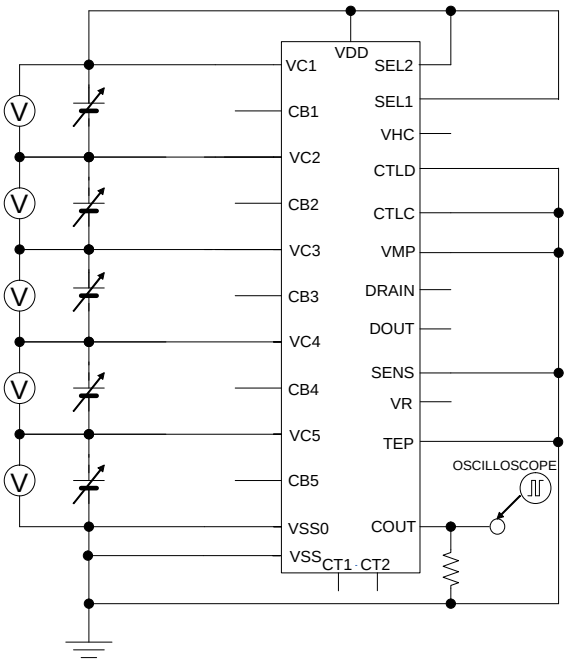
R5436TxxxBA / R5436TxxxBB Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Circuit (1)
I_{LCOUT}	COUT pin off leakage-current	VDD=VC1, V_{CELLn}=3.4V,C_{TLC}=V_{DD}, C_{OUT}= -14V	-0.1			µA	X
V_{VR}	VR output voltage	VDD=VC1, V_{CELLn}=3.4V	3.5	3.6	3.7	V	Y
V_{T_DET}	Detection voltage of TEP temperature protection	VDD=VC1, V_{CELLn}=3.4V	V_{T_DET} -0.027	V_{T_DET}(2)	V_{T_DET} +0.035	V	Z
V_{T_REL}	Release voltage of TEP temperature protection	VDD=VC1, V_{CELLn}=3.4V	V_{T_REL} -0.043	V_{T_REL}2	V_{T_REL} +0.050	V	Z
t_{T_DET}	TEP detection delay time	VDD=VC1, V_{CELLn}=3.4V, V_{TEP}=0V→2V	5	8	11	ms	Z
t_{T_REL}	TEP release delay time	VDD=VC1, V_{CELLn}=3.4V, V_{TEP}=2V→0V	11	16	21	ms	Z
t_{LT}	Broken wire scanning cycle	VDD=VC1, V_{CELLn}=V_{CBDn}+0.05V	0.7	1.25	1.8	S	a
V_{HCO1}	VHC pin Nch. ON voltage 1	I_{OH}= 2µA, VDD=VC1, V_{CELLn}=3.4V, V_{MP}=0V	14.5	15.5	16.5	V	c
V_{HCO2}	VHC pin Nch. ON voltage 2	I_{OH}=10µA, VDD=VC1, V_{CELLn}=3.4V, V_{MP}=0V		V_{HC1}+0.3	V_{HC1}+0.5	V	c
I_{LVHC}	VHC pin off leakage-current	VDD=VC1, V_{CELLn}=3.4V, V_{MP}=0.5V, V_{HC}=32V			0.1	µA	b
I_{SS1}	Supply current 1	VDD=VC1, C_{OUT}=OPEN V_{CELLn} =V_{DET1n} - 0.4V		12	30	µA	d
I_{SS2}	Supply current 2	VDD=VC1, C_{OUT}=OPEN V_{CELLn} =1.5V		6	12	µA	d
V_{STB}	Power ON voltage at standby mode	VDD=VC1=1.5V, V_{CELLn}=3.4V (n=2,3,4,5), At rising edge detection of VMP pin	0.9	1.13	1.35	V	H

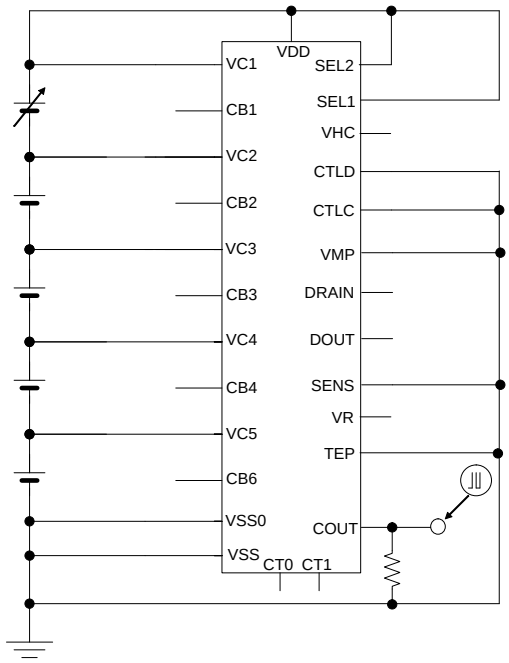
(1) Refer to *TEST CIRCUITS* for detail information.
(2) V_{T_DET}=20/21*V_{VR}, V_{T_REL}=27/29*V_{VR} (V_{VR}:VR pin output voltage)

TEST CIRCUITS

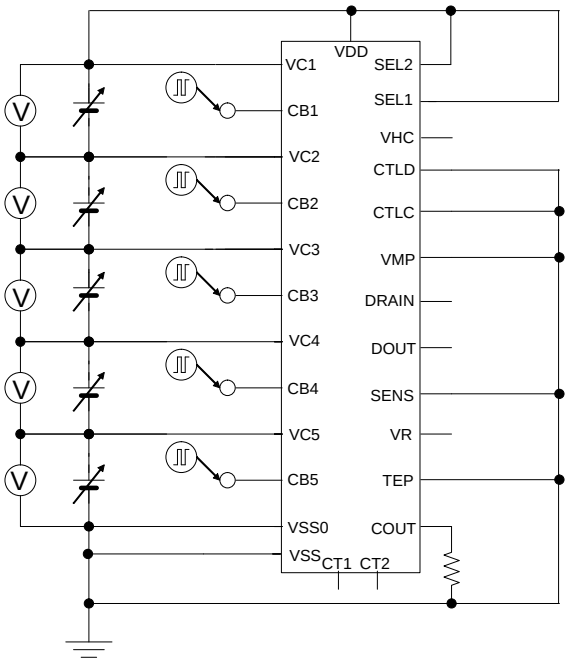
A



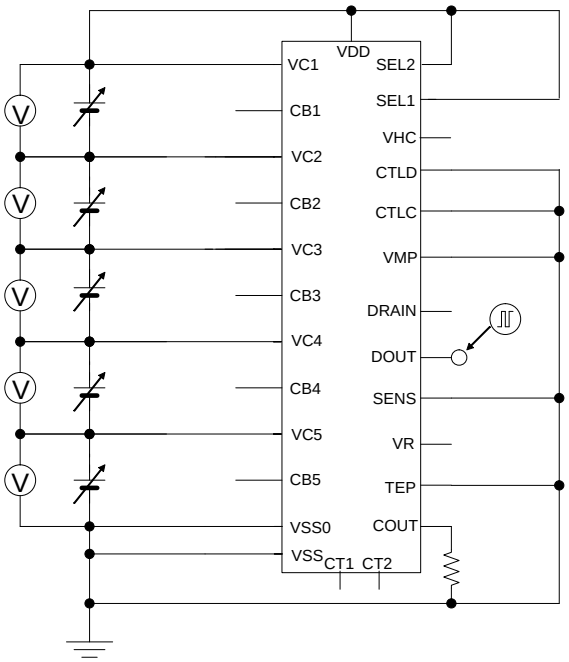
B



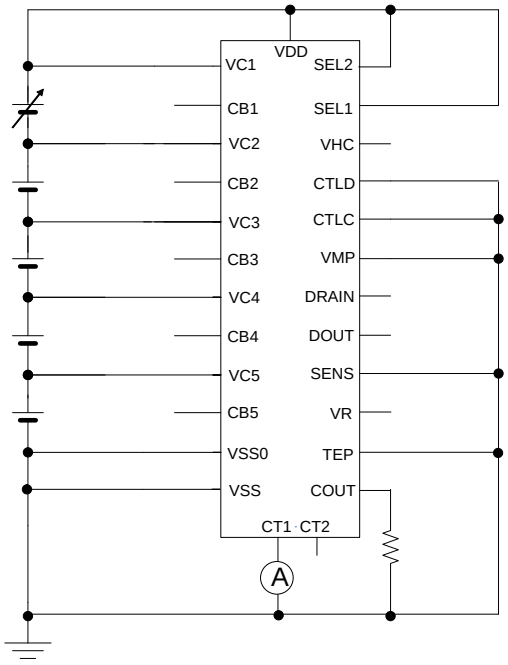
C



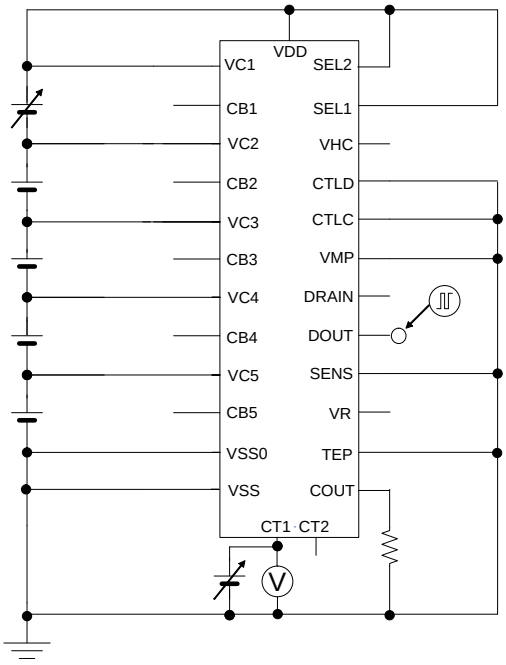
D



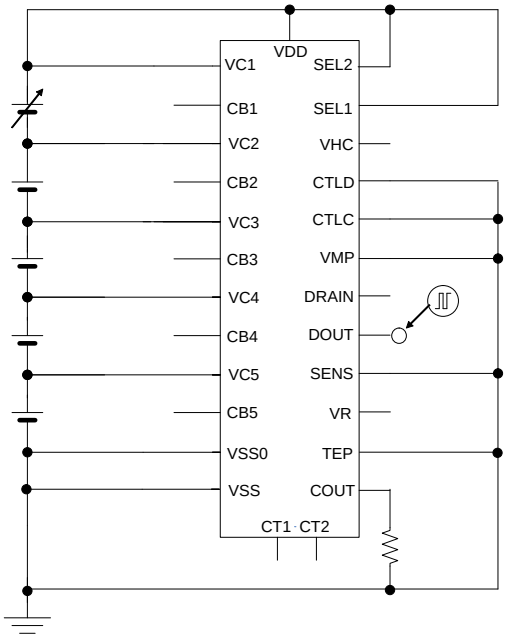
E



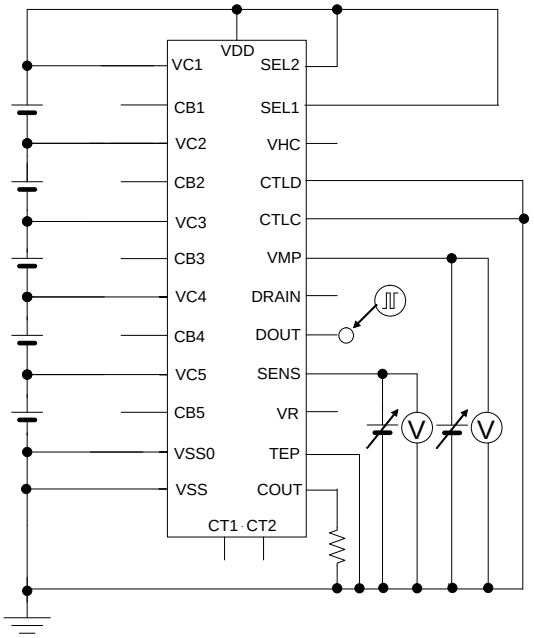
F



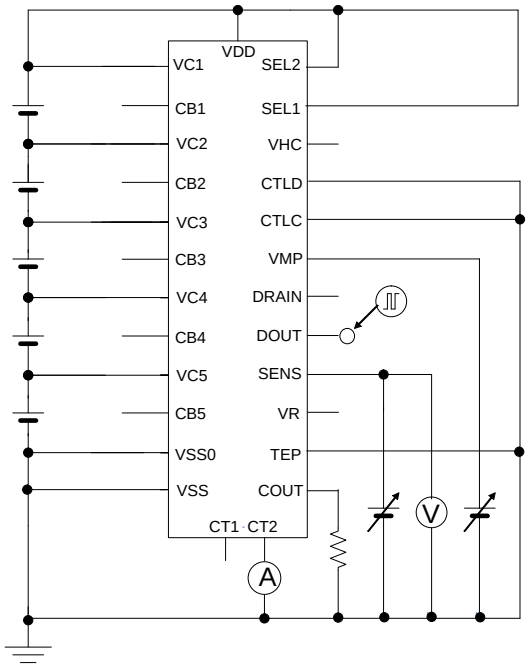
G



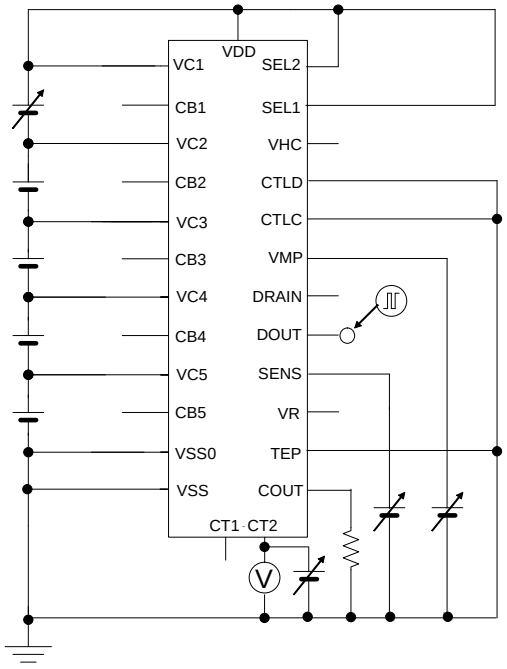
H



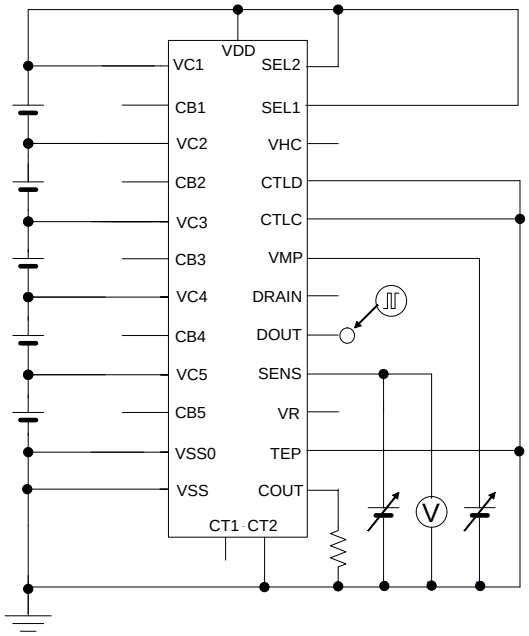
I



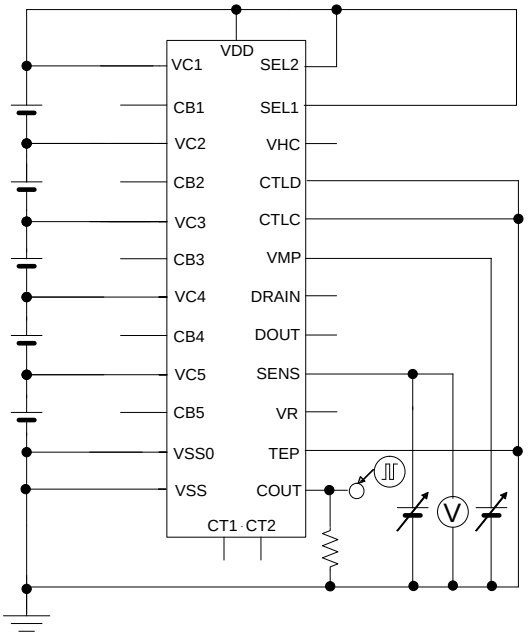
J



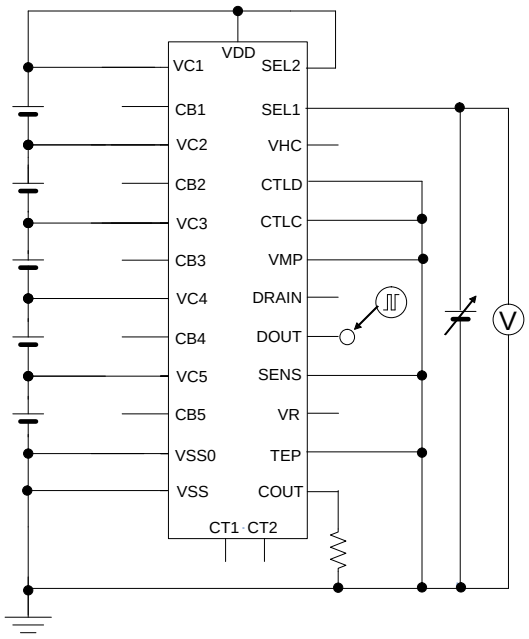
K



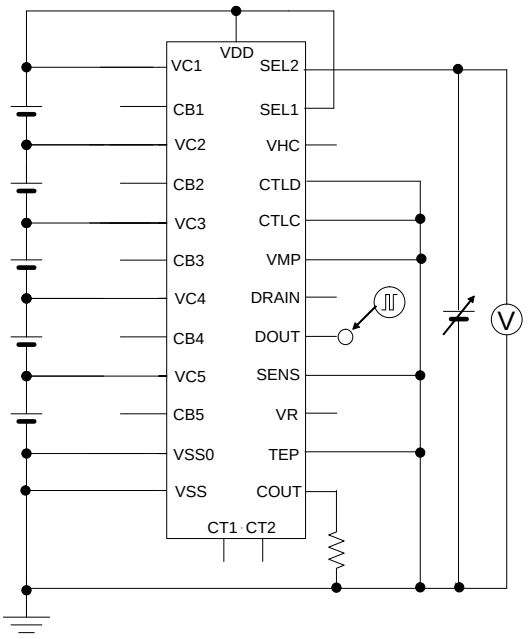
L



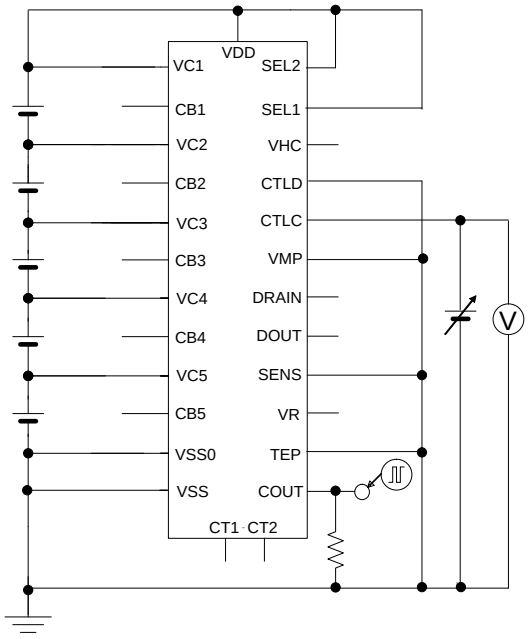
M



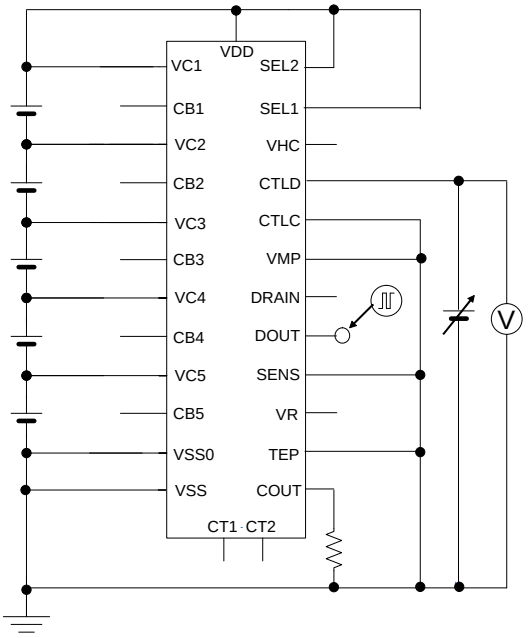
N



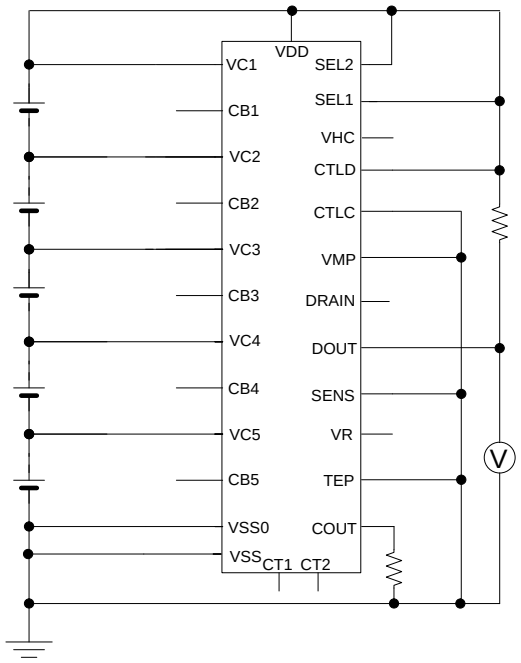
O



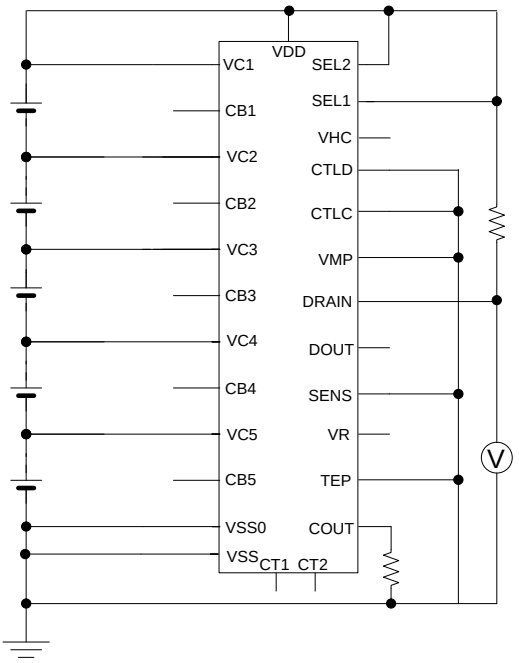
P



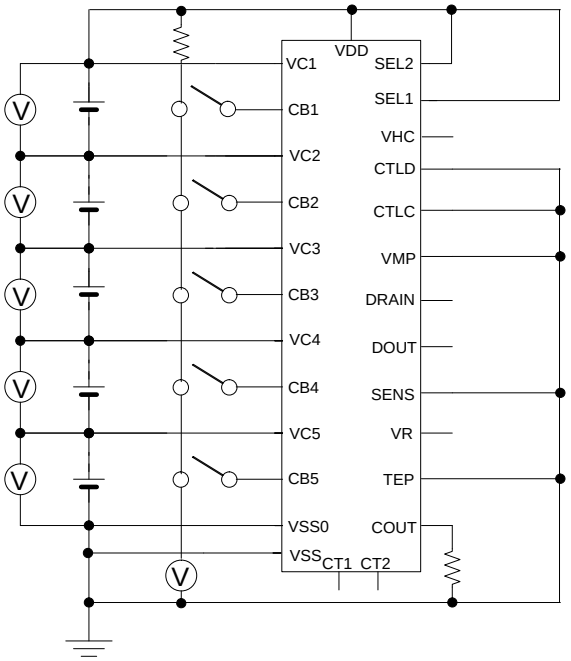
Q



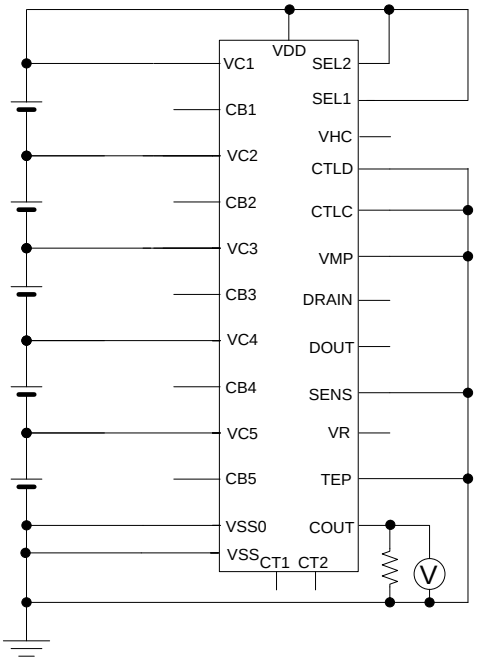
R



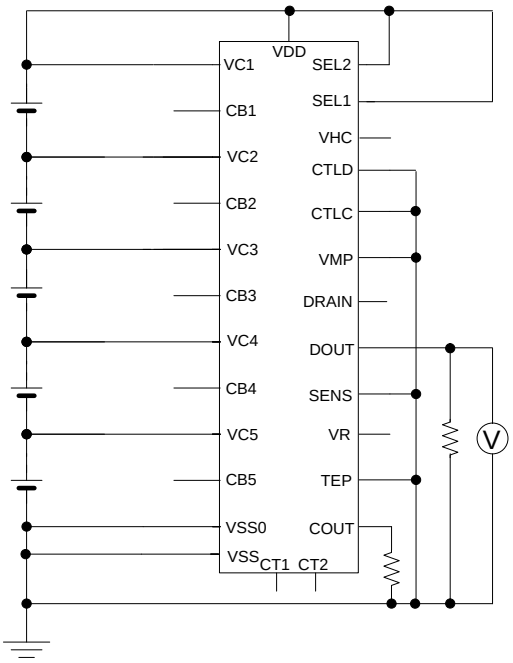
S



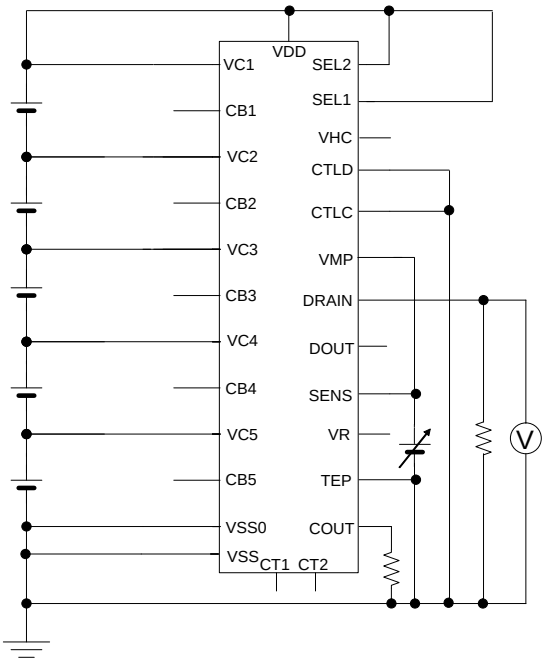
T



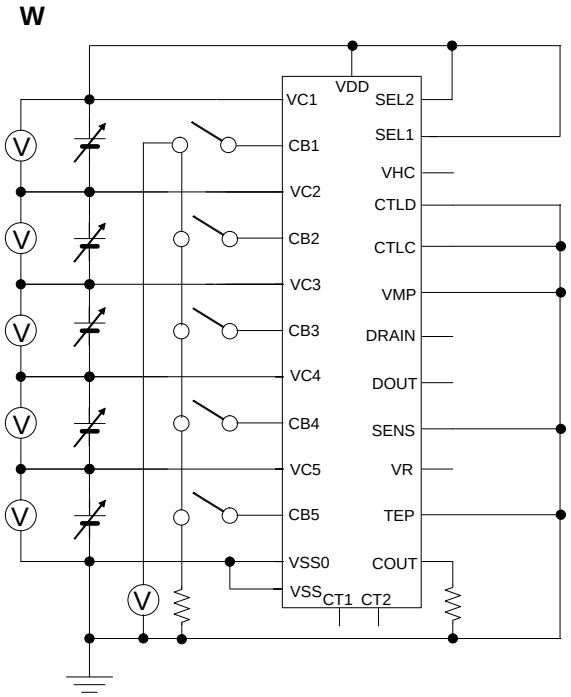
U



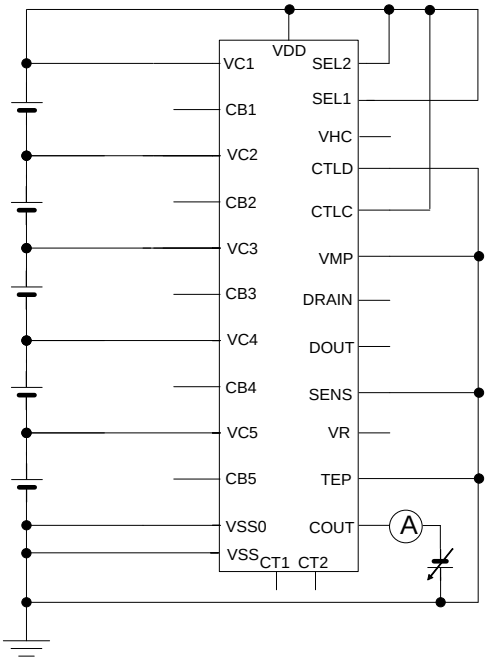
V



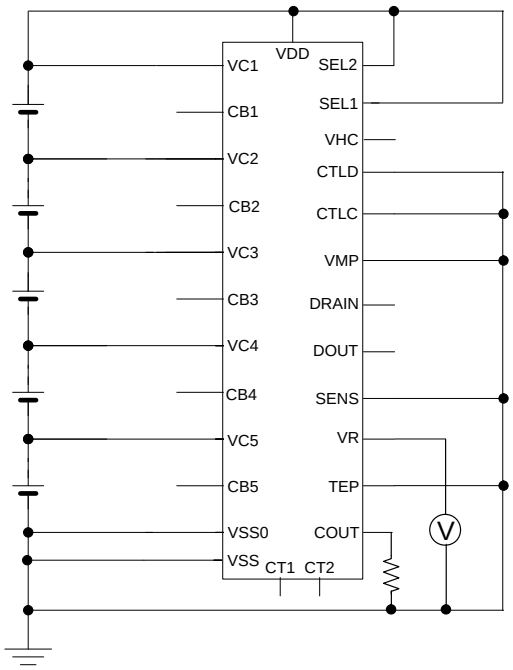
W



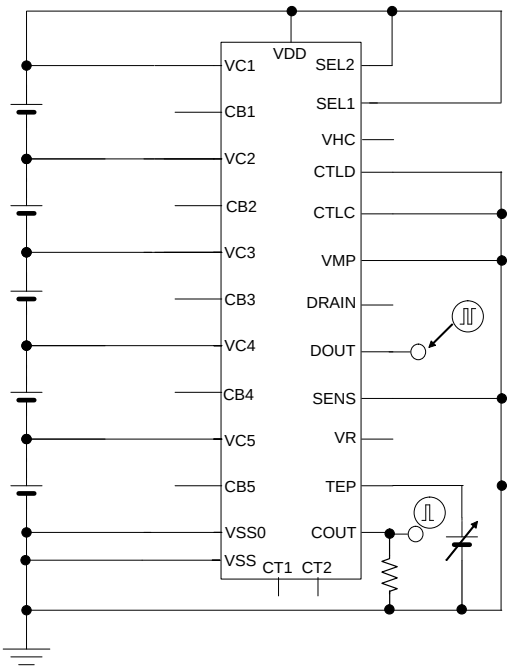
X



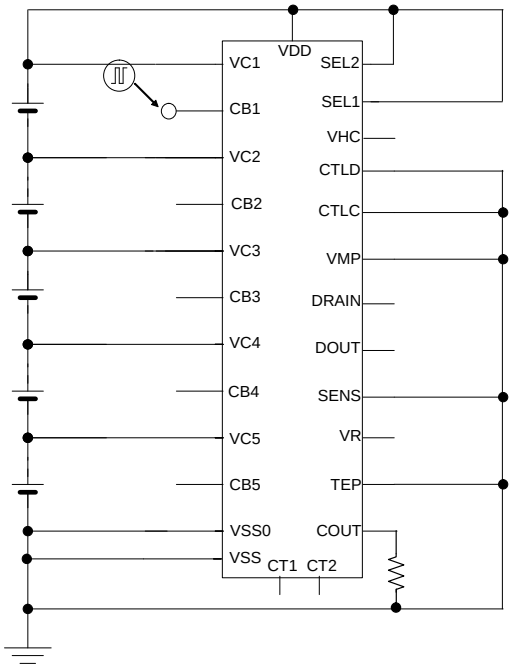
Y



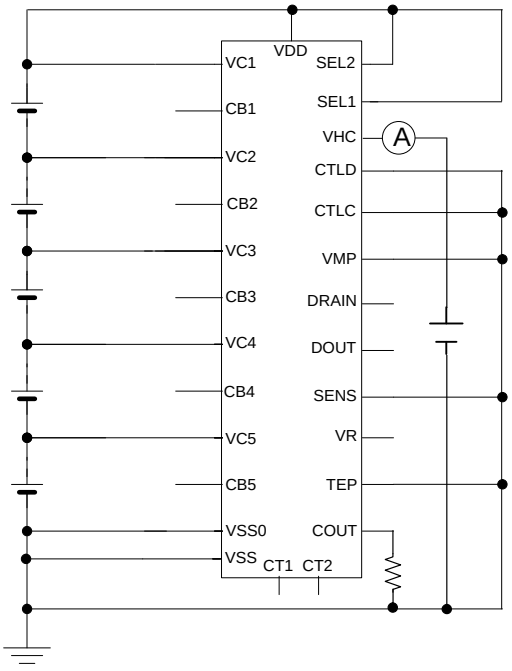
Z



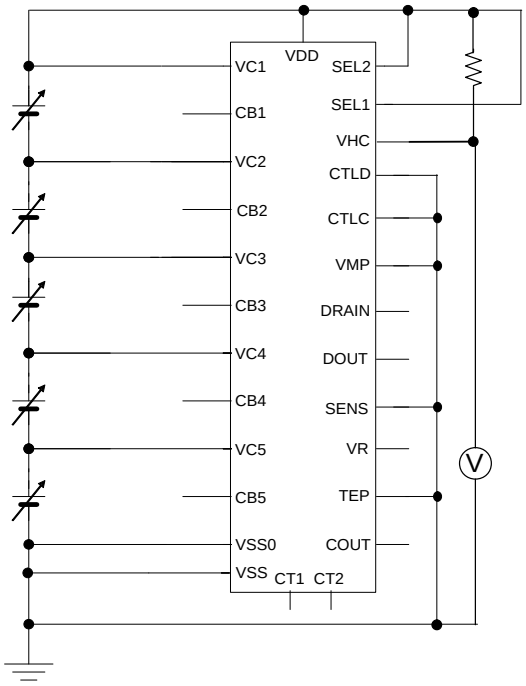
a



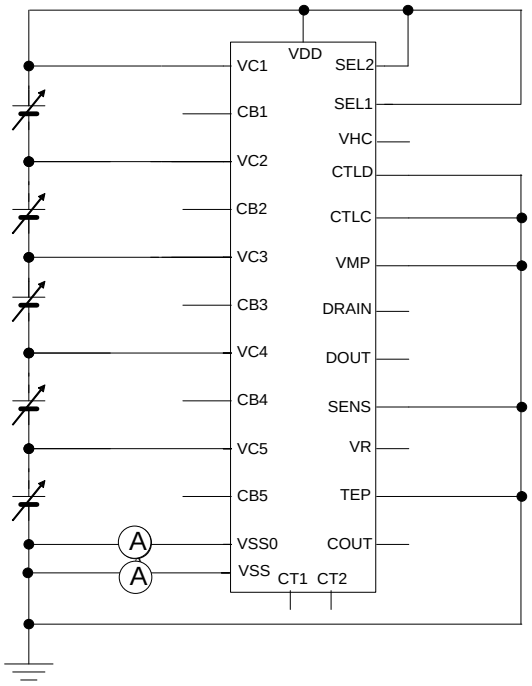
b



c



d



THEORY OF OPERATION

Overcharge Detection: VD1-n (n = 1, 2, 3, 4, 5)

During charging, the device supervises the voltage between VC1 and VC2 pins (the CELL1 voltage), the voltage between VC2 and VC3 pins (the CELL2 voltage), the voltage between VC3 and VC4 pins (the CELL3 voltage), the voltage between VC4 and VC5 pins (the CELL4 voltage), and the voltage between VC5 and VSS0 pins (the CELL5 voltage). If at least one of the cells' voltage becomes more than the overcharge detection voltage, the overcharge is detected, and COUT pin connected to an external pull-down resistor becomes "Hi-z", and it makes the external Nch.FET turn off. Then, the charging stops.

After detecting the overcharge, when all the cell voltage become lower than the overcharge detection voltage by connecting a load, COUT pin becomes "High", and it makes the external Nch. FET turn on, and the charging restarts. Even If all the cell voltage become lower than the overcharge release voltage with no load, COUT pin becomes "High" and the charging is available.

The device has internal fixed output delay times for overcharge detection and overcharge release. When the output delay time passes while any one of cell voltages is more than the overcharge detection voltage, the overcharge is detected. However, all cell voltage becomes lower than the overcharge detection voltage within the overcharge detection delay time, even if any one of cells' voltage becomes more than the overcharge detection voltage, the overcharge is not detected.

Besides, after detecting the overcharge, any one of their cell voltages becomes more than the overcharge release voltage within the overcharge release delay time, even if all the cell voltage becomes lower than the overcharge release voltage, the device does not release from the overcharge.

Overdischarge Detection: VD2-n (n = 1, 2, 3, 4, 5)

During discharging, the device supervises the voltage between VC1 and VC2 pins (the CELL1 voltage), the voltage between VC2 and VC3 pins (the CELL2 voltage), the voltage between VC3 and VC4 pins (the CELL3 voltage), the voltage between VC4 and VC5 pins (the CELL4 voltage), and the voltage between VC5 and VSS0 pins (the CELL5 voltage). If at least one of the cells' voltage becomes less than the overdischarge detection voltage, the overdischarge is detected, and DOUT pin becomes "Low", and it makes the external Nch.FET turn off. Then, the discharging stops.

The release condition from the overdischarge detection is different depending on optional functions. One is the latch type, after detecting the overdischarge, when the battery becomes higher than the overdischarge release voltage by connecting a charger, DOUT pin becomes "High". And, the other is the voltage release type, when the cell voltage becomes higher than the overdischarge release voltage, the device releases from the overdischarge even if the charger is not connected, and DOUT pin becomes "High".

An output delay time for overdischarge detection is settable by the external capacitor (C_{CT1}) connected to CT1 pin. When the output delay time passes while any one of each cell voltage is lower than the overdischarge detection voltage, the overdischarge is detected. However, all cell voltage becomes higher than the overdischarge detection voltage within the overdischarge detection delay time even if any one of cells' voltage becomes lower than the overdischarge detection voltage, the overdischarge is not detected. An output delay time for overdischarge release is fixed internally.

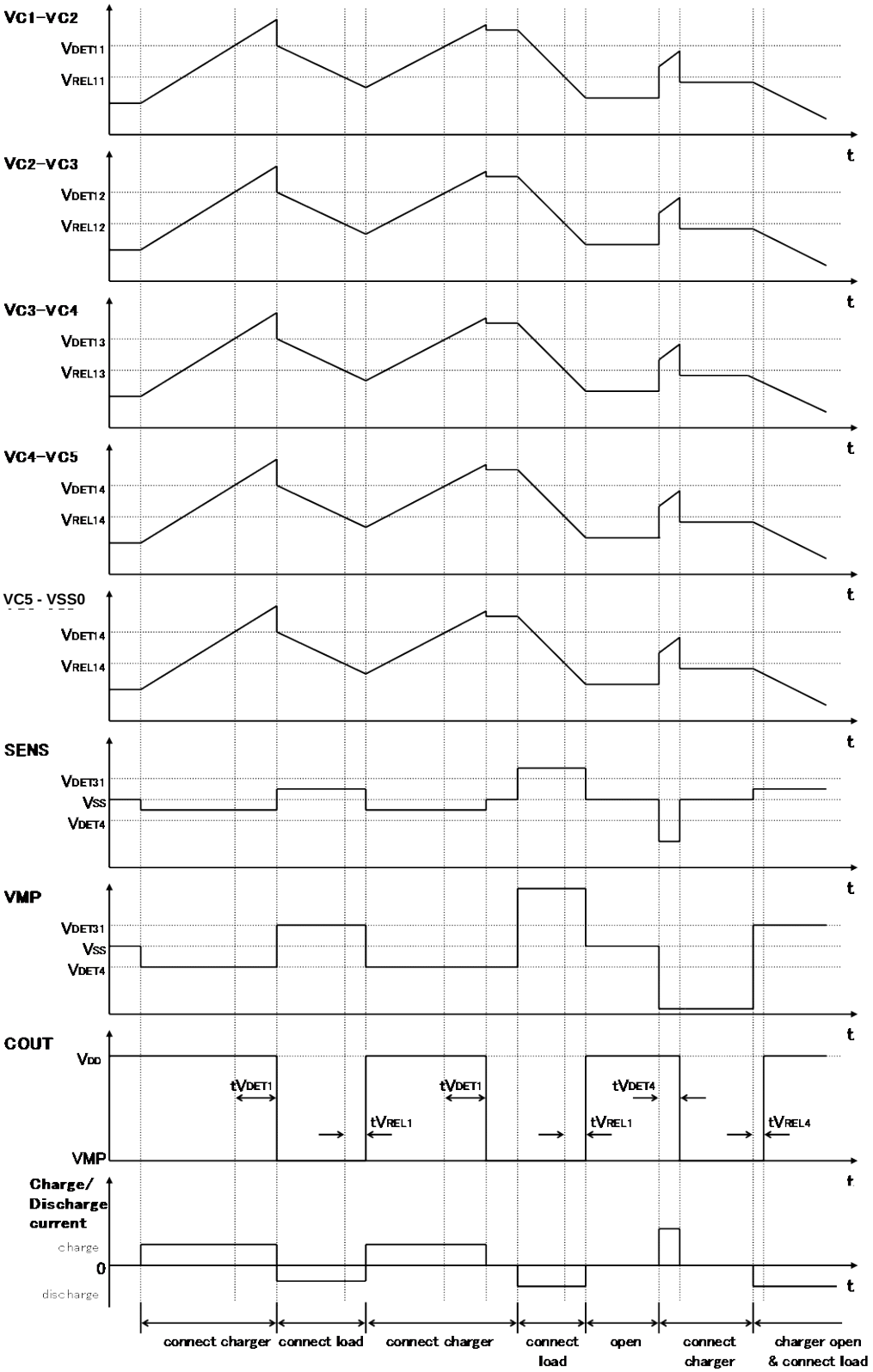
After detecting the overdischarge, the device stops unnecessary circuits to reduce the consumption current to a minimum when VMP pin becomes “High”. DOUT pin, which is CMOS output, outputs the internal regulator’s voltage (about 12 V) at “High” level and outputs VSS pin voltage at “Low” level.

Discharge Overcurrent Detection: VD3-n (n = 1, 2) and Short-circuit Detection

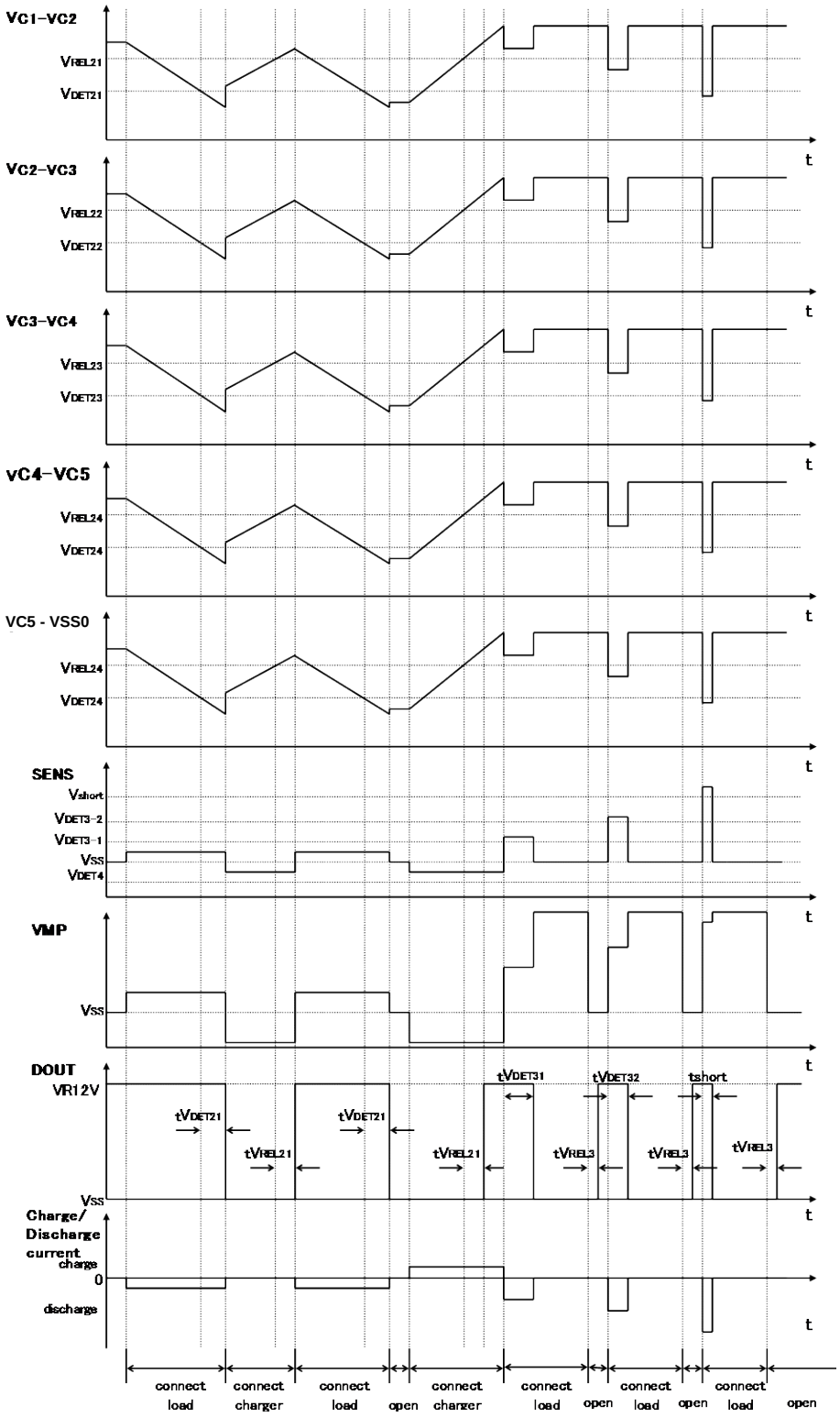
During discharging, the device supervises SENS pin voltage (V_{SENS}).
The discharge overcurrent is detected when SENS pin voltage (V_{SENS}) becomes in between the discharge overcurrent detection voltage (V_{DET3n}) and the short-circuit detection voltage (V_{SHORT}) owing to a large load, and the short-circuit is detected when V_{SENS} becomes more than V_{SHORT}. Then, to prevent from flowing large current to circuits, DOUT pin is set to “Low” and the external FET is turned OFF.
The device has two detection threshold to detect the discharge overcurrent. Each detection threshold has the output delay time each other. The discharge overcurrent detection delay time 2 (t_{VDET32}) is set to be shorter than the discharge overcurrent detection delay time 1 (t_{VDET31}). An output delay time for discharge overcurrent detection is settable by the external capacitor (C_{CT2}) connected to CT2 pin. When V_{SENS} becomes lower than V_{DET3n} within the output delay time even if V_{SENS} is in between V_{DET3x} and V_{SHORT}, the discharge overcurrent is not detected. The output delay times for discharge overcurrent release and short-circuit are fixed internally.
Connect an external resistor for discharge overcurrent release among each drain of the external FETs connected to DRAIN, COUT, and DOUT pins. After detecting the discharge overcurrent, or the short-circuit, turn ON the external FET connected to DRAIN pin, and connect a resistor for overcurrent release to VSS. When load is released and opened after detecting the discharge overcurrent or the short-circuit, The VMP pin voltage (V_{VMP}) is pulled-down to VSS via the resistor for the overcurrent release, and V_{VMP} becomes less than V_{REL3}. After a certain delay time, the discharge overcurrent detection state or the short-circuit detection state is released. When the discharge overcurrent detection is released, the external FET connected to DRAIN pin is turned OFF, and the resistor for the overcurrent release is disconnected from VSS.

Charge Overcurrent Detection: VD4

During charging or discharging, the device supervises SENS pin voltage (V_{SENS}). When a large current flows by charging with an inappropriate charger, SENS pin voltage becomes less than the charge overcurrent detection voltage, and the charge overcurrent is detected. COUT pin with the external pull-down resistor becomes “Hi-z”. And, tuning OFF the external FET can prevent from flowing large current to circuits.
When SENS pin voltage (V_{SENS}) becomes higher than V_{DET4} within the output delay time even if V_{SENS} becomes lower than the charge overcurrent detection voltage, the charge overcurrent is not detected. The output delay times for charge overcurrent detection and charge overcurrent release are fixed internally.
To release from the charge overcurrent, connect a load without the charger, and VMP pin voltage has to become higher than the charge overcurrent release voltage over the charge overcurrent release delay time.



Overcharge / Charge Overcurrent Operation Timing Chart



Overdischarge / Discharge Overcurrent / Short-circuit Operation Timing Chart

Standby Mode

This device can change from normal mode to standby mode when overdischarge is detected and VMP pin voltage (V_{VMP}) becomes higher than V_{STB}. In the standby mode, the device stops unnecessary circuits to reduce the consumption current to a minimum. At that time, VR pin output voltage becomes equal to the V_{SS} level. And, this device can return to the normal mode when V_{VMP} becomes lower than V_{STB} by connecting a charger.

Cell Imbalance

When any one of CELLs detects an overcharge and either one detects an overdischarge, COUT pin becomes "Hi-z" and DOUT pin becomes "Low".

SEL1 and SEL2 Pins

SEL1 and SEL2 pins are switching-control pins to select among 3- / 4- / 5-cell protection. When using for the 4-cell protection, connecting SEL1 pin to VSS and the SEL2 pin to VDD is required to stop the 5th cell protection circuit and shut signals. The overdischarge is not detected when VC5 pin is shortened to VSS0.
When using for the 3-cell protection, likewise, connecting SEL1 pin to VDD and SEL2 pin to VSS is required to stop the 5th and 4th cells protection circuits and shut signals. The overdischarge is not detected when VC4 and VC5 pins are shortened to VSS0. SEL1 / SEL2 pin must be fixed to VDD / VSS when using the 3- / 4- / 5-cell protection. Setting SEL1 and SEL2 pins can select disabling/enabling the open-wire detection(1) and the shorten mode 1/2. Refer to the following table for details of the operation mode.

Operation Modes

Input Voltage(2)		Operation Mode
SEL1 Pin	SEL2 Pin	
High	High	Enable the 5-cell protection mode
Low	High	Enable the 4-cell protection mode
High	Low	Enable the 3-cell protection mode
Low	Low	Disable the open-wire detection mode for 5-cell protection
Low	Middle	Disable the open-wire detection mode for 4-cell protection
Middle	Low	Disable the open-wire detection mode for 3-cell protection
Middle	Middle	Enable the delay time shorten mode 1 (approx.1/70) for 5-cell protection
Middle	High	Enable the delay time shorten mode 2 (approx.4 ms) for 5-cell protection
High	Middle	Enable the open-wire detecting test for 5-cell protection

(1) R5436TxxxBB does not support the open-wire detection.
(2) "High": VDD level, "Middle": (VDD/2-0.5) V to (VDD-3) V, "Low": VSS level

CTLC and CTLD Pins

When using cascade connection, the R5436T can transfer each state of overcharge, overdischarge, and open-wire detections by connecting between COUT and CTLC pins and between DOUT and CTLD pins. When not using it, CTLC and CTLD pins must be connected to VSS.

When CTLC / CTLD pin voltage is higher than the value of "High" threshold voltage 1 (V_{CTLC1H} / V_{CTLD1H}), or when CTLC / CTLD pin voltage is lower than the value of "High" threshold voltage 2 (V_{CTLC2H} / V_{CTLD2H}), COUT / DOUT pin becomes "High" after normal operation. By applying a voltage of between V_{CTLC1H} and V_{CTLC2H} to CTLC pin, COUT pin with an external pull-down resistor becomes "Hi-z" forcedly. And, by applying a voltage of between V_{CTLD1H} and V_{CTLD2H} to CTLD pin, DOUT pin with an external pull-down resistor becomes "Low" forcedly. Don't make CTLC and CTLD pins open. The following table indicates a relationship between the control pins (CTLC and CTLD) and the state of the external FETs for COUT and DOUT pins.

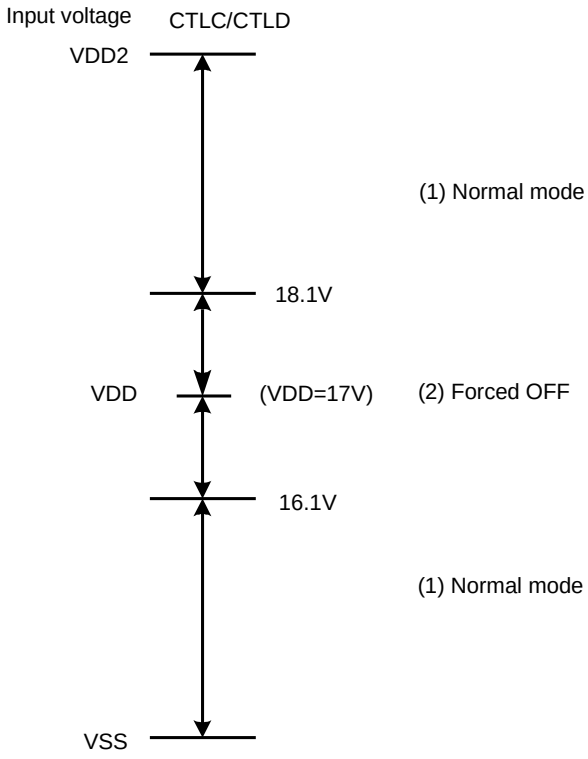
External FET's state by CTLx pins

CTLC / CTLD pins	External FET for COUT / DOUT pins
$2V_{DD}$ to V_{CTLC1H} / V_{CTLD1H}	ON (Normal operation)
V_{CTLC1H} / V_{CTLD1H} to V_{CTLC2H} / V_{CTLD2H}	Forced OFF
V_{SS} to V_{CTLC2H} / V_{CTLD2H}	ON (Normal operation)

When V_{DD} = 17 V (Refer to *"Electrical Characteristics"*),

V_{CTLC1H} / V_{CTLD1H}: Typ.18.1 V

V_{CTLC2H} / V_{CTLD2H}: Typ.16.1 V



CT1 and CT2 Pins

CT1 and CT2 pins are used for setting each output delay time of the overdischarge detection (t_{VDET2}), and the discharge overcurrent detection 1/2 (t_{VDET31} / t_{VDET32}) by connecting external capacitors C_{CT1} and C_{CT2}. t_{VDET2} can be set with CT1 pin. t_{VDET31} and t_{VDET32} can be set with CT2 pin. Each delay time can be calculated by following Equation 1:

$$CV = i\Delta t \quad \text{Equation 1}$$

■ Delay time (t_{VDET2}) setting with external capacitor (C_{CT1})
By substitution of Equation1,

$$t_{VDET2} = C_{CT1} \times V_{DCT1} / I_{CT1} \quad \text{Equation 2}$$

If C_{CT1} = 33 nF, V_{DCT1} = 1.8 V, I_{CT1} = 500 nA (Refer to *"Electrical Characteristics"*).
When substituting values to Equation 2, t_{VDET2} is as follow;

$$t_{VDET2} = 33\ nF \times 1.8\ V / 500\ nA$$
$$= 118.8\ ms$$

■ Delay time (t_{VDET31}, t_{VDET32}) setting with external capacitor (C_{CT2})
By substitution of Equation1,

$$t_{VDET31} = C_{CT2} \times V_{DCT2} / I_{CT2} \quad \text{Equation 3}$$
$$t_{VDET32} = t_{VDET31} / 6 \quad \text{Equation 4}$$

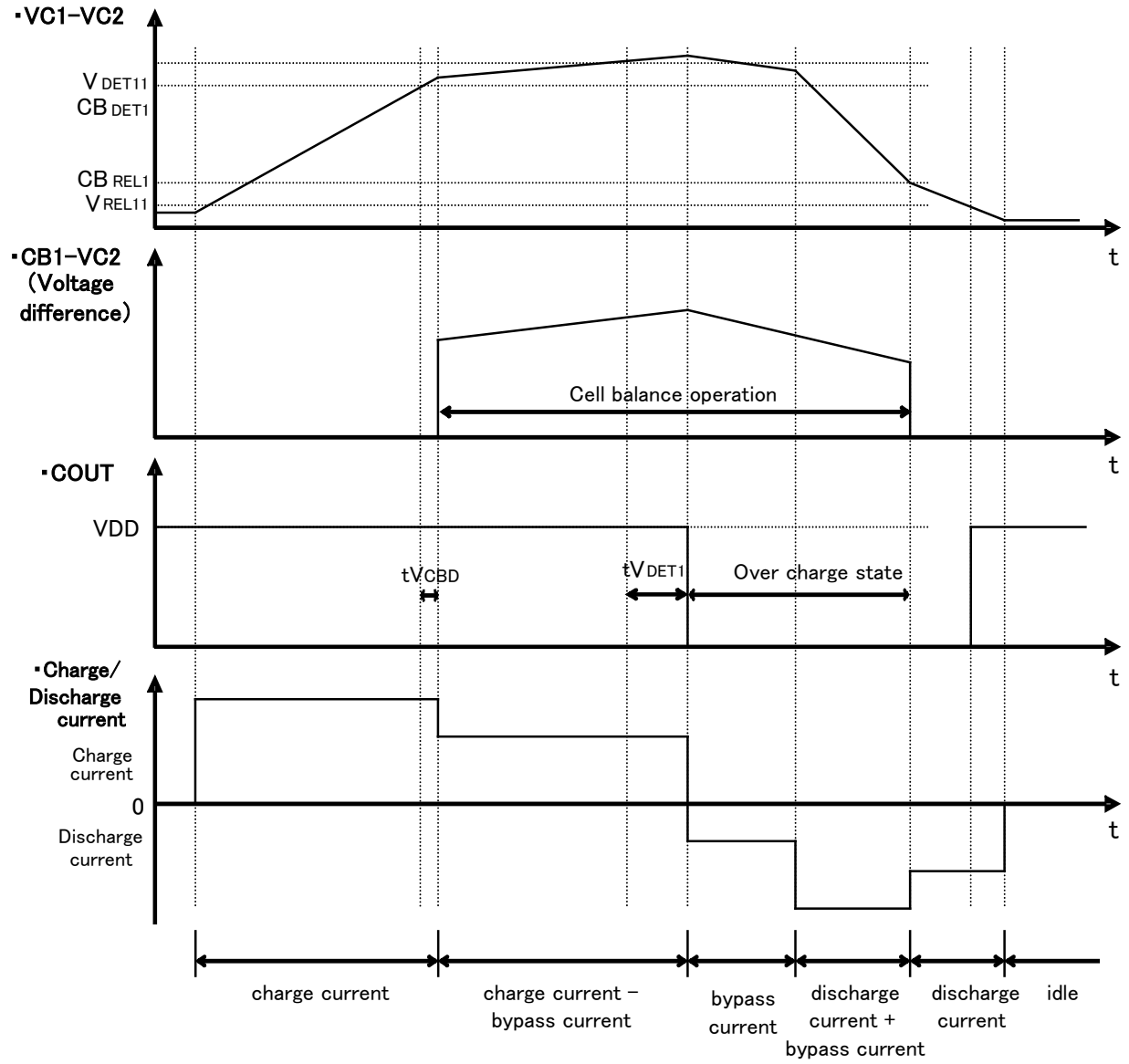
If C_{CT1} = 3.3 nF, V_{DCT1} = 1.5 V, I_{CT1} = 500 nA (Refer to *"Electrical Characteristics"*).
When substituting values to Equation 3 / Equation 4, t_{VDET31} and t_{VDET32} are as follow;

$$t_{VDET31} = 3.3\ nF \times 1.5\ V / 500\ nA$$
$$= 9.9\ ms$$
$$t_{VDET32} = 9.9\ ms / 6$$
$$= 1.65\ ms$$

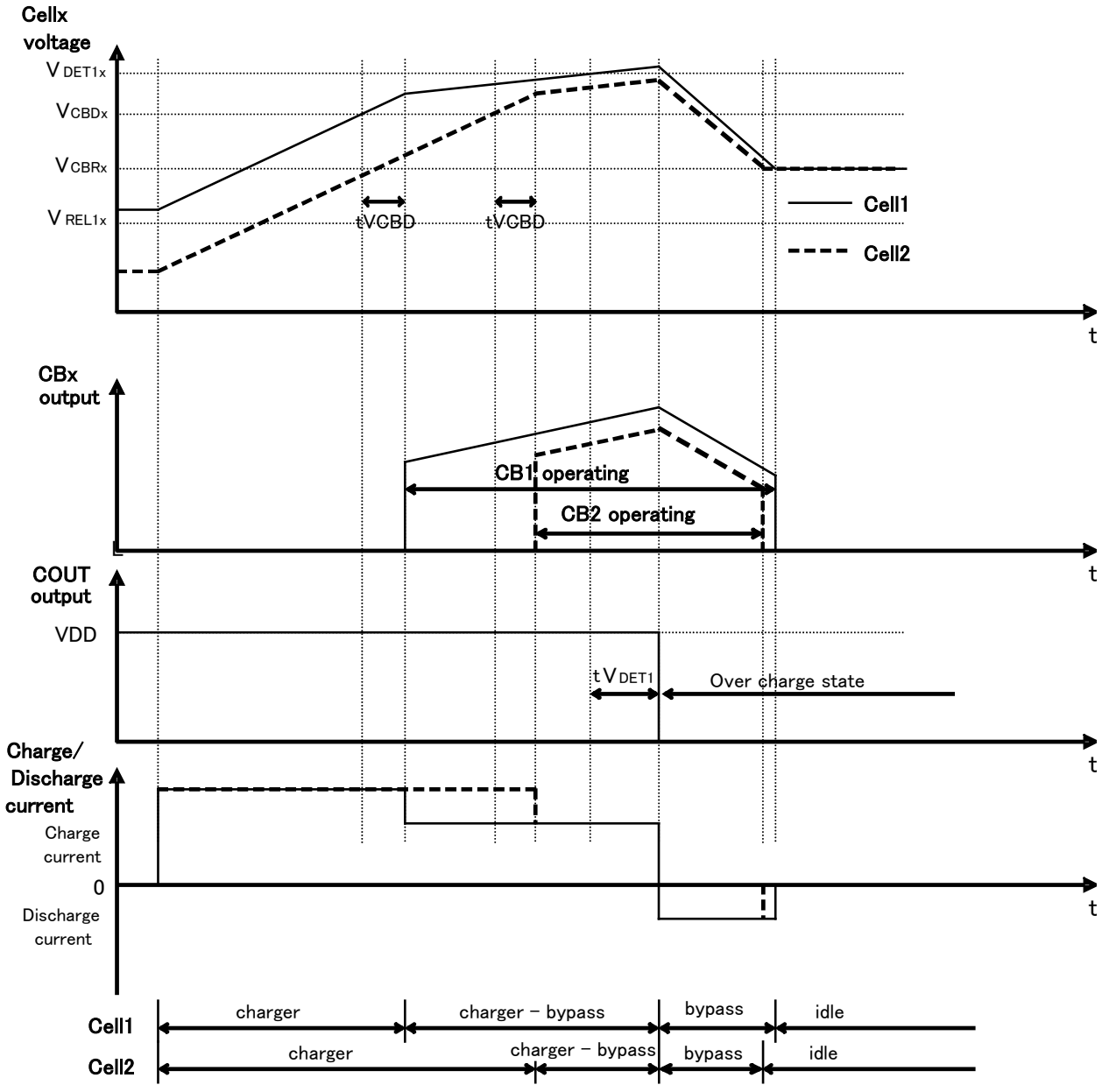
Cell Balance Function

When the cell voltage exceeds the cell balance detection voltage (V_{CBDn}, n=1,2,3,4,5), CBn pin become "High" by cell balancing. By turning ON an external Nch. FET for cell balance, a current flows through the discharge path in parallel with the cell in order to reduce the charging current or to discharge the cell voltage. And, when the cell voltage is less than the cell balance release voltage (V_{CBRn}, n=1,2,3,4,5), CBn pin become

“Low” after the cell balancing is released, and the external Nch. FET is turned OFF. When not using this function, CBn pin must be open.



CELL1 Balancing Timing Chart



CELL1/2 Balancing Timing Chart

Open-wire Detection (R5436TxxxBA only)

When using the 5-cell protection, the voltage of VDD (= VC1) becomes lower than VC2 voltage if the connection between the battery and VDD (= VC1) is open. And, the voltage of VSS (= VSS0) becomes higher than VC5 voltage if the connection between the battery and VSS (= VSS0) is open. The voltage variation is detected as “Open-wire”. When the open-wire is detected, COUT becomes “HI-z” and DOUT becomes “Low”. But, if VC1 or VSS0 line is cut off when each VC1 and VSS0 pins are connected with separate lines, only DOUT pin will become “Low”. Likewise, as for an open-wire detection between VDD and VSS pins, if VDD or VSS line is cut off, COUT pin will become “Hi-z” and DOUT pin will become “Low”.

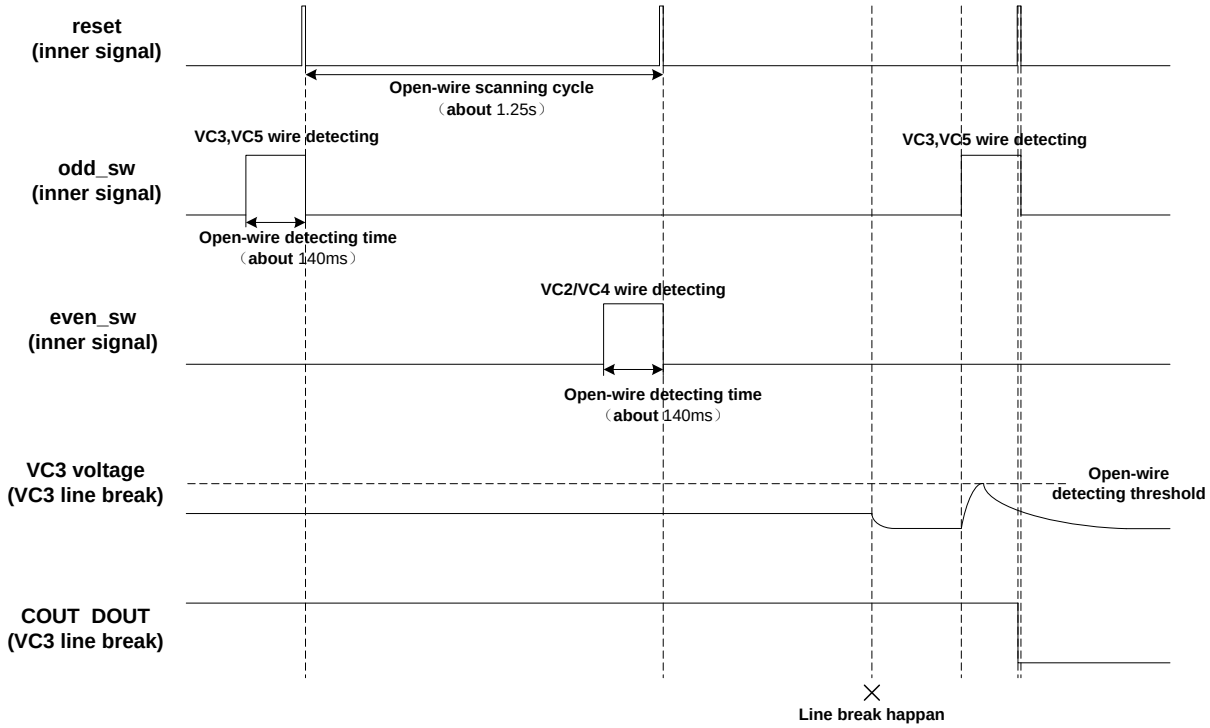
Open-wire detection for VC2, VC3, VC4, and VC5 is performed at interval of 1.25 seconds. The cell switch for VC1, VC3, and VC5 and the cell switch for VC2 and VC4 are alternately turned ON by even_sw and odd_sw signals. The internal impedance between pins, which are turned the switch ON, is lowered for about 140 ms. If not detecting the open-wire, this cycle will exit and the next cycle will start. If detecting the open-wire, the VC voltage will be shifted according to the difference of the internal impedance caused by turning ON either of two switches. This voltage change is detected during the delay time of 0.5 ms or more, the open-wire detection works. Then, COUT pin becomes “Hi-z” and DOUT pin becomes “Low”. By applying a certain voltage to SEL1 and SEL2 pins, the open-wire detection for VC2, VC3, VC4, and VC5 is disabled. The open-wire detection is disabled even when this device is in standby mode - but the open-wire detection for VDD and VSS lines is enabled.

When using the 10-cell protection, if VSS of the higher-voltage device and VDD of the lower-voltage device in cascade connection are connected with the battery’s line, an open-wire in this line cannot be detected.

[Limitations of Open-wire detection for VC2, VC3, VC4, and VC5]

When using the open-wire detection for VC2, VC3, VC4, and VC5, confirm the limitations below:

- The cycle time of open-wire detection is 1.25 second, and the open-wire detection is performed for 140 ms in each cycle. The device controls these internal-set times.
- When the battery voltage is lower even when this device is not in standby, an open-wire might not be detected due to some factors: the device’s distribution, the cell balancing in the battery, the operating environment, the characteristics of the external components, etc.
- During the overcharge detection delay time, the device does not shift to the open-wire detection until the overcharge detection is finished. The overcharge detection does not start even if the battery voltage is higher than the overcharge detection voltage. After the completion of the open-wire detection, the overcharge detection will start if the battery voltage is more than the overcharge detection voltage. That is, the overcharge detection delay time increases for the time required for the open-wire detection.
- Likewise, the device does not shift to the open-wire detection during the overdisharge detection delay time, and the device does not start the overdischarge detection when the battery voltage is less than the overdischarge detection voltage during the open-wire detection. But, after the completion of the open-wire detection, the overdischarge detection delay time increases for the time required for the open-wire detection.



Open-wire Detection Timing Chart

Temperature Protection by External NTC

The temperature protection is realized with VR and TEP pins. VR pin supplies a source voltage to be divided by a series of resistors of R_{TEP} and NTC. The divided voltage becomes an input to TEP pin.

When rising of the temperature under the NTC's supervising, TEP pin voltage, which is the divided voltage, rises depending on a reduction of the NTC resistance value. When the delay time (t_{T_DET}) has passed while holding the divided voltage being higher than the temperature protection detection voltage (V_{T_DET}), the temperature protection will function, and changing COUT pin to "Hi-z" and DOUT pin to "Low" can stop charging/ discharging. After the temperature falling, the delay time (t_{T_REL}) has passed while holding the divided voltage being lower than the temperature protection release voltage (V_{T_REL}), COUT and DOUT pins return "High", and charging / discharging is available.

VR pin cannot supply a large current because of supplying a source voltage for the voltage divider. In standby mode, the temperature protection stops since VR pin becomes "Low" to reduce the consumption current. When using the temperature protection at desired temperature, each resistance value of NTC and R_{TEP} can be calculated by following Equation:

$$\frac{R_{TEP}}{R_{TEP} + R_{NTC}} \times VR = \frac{20}{21} \times VR$$

$R_{TEP} = 20\ R_{NTC}$

For example, when using the following requirements:

NTC resistor: SNS104B24B24360FE1L050ET

Available temperature for protection: 65°C

R_{NTC} = 17.63 kΩ (at 65°C)

Then,

$R_{TEP} = 20 \times R_{NTC}$

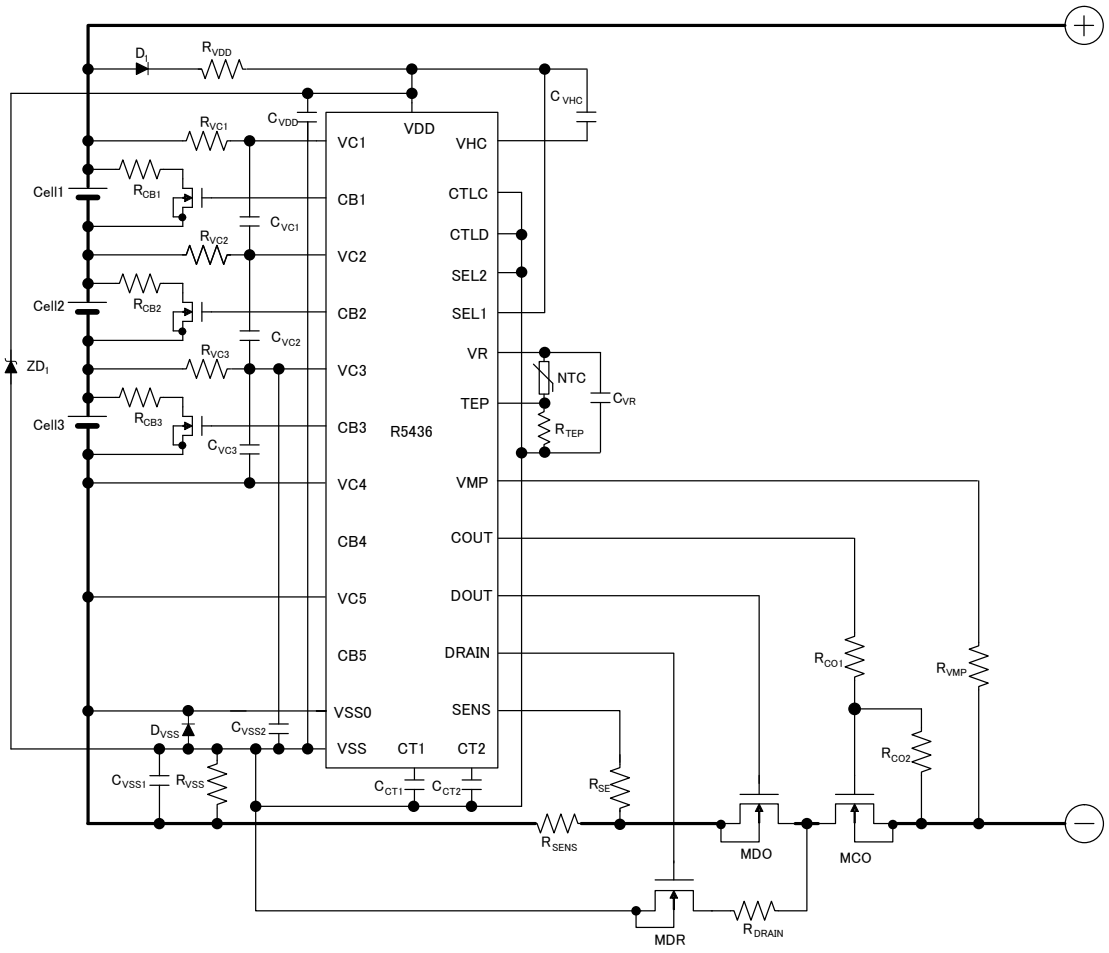
$= 352.6$ (kΩ)

As a result, choose a nearest value and normal type resistance: R_{TEP}=348KΩ.

APPLICATION INFORMATION

Typical Application Circuits 1

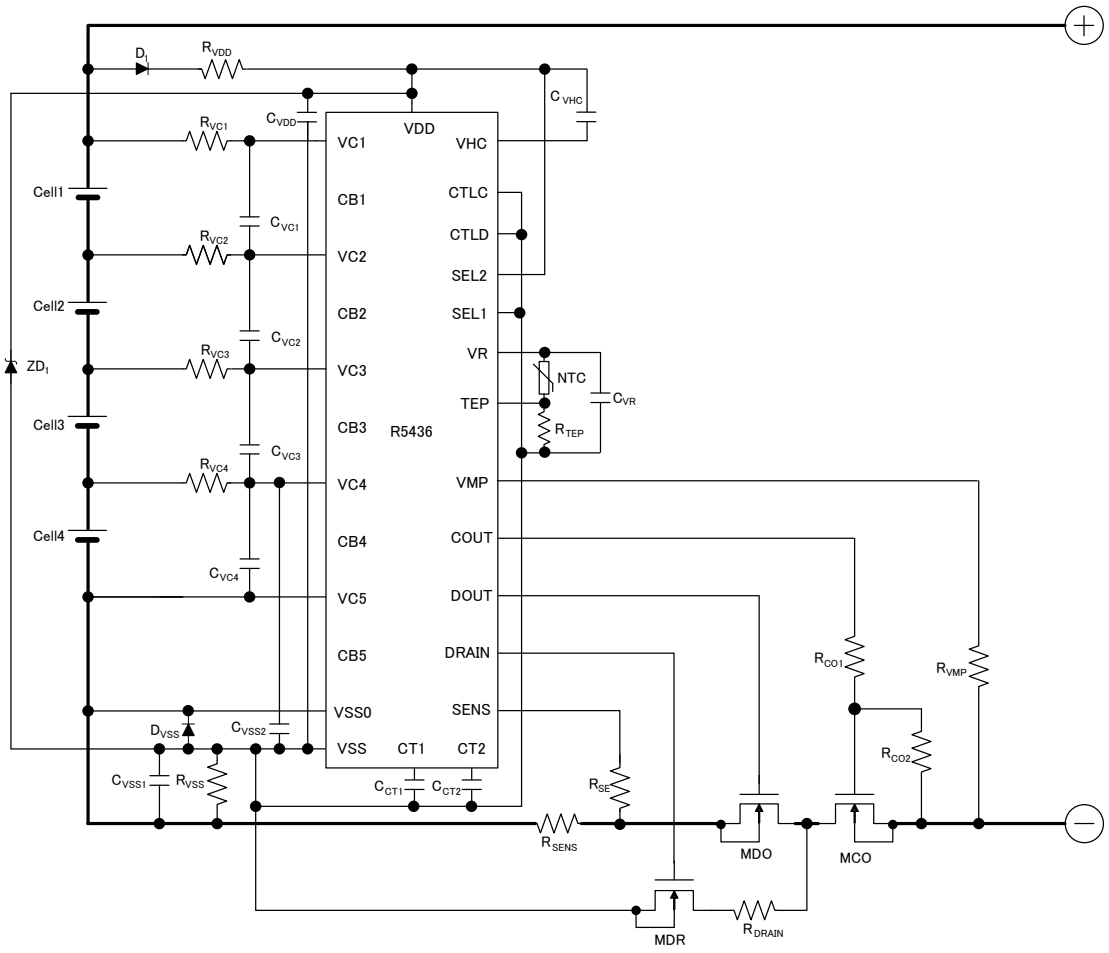
3-cell Protection Battery Charger



Typical Application Circuit for 3-cell Protection Battery Charger

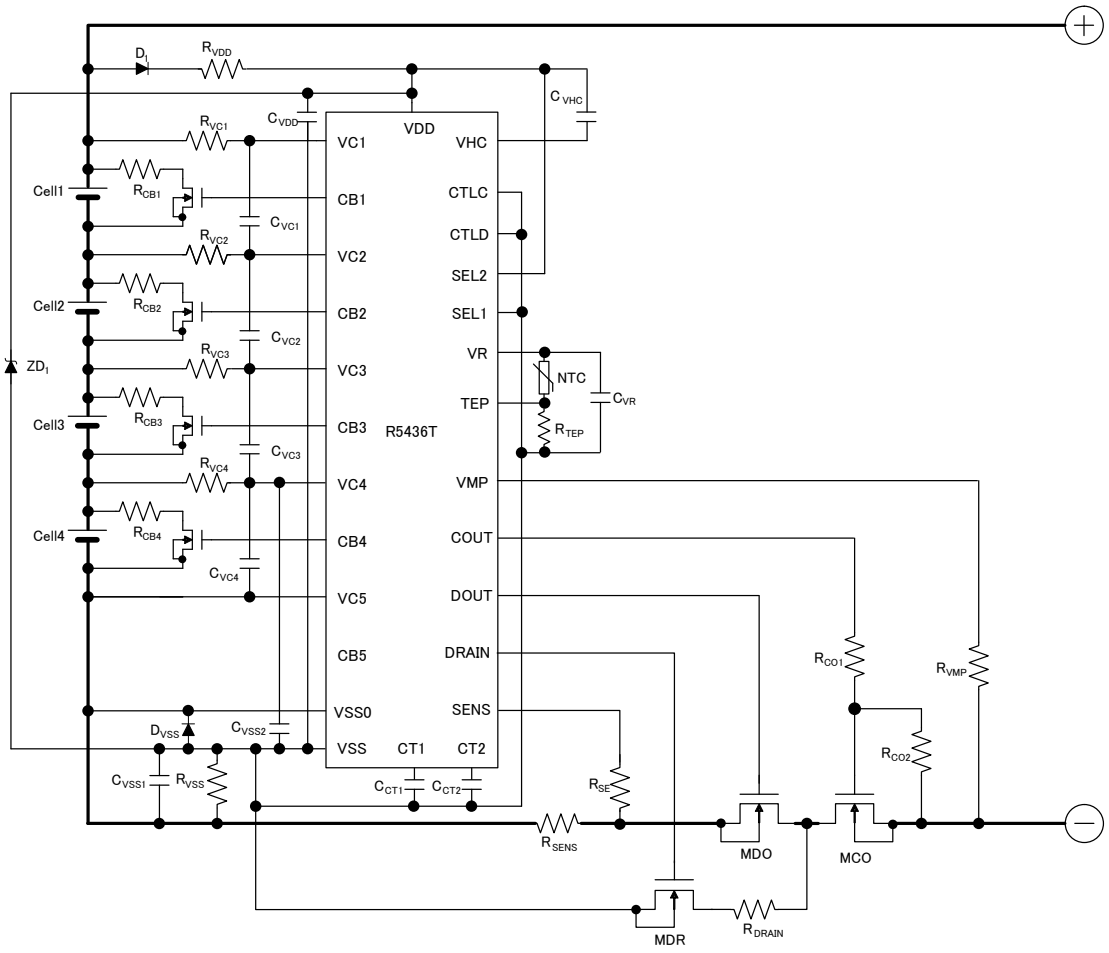
Typical Application Circuits 2

4-cell Protection Battery Charger with Cell-balancing Disabled



Typical Application Circuit for 4-cell Protection Battery Charger with Cell-balancing Disabled

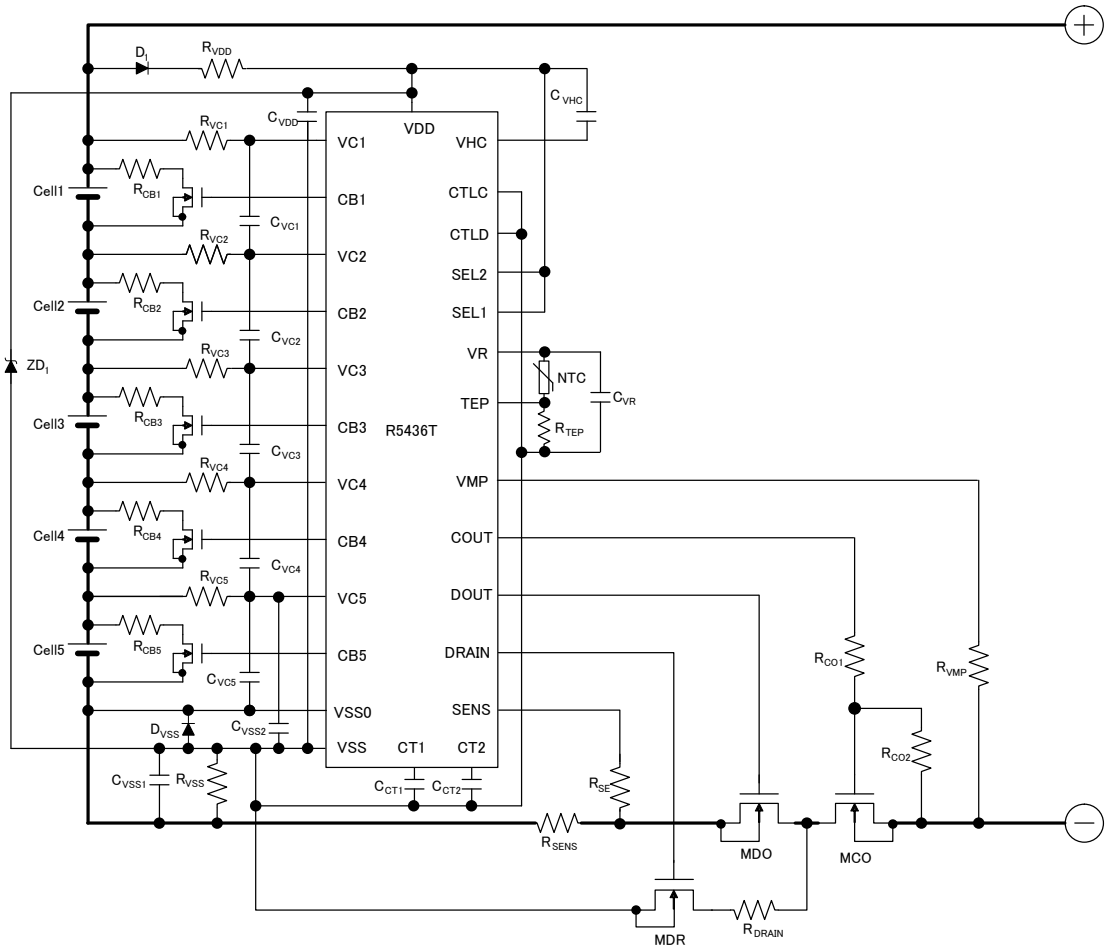
4-cell Protection Battery Charger with Cell-balancing Enabled



Typical Application Circuit for 4-cell Protection Battery Charger with Cell-balancing Enabled

Typical Application Circuits 3

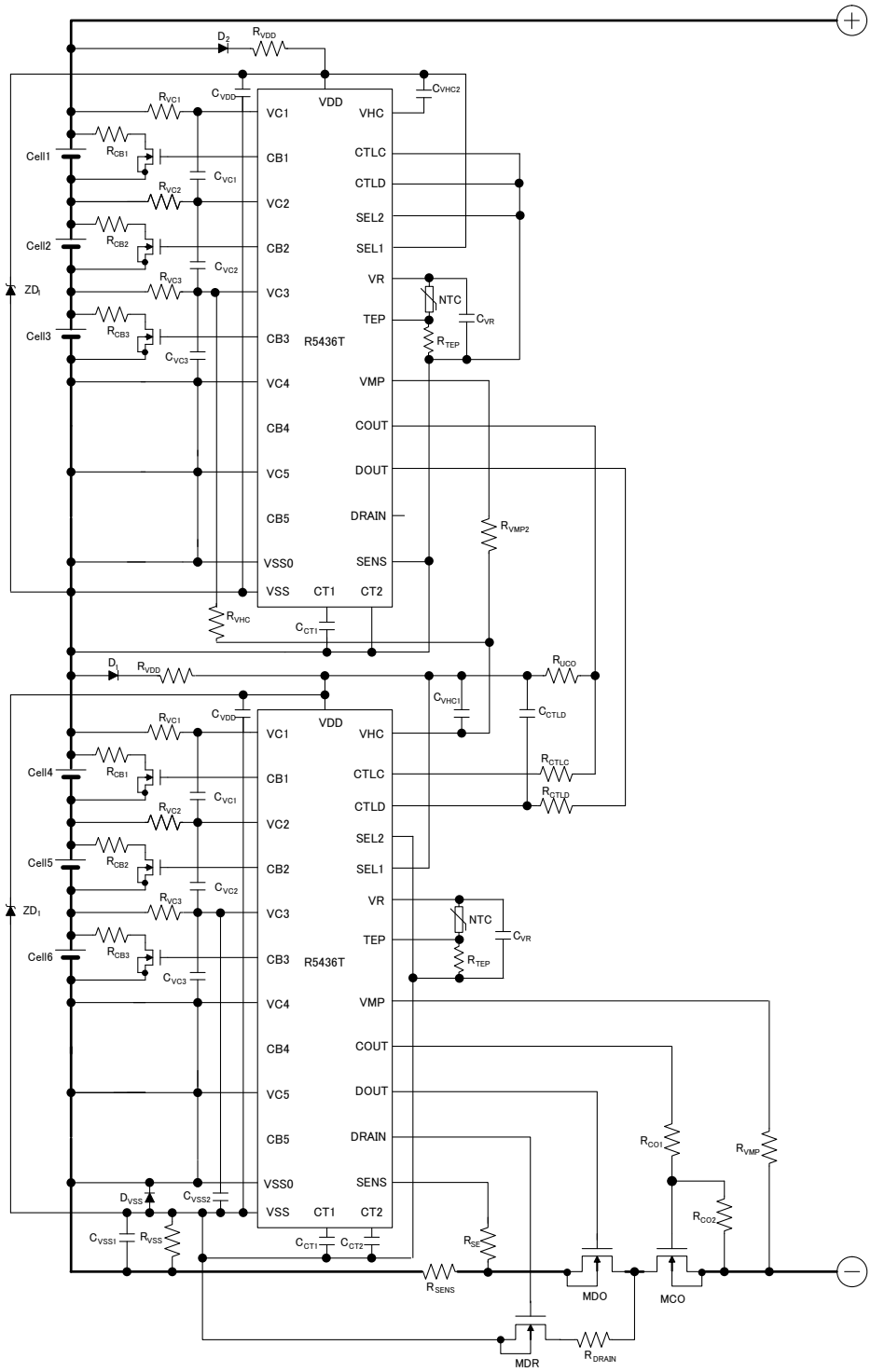
5-cell Protection Battery Charger with Cell-balancing Enabled



Typical Application Circuit for 5-cell Protection Battery Charger with Cell-balancing Enabled

Typical Application Circuits 4

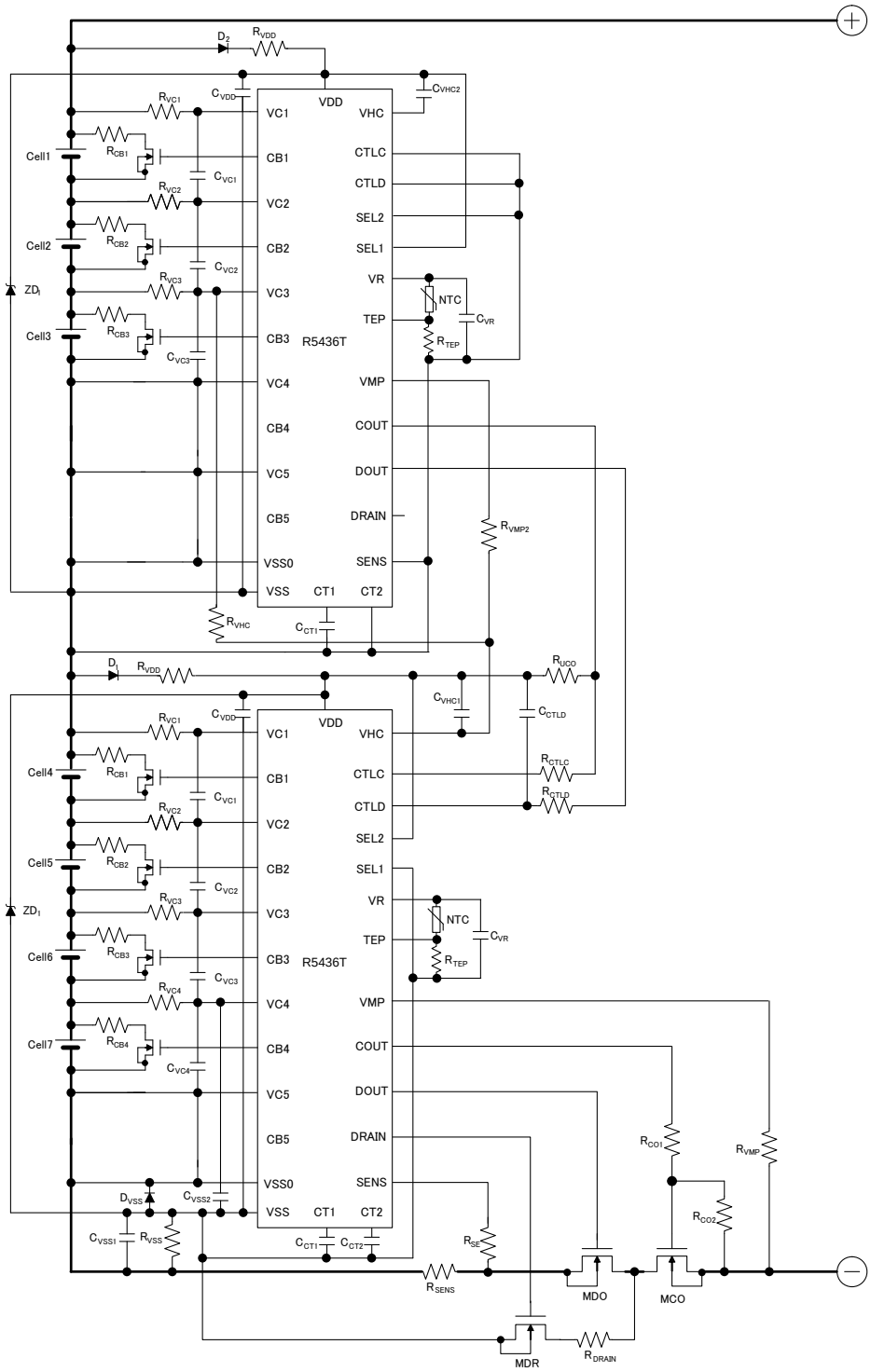
6-cell Protection Battery Charger with Cell-balancing Enabled



Typical Application Circuit for 6-cell Protection Battery Charger with Cell-balancing Enabled

Typical Application Circuits 5

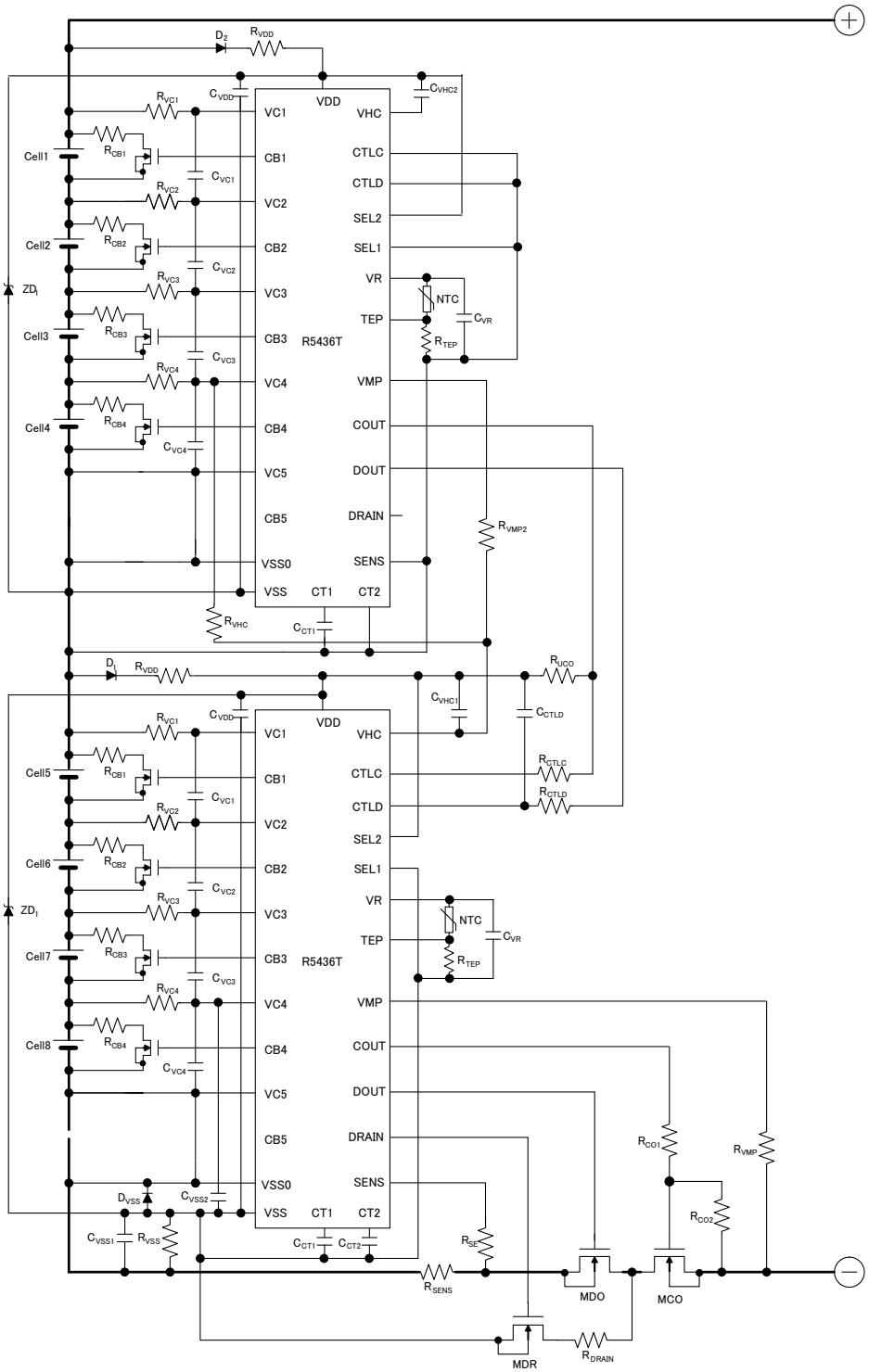
7-cell Protection Battery Charger with Cell-balancing Enabled



Typical Application Circuit for 7-cell Protection Battery Charger with Cell-balancing Enabled

Typical Application Circuits 6

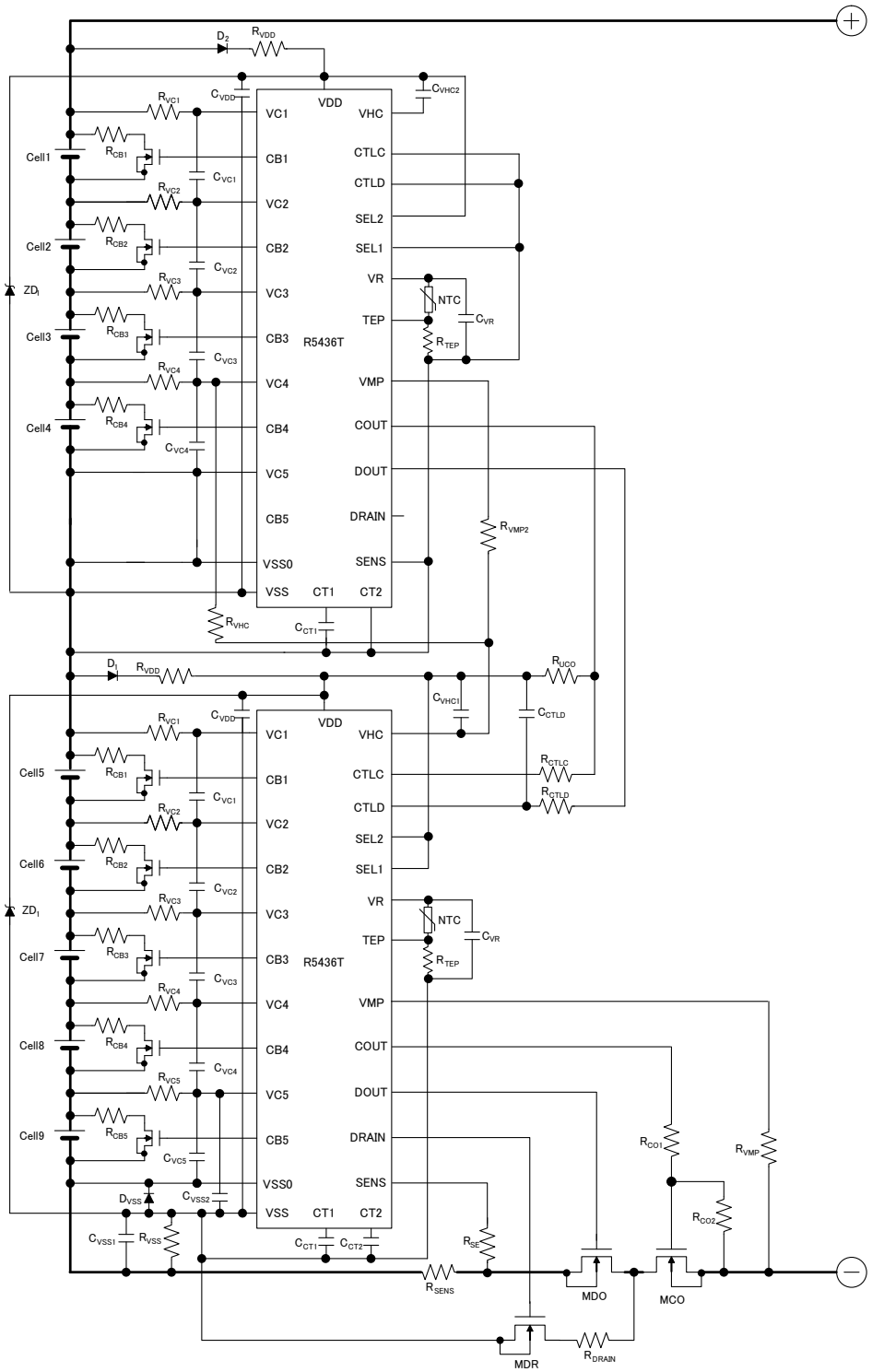
8-cell Protection Battery Charger with Cell-balancing Enabled



Typical Application Circuit for 8-cell Protection Battery Charger with Cell-balancing Enabled

Typical Application Circuits 7

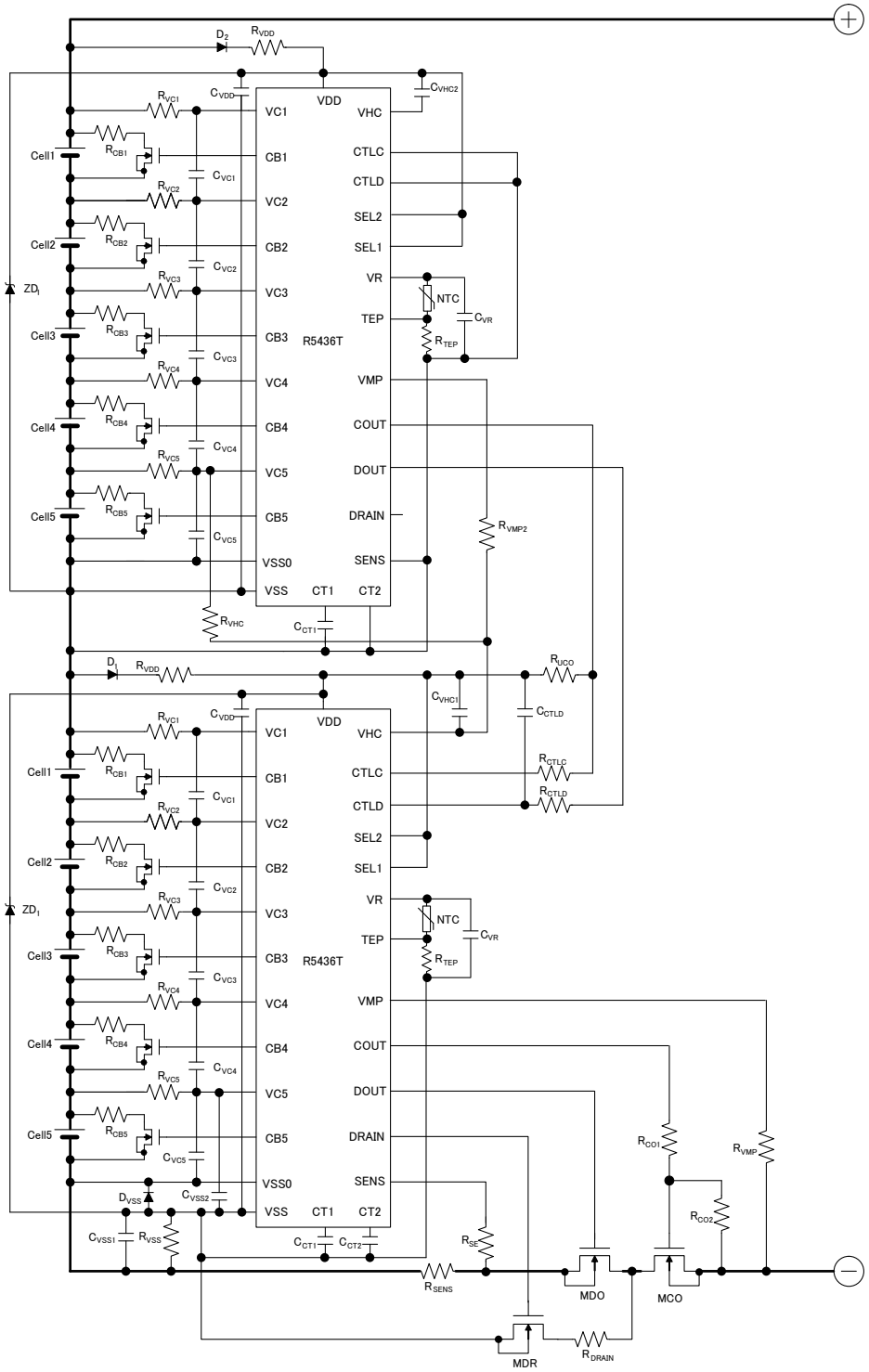
9-cell Protection Battery Charger with Cell-balancing Enabled



Typical Application Circuit for 9-cell Protection Battery Charger with Cell-balancing Enabled

Typical Application Circuits 8

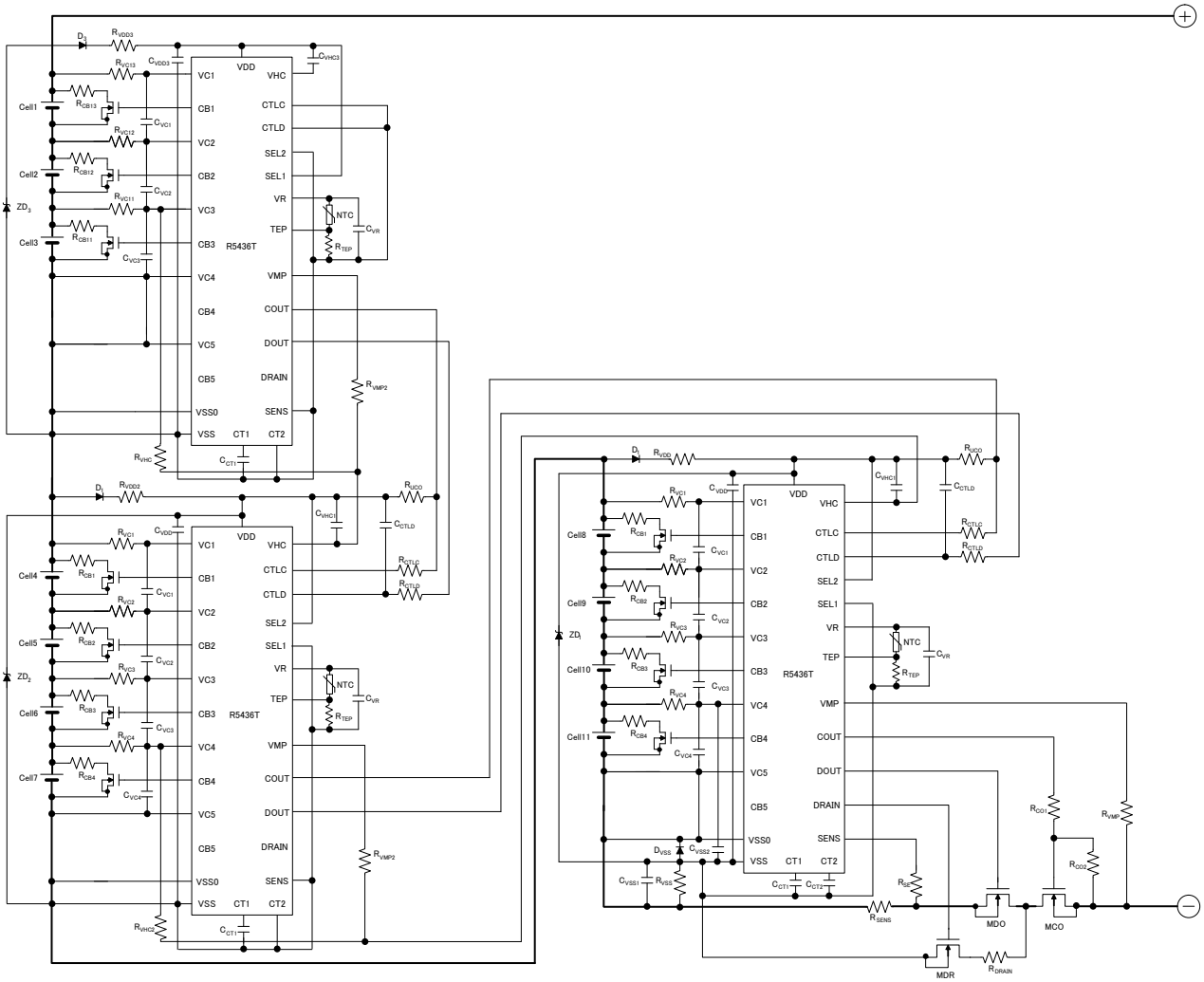
10-cell Protection Battery Charger with Cell-balancing Enabled



Typical Application Circuit for 10-cell Protection Battery Charger with Cell-balancing Enabled

Typical Application Circuits 9

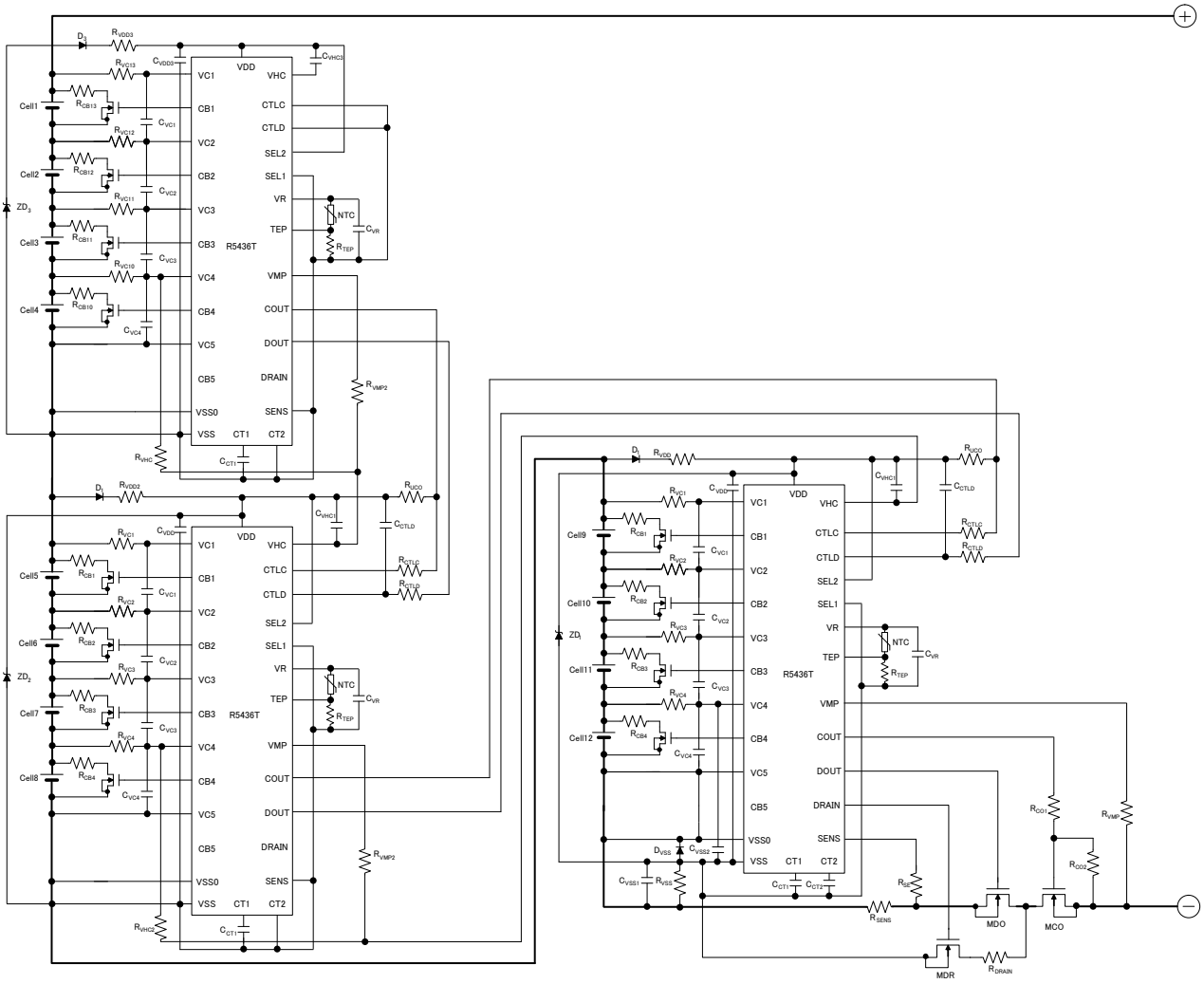
11-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)



Typical Application Circuit for 11-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)

Typical Application Circuits 10

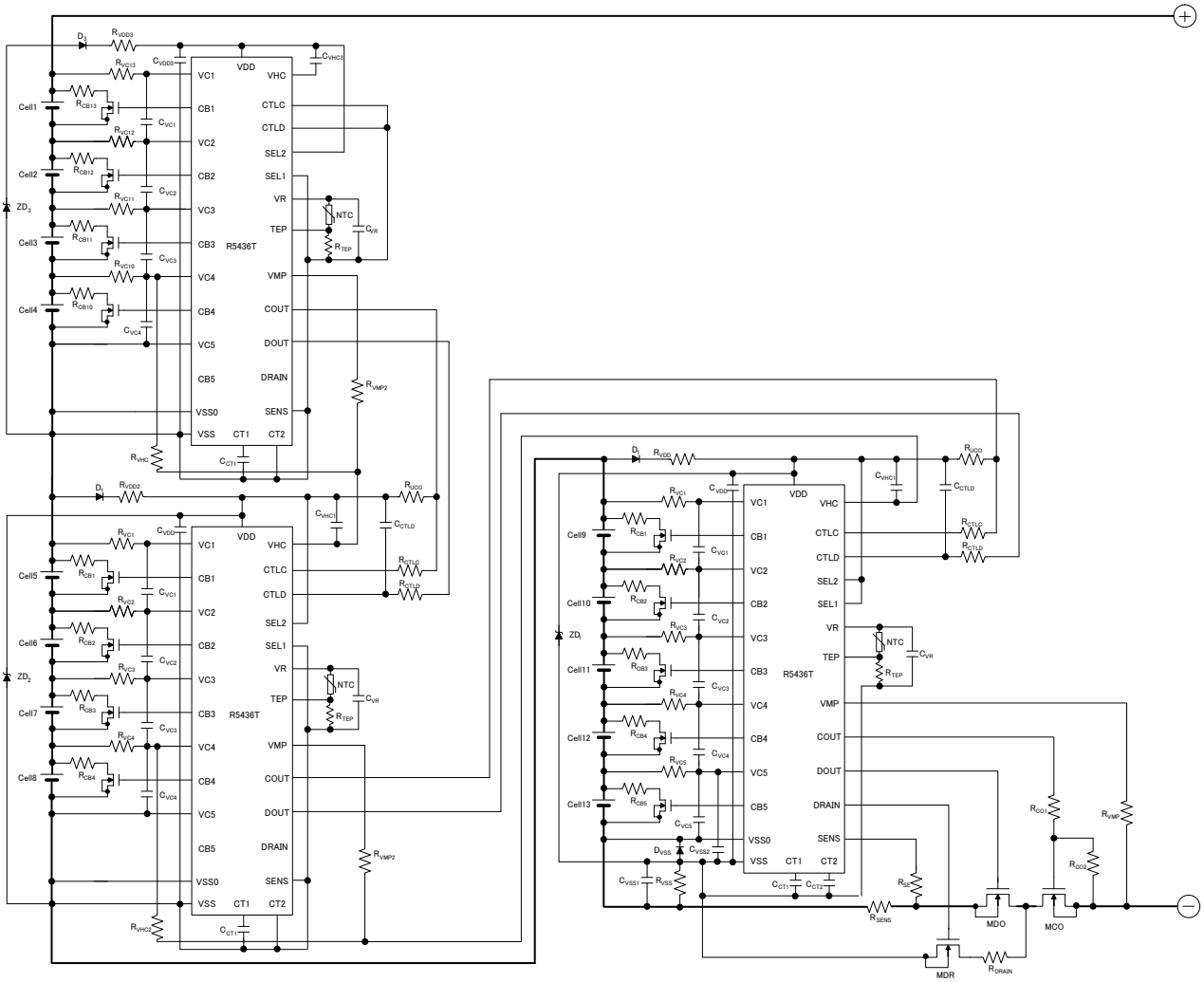
12-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)



Typical Application Circuit for 12-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)

Typical Application Circuits 11

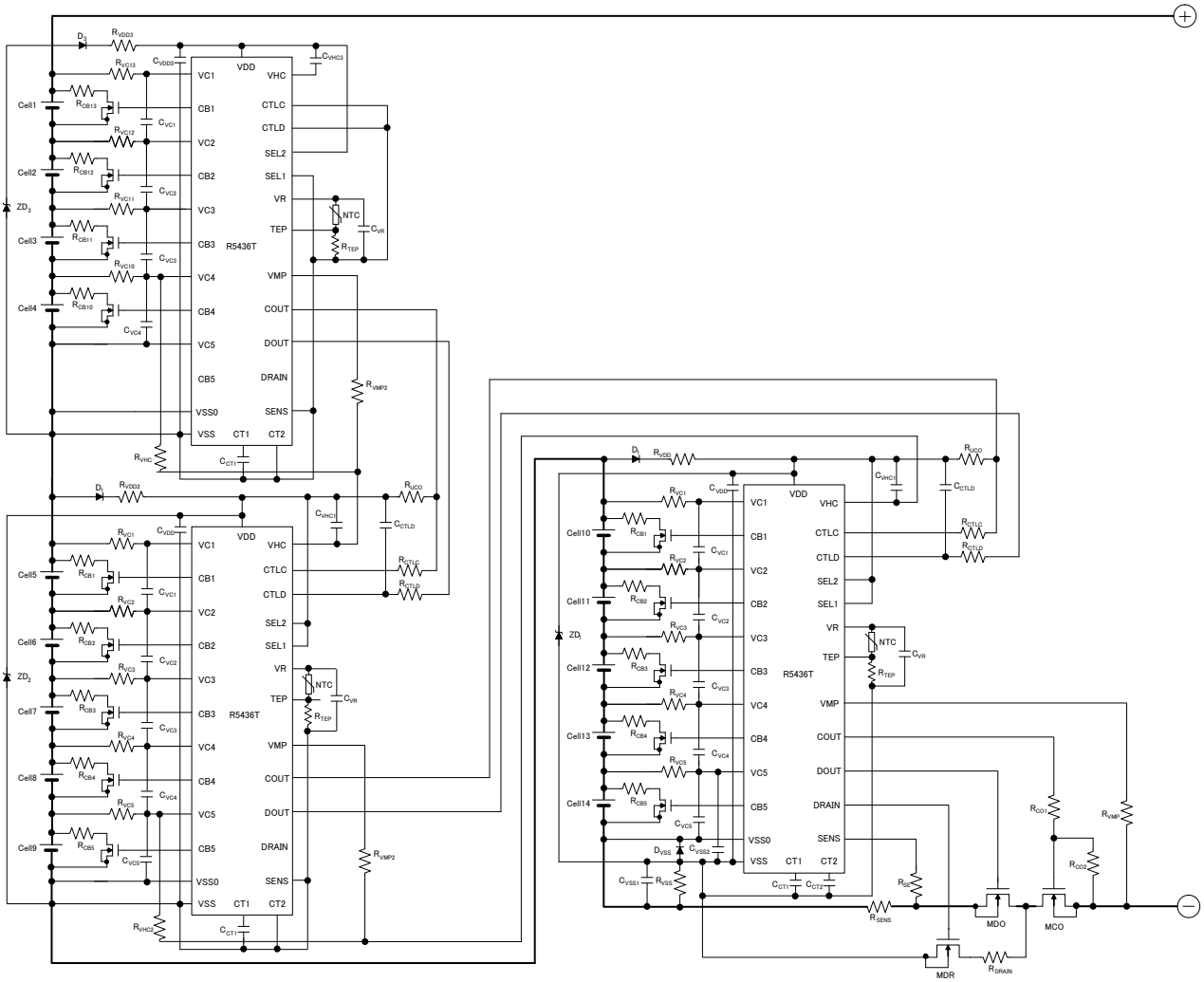
13-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)



Typical Application Circuit for 13-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)

Typical Application Circuits 12

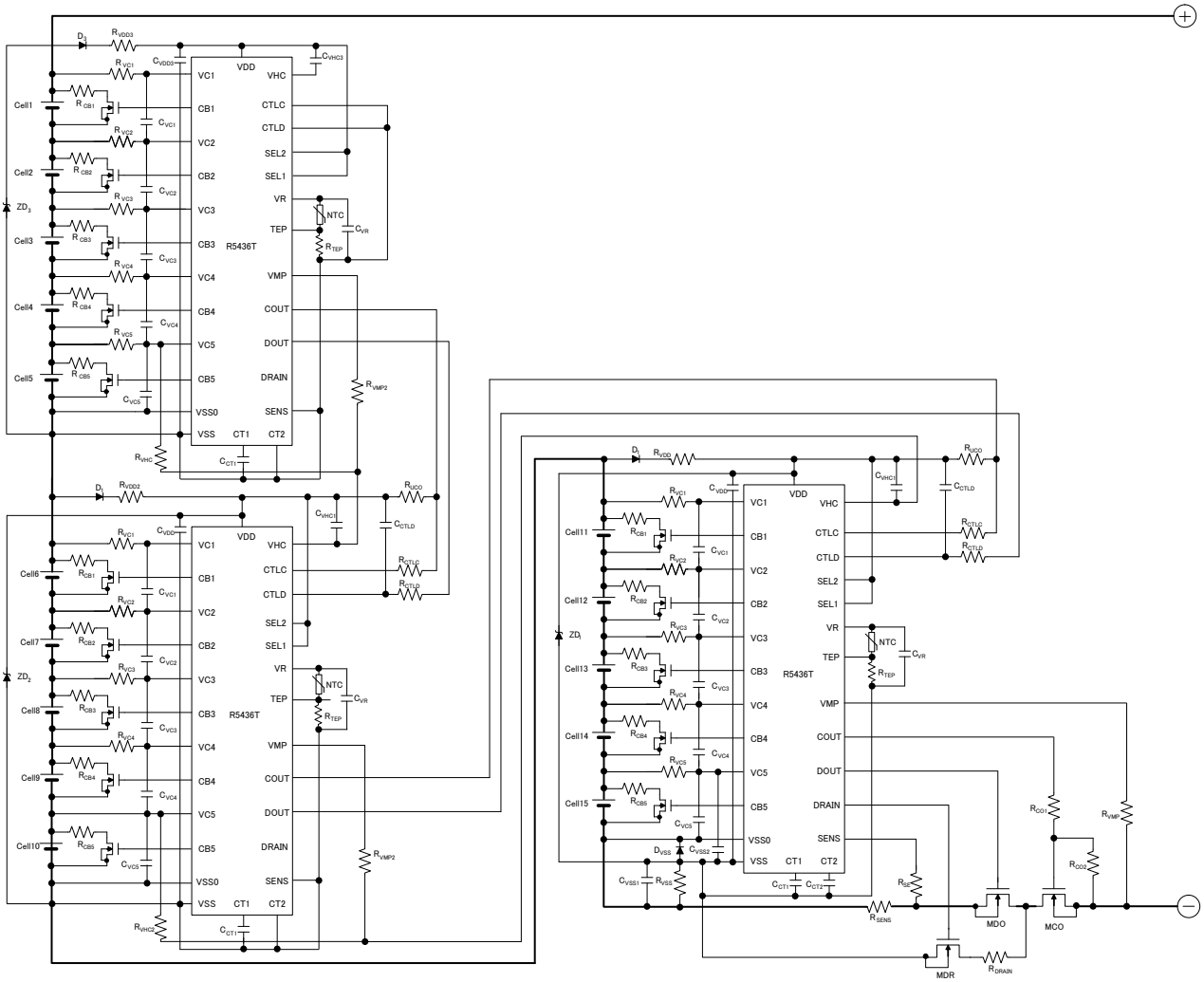
14-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)



Typical Application Circuit for 14-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)

Typical Application Circuits 13

15-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)



Typical Application Circuit for 15-cell Protection Battery Charger with Cell-balancing Enabled (Cascade Connection)

External Components

Symbol	Value (Typ.)	Range	Unit	Remarks[1]
R_{VDDX}	330	330 to 1000	Ω	Refer to *Technical Note [1]*.
R_{VC1X}	330	330 to 1000	Ω	Refer to *Technical Note [2]*.
R_{VC2X}	330	330 to 1000	Ω	
R_{VC3X}	330	330 to 1000	Ω	
R_{VC4X}	330	330 to 1000	Ω	
R_{VC5X}	330	330 to 1000	Ω	
R_{CB1X}	100	Note [3]	Ω	Refer to *Technical Note [3]*.
R_{CB2X}	100	Note [3]	Ω	
R_{CB3X}	100	Note [3]	Ω	
R_{CB4X}	100	Note [3]	Ω	
R_{CB5X}	100	Note [3]	Ω	
R_{SENS}	100	1 or more	mΩ	Depending on Set Value of Overcurrent
R_{SE}	10	1 to 10	kΩ	Refer to *Technical Note [4]*.
R_{DRAIN}	75	Note [5]	kΩ	Refer to *Technical Note [5]*.
R_{CO1}	1	Note [5]	MΩ	
R_{CO2}	2	Note [5]	MΩ	
R_{VMP1}	10	0.01 to 10	MΩ	Refer to *Technical Note [6]*.
R_{VMP2}	1	1	MΩ	
R_{VMP3}	1	1	MΩ	
R_{CTLC}	1	1 to 10	kΩ	-
R_{CTLD}	10	10 to 100	kΩ	Refer to *Technical Note [17]*.
R_{UCOX}, R_{UDO}	3	3	MΩ	Refer to *Technical Note [7] and [19]*.
R_{VSS}	10	10	Ω	Refer to *Technical Note [15]*.
C_{VSS1}	1	1	µF	
C_{VSS2}	1	0.1 to 1	µF	
C_{VDDX}	1	0.1 to 1	µF	Refer to *Technical Note [1]*.
C_{VC1X}	0.1	0.1	µF	Refer to *Technical Note [2]*.
C_{VC2X}	0.1	0.1	µF	
C_{VC3X}	0.1	0.1	µF	
C_{VC4X}	0.1	0.1	µF	
C_{VC5X}	0.1	0.1	µF	
C_{CT1X}	33	10 to 1000	nF	-

[1] Refer to "*Technical Notes for External Components*" for details.

Symbol	Typ.Value	Range	Unit	Remarks[1]
C_{CT2X}	3.3	2.2 or more	nF	Refer to *Technical Note [8]*.
C_{VRX}	1	1	µF	Refer to *Technical Note [9]*.
C_{CTLD}	33	10 to 100	nF	Refer to *Technical Note [17]*.
C_{VHCX}	10	3.3 to 10	nF	Refer to *Technical Note [18]*.
ZD_X	30	30 or less	V	Refer to *Technical Note [10]*. Recommended Component: MM1Z30_0.5W_30V_J_SOD-123_EIC
R_{VHCX}	5	5 to 10	MΩ	Refer to *Technical Note [11]*.
R_{TEPX}	350	300 and more	kΩ	Refer to *Technical Note [12]*. 100 kΩ level at ambient temperature
NTC_X	100	100	kΩ	Refer to *Technical Note [12]*.
SBD_{VSS}		−	−	Refer to *Technical Note [15]*. Recommended Component: RB491D_SOT-23
D_X		−	−	Refer to *Technical Note [16]*. Recommended Component: 1N4148_100mA/100V_4nS_SOT-23
MCO		−	−	Refer to *Technical Note [13]*.
MDO		−	−	
MDR		−	−	Refer to *Technical Note [14]*.

[1] Refer to "*Technical Notes for External Components*" for details.

Component Selection Guide

- The typical application circuit diagrams are just examples. The operation in application circuits is not guaranteed. Be sure to perform a sufficient evaluation with the external components under the actual usage conditions for selection.

- Be careful not to apply the overvoltage and the overcurrent which exceed the rating to the protection IC and external components. Especially, select an FET with enough current capacity to endure the large current because a large current might flow through the FET during the time between an overcharge detection a blown fuse.

Technical Notes for External Components

【1】The voltage fluctuation is stabilized with R_{VDD} and C_{VDD}. If a small R_{VDD} is set, in the case of the large transient may happen to the cell voltage, by the flowing current, the IC may be unstable. If a large R_{VDD} is set, by the consumption current of the IC itself, the voltage difference between VDD pin and VC1 pin is generated, and unexpected operation may result. Therefore, the appropriate value range of R_{VDD} is from 330Ω to 1kΩ. To make a stable operation of the IC, the appropriate value range of C_{VDD} is from 0.1μF to 1.0μF.

【2】R_{VCxx}, C_{VCxx} stabilize the voltage fluctuation. If large R_{VCxx} is set, the detector threshold will be high because of the internal conduction current of the IC. The operation error of open-wire detector function may happen easily by the distribution of the ICs or environment. If small R_{VCxx} is set, the effect by noise will be large. Therefore the appropriate value range of R_{VCxx} is from 330Ω to 1kΩ. To make stable operation, use 0.1μF as C_{VCxx}.

【3】When the cell balance function is necessary, R_{CBxx} must be chosen carefully with considering the bypass current, and consumption power by the bypass current, and the external MOSFET. Especially, if a small resistance (to set the large bypass current) is set, fully evaluation is necessary. If a large resistance (to set the small bypass current) is set, the time for cell balance will be long.

【4】When the cascade connection is used, if short circuit is happened, by the short current and the RSENS enlarges the voltage, and as a result, if the voltage of SENS pin becomes larger than the VDD of the IC, during the short circuit output delay time, the current flows into SENS pin. Therefore, if a small R_{SE} is set, a large current may flow into SENS pin. If a large R_{SE} is set, the over-current detector threshold may shift. Therefore the appropriate value is around 10kΩ.

【5】Choose appropriate values for R_{DRAIN}, R_{CO1}, and R_{CO2} to satisfy the next equation, otherwise, the release from excess discharge current and short may be impossible.

$R_{DRAIN} < V_{REL3} \times (R_{CO1} + R_{CO2})/V_{DD}$

If small R_{CO1} or R_{CO2} is set, when the output of C_{OUT} is "H", the consumption current of protection circuit board increases. If large R_{CO1} or R_{CO2} is set, when the output of C_{OUT} is "Hi-z", the speed for pull-down the gate of the charge FET becomes slow and turning off the FET will be slow. Dividing between the "Hi-z" output and the resistance might be not enough to turn OFF the charge FET. If a small R_{DRAIN} is set, when the excess discharge current and short circuit is detected, the large current may flow until the load is removed.

【6】When the cascade connection is used, if DOUT turns off, VMP pin is pulled up via R_{VMP} to the top cell. In this case, the current flows via R_{VMP} and the internal diode, therefore, appropriate value must be chosen (usually MΩ level). If the cascade connection is not used, around 10kΩ is acceptable.

【7】Set R_{UCO} to satisfy $R_{UCO}=R_{CO1}+R_{CO2}$. If an extremely large resistance is set, when the output of C_{OUT} is "Hi-Z", by the dividing resistance, CTLC pin may not be pulled down. If a small resistance is used, when the output of C_{OUT} is "H", the consumption current via R_{UCO} increases.

【8】If a too small C_{CT2} is set, excess discharge current detector output delay time 2 becomes shorter than the short circuit output delay time. Therefore, use a capacitor with 0.0022μF or more.

【9】To make a stable VR output, it should connect a 1.0μF capacitor to VR pin.

【10】Considering the break-down of the resistors and capacitors to stabilize the fluctuation of the voltage, to avoid that the high voltage is directly forced to the IC, adding a zener diode is our recommendation. Connect the zener diode between VDD pin of the IC and VSS pin directly. (Refer to the typical application circuits.) Zener diode MM1Z30_0.5W_30V_J_SOD-123_EIC is recommended.

【11】When the cascade connection is used, the lower side IC can transfer the VMP signal to upper side IC through VHC pin by pulling up VHC pin to the upper side IC's VC5 level through RVHC. The recommended value of RVHC is 5MΩ. If the upper side IC works at 4-cell protection mode, VHC pin should be pulled up to upper side IC's VC4 level. If the upper side IC works at 3-cell protection mode, VHC pin should be pulled up to upper side IC's VC3 level.

【12】The temperature protection function is realized by the voltage divider between a resistor of R_{TEP} and an NTC thermistor. R_{TEP} is equal to 20 times R_{NTC} at the desired protecting temperature. Choose an NTC thermistor with a high resistance capability to reduce the IC consumption current since VR pin cannot supply a large current. Using the high-accuracy thermistor and resistor can be realized more high-accuracy temperature protection.

【13】As for the charge control FET (MCO) and the discharge control FET (MDO), be sure to perform a sufficient consideration of their maximum voltage tolerance, current rating, maximum power consumption and peak consumption when short-circuit.

【14】As for the pull-down FET (MDR), be sure to perform a sufficient consideration to its maximum voltage tolerance.

【15】Schottky Diode (SBD_{VSS}) is required to prevent VSS pin voltage from being larger than VSS0 pin voltage.

【16】Diode (D_X) is required to prevent a drop in the VDD pin voltage (V_{DD}), along with the battery voltage drop.

【17】C_{CTLD} and R_{CTLD} make CTLD pin's transmission stable.

【18】C_{VHC} makes VHC pin signal stable.

Ver. B

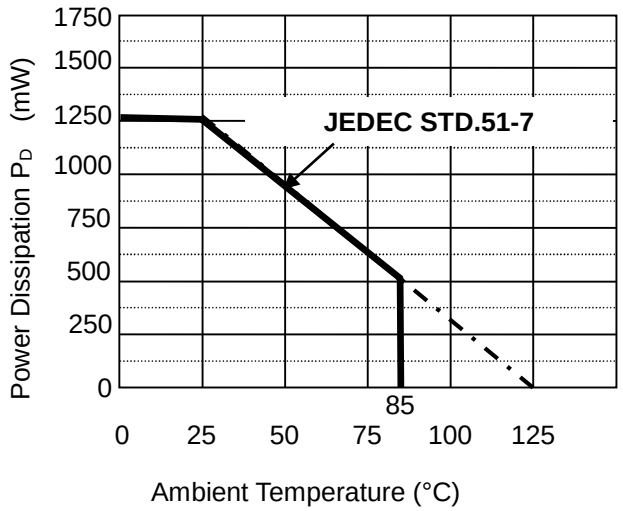
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

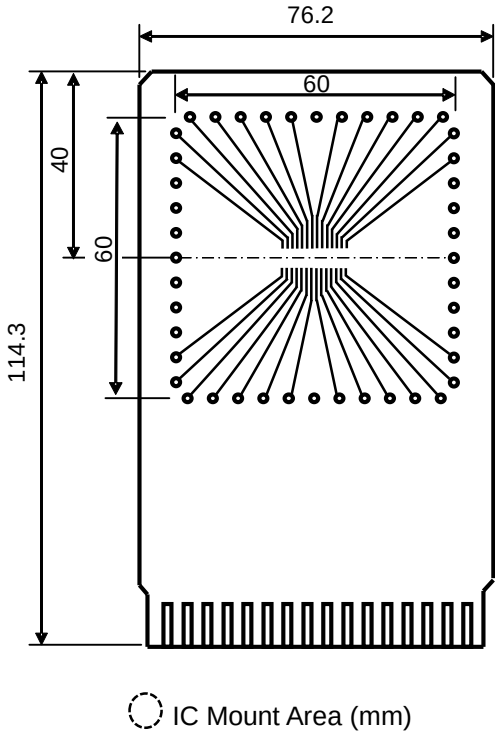
	JEDEC STD.51-7 Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layers (First and Fourth Layers): Less than 10% of 60 mm Square Inner Layers (Second and Third Layers): 100% of 74.2 mm Square
Through-holes	ϕ 0.85 mm × 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	JEDEC STD.51-7 Test Land Pattern
Power Dissipation	1250 mW
Thermal Resistance	θja = (125 − 25°C) / 1.25 W = 80°C/W θjc = 25°C/W



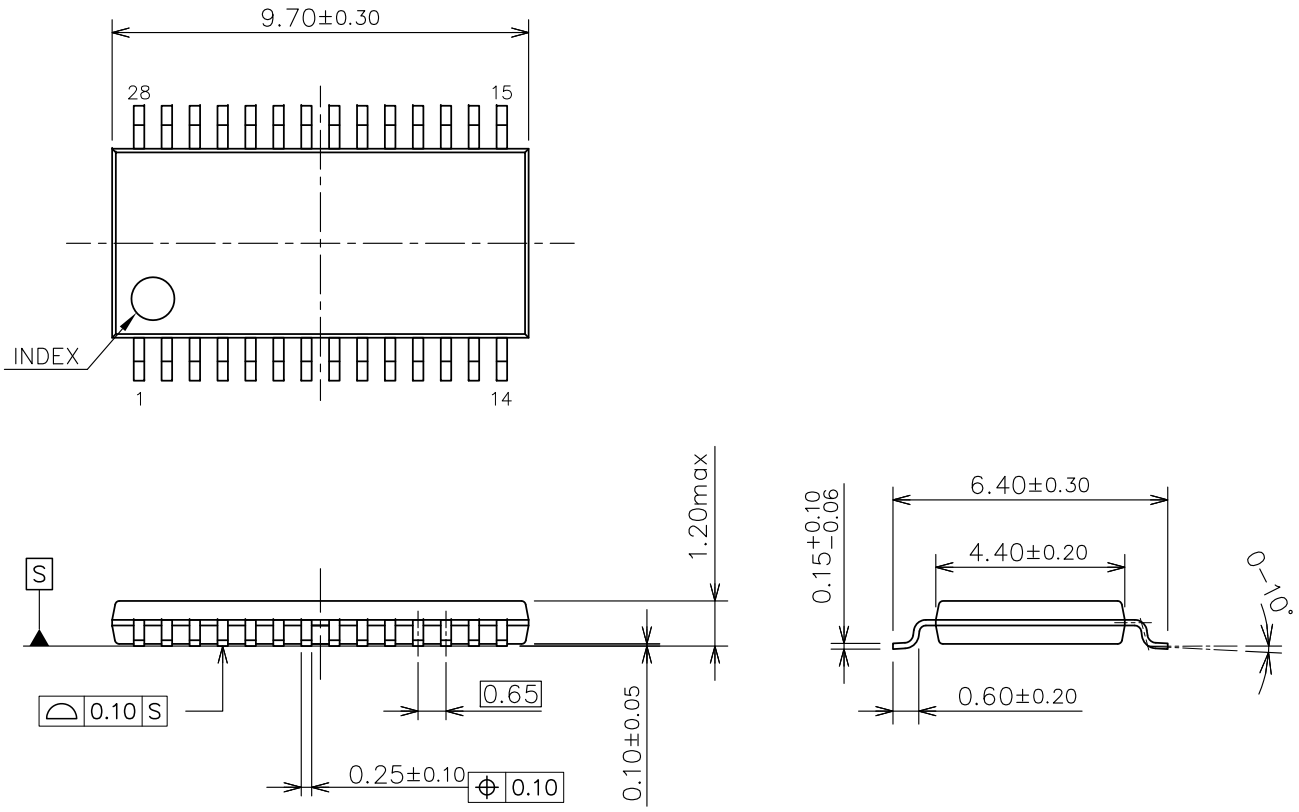
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH

Ver. A



TSSOP-28 Package Dimensions (Unit: mm)

RICOH

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