TW6872

Triple-Rate (SD/HD/3G) SDI Transmitter with VC-2 Encoder and Audio Decoder

FN8616
Rev 0.00
May 23, 2014

The TW6872 is a triple-rate (SD/HD/3G) SDI transmitter. It receives parallel BT.656/BT.1120/ASI video data from a CMOS sensor/ISP chip. It also receives analog audio, or serial digital audio. The TW6872 serializes the video and audio into an SDI stream and transmits it to an SDI receiver via its integrated cable driver.

In addition to the standard SDI format with uncompressed raw video data, TW6872 can optionally compress video with a visually lossless VC-2 compression algorithm to send the video formats normally running at HD rate (1.5Gbps) on the cable at SD rate (270Mbps), and therefore achieve longer cable reach.

Together, the TW6872 and Intersil's TW6874 SDI receiver provide a complete end-to-end SDI link solution and can operate with or without VC-2 compression. Integrated audio/video test patterns and PRBS checker ease system design and implementation.

The TW6872 is available in a 76 Ld QFN. It is specified for operation over the -40°C to +85°C ambient temperature range and operates on two power supplies: 1V and 3.3V. A single 27MHz crystal is used for all supported audio/video operating modes.

Applications

- SD/HD/3G-SDI Camera

Features

- Triple-rate (SD/HD/3G) SDI transmitter for Standard Definition (SD) and High Definition (HD), and 3G 10-bit component video
- Encoding SDI standard of ITU-R BT.656/SMPTE 259M Level C, ITU-R BT.1120/SMPTE ST 292, SMPTE 424M 10-bit parallel component video inputs into 10-bit serial video output
- BT.656/BT.1120 interface for CMOS sensor/ISP chip
- Asynchronous Serial Interface (ASI) for IEC 13818-1 compliant transport streams
- Integrated 75Ω cable driver with pre/de-emphasis
- Integrated VC-2 encoder allows transmission of HD video over SD transmission lengths
- Analog audio and I2S serial audio input interfaces over ancillary field
- Digital audio with PCM encoding for embedding audio samples into the audio ancillary field of SDI stream
- Single 27MHz clock/crystal input
- Optional clock output for use as the ISP chip's clock input to enhance overall jitter
- PRBS7/23 and video/audio pattern generator
- I^2C for external micro-controller interface
- Low power consumption
- Small footprint LTZ-QFN76L (9mm x9mm) package
- Pb-free (RoHS compliant)

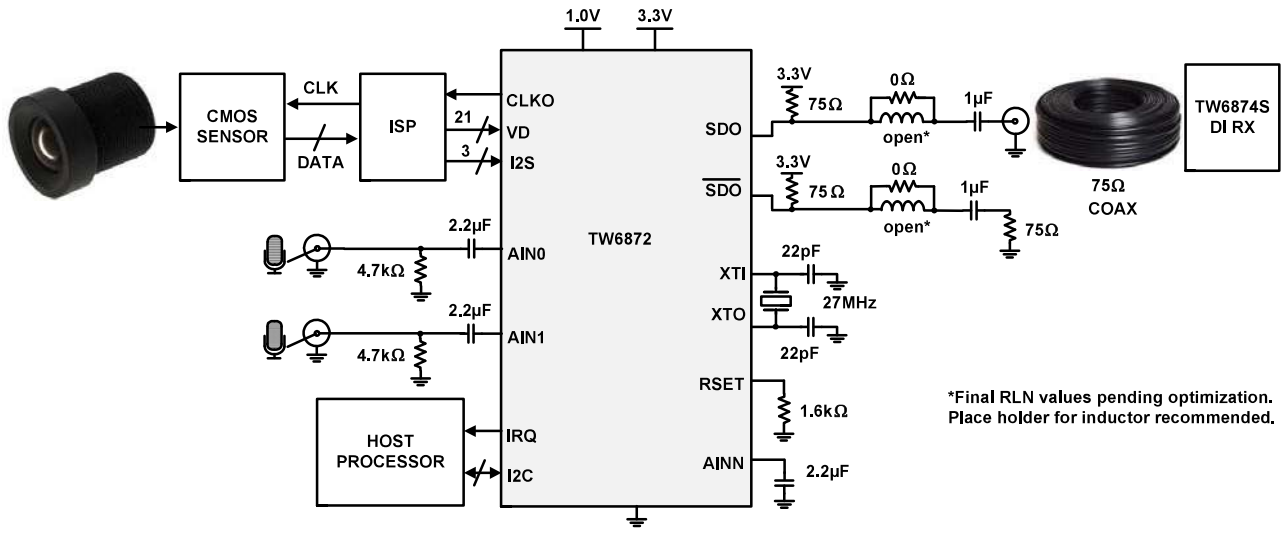

FIGURE 1. TW6872 TYPICAL APPLICATION

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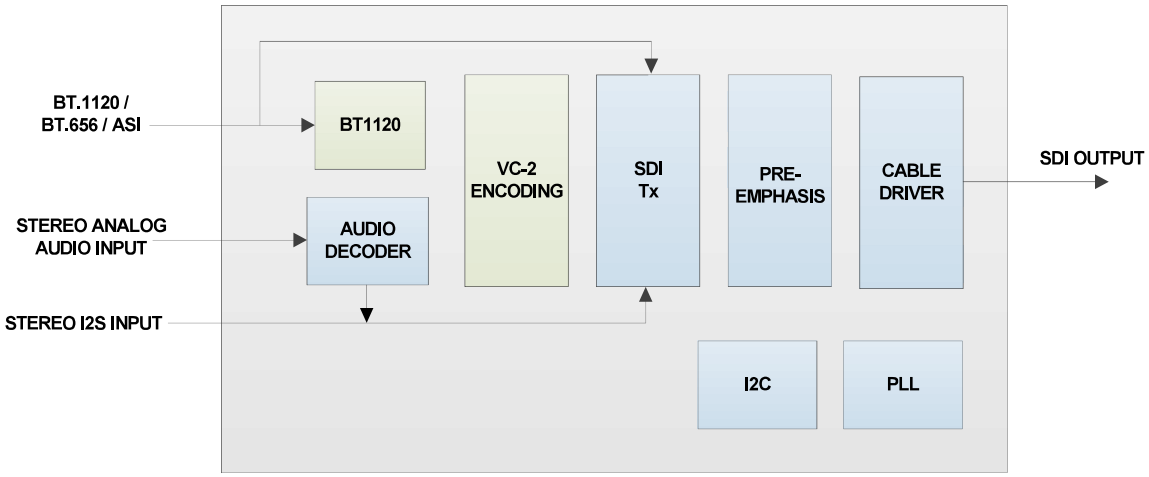
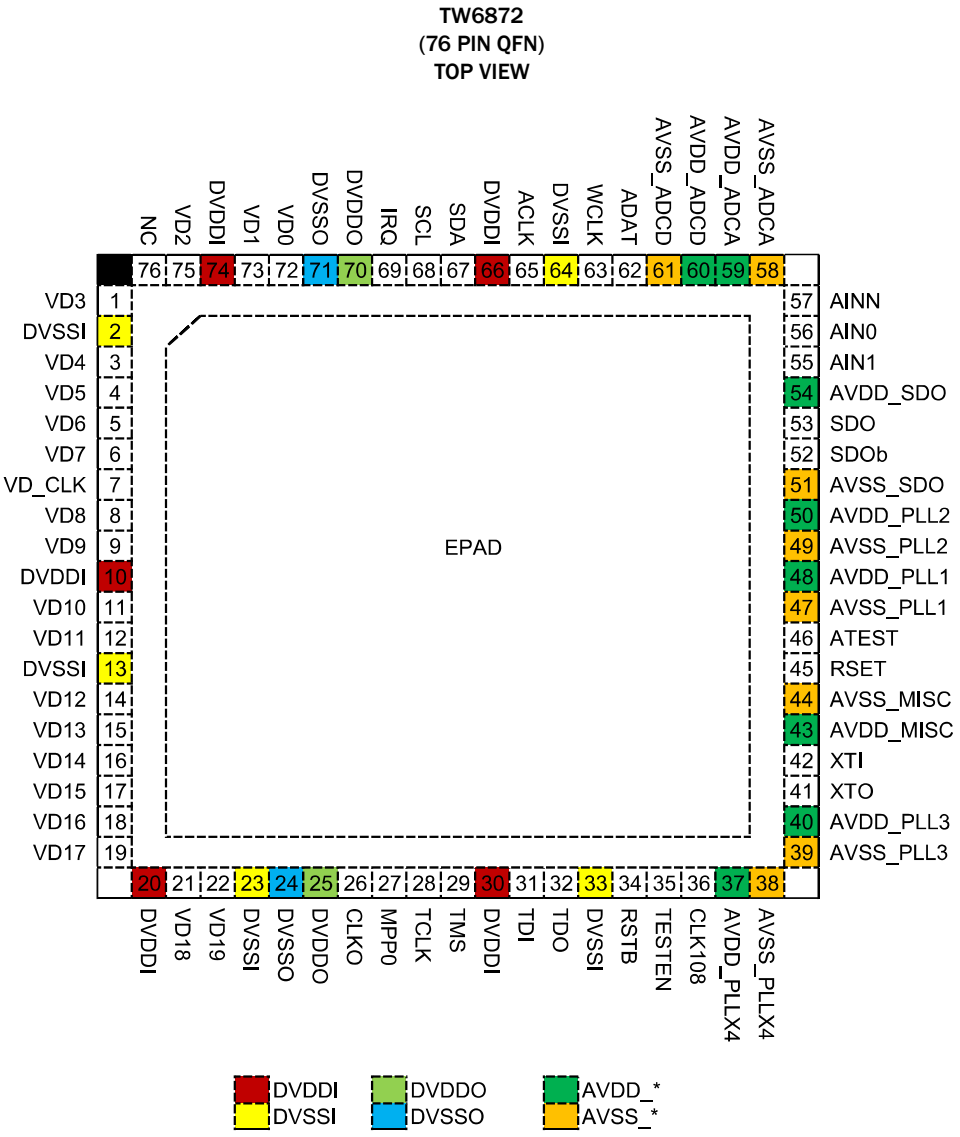
Block Diagram



Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
PARALLEL DIGITAL VIDEO			
22	VD19	Digital Input	Parallel video data input. HD/3G mode: Chroma (C) data SD mode: not used ASI mode: not used
21	VD18	Digital Input	
19	VD17	Digital Input	
18	VD16	Digital Input	
17	VD15	Digital Input	
16	VD14	Digital Input	
15	VD13	Digital Input	
14	VD12	Digital Input	
12	VD11	Digital Input	
11	VD10	Digital Input	
9	VD9	Digital Input	Parallel video data input. HD/3G mode: Luma (Y) data SD mode: multiplexed BT.656 chroma/luma data ASI mode: transport stream data input
8	VD8	Digital Input	
6	VD7	Digital Input	
5	VD6	Digital Input	
4	VD5	Digital Input	
3	VD4	Digital Input	
1	VD3	Digital Input	
75	VD2	Digital Input	
73	VD1	Digital Input	
72	VD0	Digital Input	
7	VD_CLK	Digital Input	Parallel video clock input. 3G mode: 148.5MHz HD mode: 74.25MHz SD mode: 27MHz ASI mode: 27MHz
26	CLKO	Digital Output	Clock source for the ISP in master mode. Generated frequencies are: 27MHz 3G mode: 148.5MHz HD mode: 74.25MHz or 148.5MHz SD mode: 13.5MHz or 27MHz
36	CLK108	Digital I/O	Alternate 108MHz clock source for the ISP in master mode
I2S AUDIO			
62	ADAT	Digital Input	Audio serial data input.
63	WCLK	Digital Input	Audio word clock input.
65	ACLK	Digital Input	Audio serial bit clock.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
I^2C			
67	SDA	Digital I/O	I^2C serial data IO. Requires pull-up resistor to VDDO.
68	SCL	Digital Input	I^2C serial clock input. Requires pull-up resistor to VDDO.
JTAG			
32	TDO	Digital Output	JTAG test data output.
31	TDI	Digital Input	JTAG test data input.
29	TMS	Digital Input	JTAG test mode start.
28	TCLK	Digital Input	JTAG test clock input.
SYSTEM			
69	IRQ	Digital I/O	Interrupt request.
34	RSTB	Digital Input	Resets chip when pulled LO. Reset must be asserted for 1µs every time the power supplies have powered up and settled to their final value.
35	TESTEN	Digital Input	For internal use only. Tie LO.
27	MPP0	Digital I/O	Multi-purpose pin.
46	ATEST	Analog Output	Analog test output. For internal use only. Do not connect anything to this pin.
76	NC	No Connect	Do not connect anything to this pin.
SERIAL DATA OUTPUT			
53	SDO	Analog Output	SDI serial data output. See "SDO Routing" on page 15 for termination guidelines.
52	SDOb	Analog Output	Inverted SDI serial data output. See "SDO Routing" on page 15 for termination guidelines.
45	RSET	Analog Output	Tie a 1.6kΩ (1%) resistor from this pin to analog ground. The resistor should be placed as close as possible to the RSET pin. SDI output amplitude can be adjusted by changing the value of the resistor.
CLOCK INPUT			
42	XTI	Analog Input	27MHz crystal connection or 27MHz oscillator input.
41	XTO	Analog Output	27MHz crystal connection.
ANALOG AUDIO			
55	AIN1	Analog Input	Audio input for channel 1. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF.
56	AIN0	Analog Input	Audio input for channel 0. Terminate with 4.7kΩ to ground and AC-couple with 2.2µF.
57	AINN	Analog Input	Audio ADC reference. Terminate with 2.2µF to ground. Do not connect external audio signal to this pin.
DIGITAL POWER			
10, 20, 30, 66, 74	DVDDI	Digital Power	1.0V digital power supply for core. Place a local 0.1µF ceramic bypass capacitor to the digital ground as close to the pin as possible.
2, 13, 23, 33, 64	DVSSI	Digital Ground	Digital ground.
25, 70	DVDDO	Digital Power	3.3V digital power supply for I/O. Place a local 0.1µF ceramic bypass capacitor to the digital ground as close to the pin as possible.
24, 71	DVSSO	Digital Ground	Digital ground.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
ANALOG POWER			
54	AVDD_SDO	Analog Power	3.3V analog power supply for SDO driver. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
51	AVSS_SDO	Analog Ground	Analog ground.
43	AVDD_MISC	Analog Power	3.3V analog power supply for SDO driver. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
44	AVSS_MISC	Analog Ground	Analog ground.
60	AVDD_ADCD	Analog Power	3.3V analog power supply for ADC. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
61	AVSS_ADCD	Analog Ground	Analog ground.
59	AVDD_ADCA	Analog Power	3.3V analog power supply for ADC. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
58	AVSS_ADCA	Analog Ground	Analog ground.
48	AVDD_PLL1	Analog Power	3.3V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
47	AVSS_PLL1	Analog Ground	Analog ground.
50	AVDD_PLL2	Analog Power	3.3V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
49	AVSS_PLL2	Analog Ground	Analog ground.
40	AVDD_PLL3	Analog Power	3.3V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
39	AVSS_PLL3	Analog Ground	Analog ground.
37	AVDD_PLLX4	Analog Power	3.3V analog power supply for PLL. Place a local 0.1µF ceramic bypass capacitor to the analog ground as close to the pin as possible.
38	AVSS_PLLX4	Analog Ground	Analog ground.
EPAD	EPAD	Ground	Ground.

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
TW6872-NA1-CR	TW6872 NA1-CR	-40 to +85	76 Lead QFN	L76.9x9

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for TW6872. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

Supply Pins
- AVDD_SDO to AVSS_SDO . . . . . +4.0V
- AVDD_MISC to AVSS_MISC . . . . . +4.0V
- AVDD_ADCA to AVSS_ADCA . . . . . +4.0V
- AVDD_ADCD to AVSS_ADCD . . . . . +4.0V
- AVDD_PLL1 to AVSS_PLL1 . . . . . +4.0V
- AVDD_PLL2 to AVSS_PLL2 . . . . . +4.0V
- AVDD_PLL3 to AVSS_PLL3 . . . . . +4.0V
- AVDD_PLLX4 to AVSS_PLLX4 . . . . . +4.0V
- DVDDI to DVSSI . . . . . +1.2V
- DVDDO to DVSSO . . . . . +4.0V

Other Pins
- Voltage on any Input Pin . . . . . DVSSO-0.3 V to DVDDO V
- SDO/SDOb Voltage . . . . . AVSS_SDO V to AVDD_SDO V
- XTI/XTO Voltage . . . . . 0 V to 1 V
- AIN0/1/N Voltage . . . . . AVSS_ADCA V to AVDD_ADCA V

ESD Ratings
- IEC 61000-4-2 (contact discharge) Analog Audio Pins 6kV
- Human Body Model (JEDEC JS-001-2011) all Pins 2kV
- Charged Device Model (JESD22-C101) 750V

Latch Up (Tested per JESD78; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 3, 4)	22	1.5

Power Dissipation . . . . . See "Electrical Specifications"

Maximum Die Temperature . . . . . +125°C

Storage Temperature . . . . . -65°C to +150°C

Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Operating Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

DVDDI = 1.0V, AVDD_SDO = AVDD_MISC = AVDD_ADCD = AVDD_ADCA = AVDD_PLL1 = AVDD_PLL2 = AVDD_PLL3 = AVDD_PLLX4 = DVDDO = 3.3V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
POWER SUPPLY VOLTAGE						
AVDD_SDO	Analog SDO Driver Supply Voltage		3.0	3.3	3.6	V
AVDD_MISC	Analog Misc Supply Voltage		3.0	3.3	3.6	V
AVDD_ADCA	Analog ADC Supply Voltage		3.0	3.3	3.6	V
AVDD_ADCD	Analog ADC Supply Voltage		3.0	3.3	3.6	V
AVDD_PLL1	Analog PLL Supply Voltage		3.0	3.3	3.6	V
AVDD_PLL2	Analog PLL Supply Voltage		3.0	3.3	3.6	V
AVDD_PLL3	Analog PLL Supply Voltage		3.0	3.3	3.6	V
AVDD_PLLX4	Analog PLL Supply Voltage		3.0	3.3	3.6	V
DVDDI	Digital Core Supply Voltage		0.9	1.0	1.1	V
DVDDO	Digital IO Supply Voltage		3.0	3.3	3.6	V
POWER DISSIPATION						
I_AVDD	Analog Supply Current (Note 10) (all AVDD_* tied together except SDO)			60		mA
I_AVDD_SDO	Analog SDO Supply Current			60		mA
I_DVDDI	Digital Core Supply Current			90		mA
I_DVDDO	Digital IO Supply Current			6		mA
P_{TOT}	Total Power			505.8		mW

Electrical Specifications

DVDDI = 1.0V, AVDD_SDO = AVDD_MISC = AVDD_ADCD = AVDD_ADCA = AVDD_PLL1 = AVDD_PLL2 = AVDD_PLL3 = AVDD_PLLX4 = DVDDO = 3.3V, T_A = +25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
PARALLEL VIDEO INPUT						
f_{VDCLK}	Pixel Clock Frequency		27		148.5	MHz
$DCYC_{VDCLK}$	Pixel Clock Duty Cycle			50		%
t_{SU}	Data Set-up Time		3.8			ns
t_{HD}	Data Hold Time		0.6			ns
SERIAL DIGITAL OUTPUT						
DR_{SDO}	Serial Data Rate		0.27		2.97	Gbps
OS_{SDO}	Serial Data Output Swing		720	800	880	mV
OV_{SDO}	Serial Data Output Overshoot		-10		+10	%
TT_{SDO}	Transition (Rise/Fall) Time (20% to 80%)	270Mbps	400	850	1500	ps
		1.485Gbps		135	270	ps
TTD_{SDO}	Difference between Rise/Fall Time	270Mbps		40		ps
		1.485Gbps		10		ps
RL_{SDO}	Return Loss (Note 9)	<1.5GHz	-13			dB
		1.5GHz to 3GHz	-10			dB
JIT_{SDO}	Output Jitter	270Mbps: timing jitter above 10Hz		0.11		UI_{P-P}
		270Mbps: alignment jitter above 1kHz		0.09		UI_{P-P}
		1.485Gbps: timing jitter above 10Hz		0.37		UI_{P-P}
		1.485Gbps: alignment jitter above 100kHz		0.09		UI_{P-P}
CLKO OUTPUT						
f_{CLKO}	Nominal Frequency		13.5		148.5	MHz
$DCYC_{CLKO}$	Duty Cycle		45		55	%
DIGITAL INPUTS						
VIH	Input High Voltage		2.0		3.6 (DVDDO + 10%)	V
VIL	Input Low Voltage		-0.3		0.8	V
I_L	Input Leakage Current		-10	0	+10	µA
C_{IN}	Input Capacitance	f = 1MHz, V_{IN} = 2.4V		2		pF
DIGITAL OUTPUTS						
VOH	Output High Voltage	IO = -2mA	2.4		DVDDO	V
VOL	Output Low Voltage	IO = +2mA		0.2	0.4	V
I_{OZ}	Tri-State Current				10	µA
CRYSTAL (CONNECTED to XTI and XTO)						
f_{XTAL}	Nominal Frequency (Fundamental)			27		MHz
DEV_{XTAL}	Deviation (Note 6)				±50	ppm
CL	Load Capacitance			18		pF
RS	Series Resistor (ESR)			50		Ω
OSCILLATOR INPUT (CONNECTED TO XTI)						
f_{OSC}	Nominal Frequency (Fundamental)			27		MHz
TJ_{OSC}	Total jitter				1.8	ps-pp
$DCYC_{OSC}$	Duty Cycle				55	%

Electrical Specifications

DVDDI = 1.0V, AVDD_SDO = AVDD_MISC = AVDD_ADCD = AVDD_ADCA = AVDD_PLL1 = AVDD_PLL2 = AVDD_PLL3 = AVDD_PLLX4 = DVDDO = 3.3V, T_A = +25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
ANALOG AUDIO INPUT						
AUD_{RANGE}	Input Voltage Range		0	1.4	2.4	V_{P-P}
AUD_{FS}	Full Scale Input Voltage Range (Note 7)		0.21	1.4	2.4	V_{P-P}
AUD_{ISO}	Interchannel Isolation (Note 8)			90		dB
DIGITAL AUDIO INPUT						
T_{A_ct}	ACLK Cycle Time			70.76		ns
T_{A_dc}	ACLK Duty Cycle			50		%
T_{A_su}	WCLK, ADAT Setup Time		30			ns
T_{A_h}	WCLK, ADAT Hold Time		5			ns
I^2C SERIAL CONFIGURATION INTERFACE						
f_{SCL}	Maximum SCL Clock Frequency				400	kHz
$t_{SU:STA}$	Set-up Time for a START Condition		370			ns
$t_{HD:STA}$	Hold Time for a START Condition		74			ns
$t_{SU:STO}$	Set-up Time for a STOP Condition		370			ns
t_{BUF}	Bus Free Time between a STOP and START Condition		740			ns
$t_{SU:DAT}$	Data Set-up Time		74			ns
$t_{HD:DAT}$	Data Hold Time		50		900	ns
t_r	Rise Time of SDA and SCL				300	ns
t_f	Fall Time of SDA and SCL				300	ns
CBUS	Capacitive Load for each Bus Line				400	pF

NOTES:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
6. Crystal deviation is based on normal operating condition.
7. Refer to Table 79 on page 37 for gain settings. F_{IN} = 1kHz.
8. Tested at input gain of 0dB. F_S = 8kHz and 16kHz.
9. Return Loss depends on PCB design.
10. Add 15mA to I_ADD for Dirac_Compression.

Video Input Modes

The TW6872 has a 20-bit wide parallel video input interface. Through this interface, the input can be configured in one of two modes by registers: either the BT.656/BT.1120 mode, or the Asynchronous Serial Interface (ASI) mode. In the BT.656/BT.1120 mode, the video data can be either YC multiplexed (10-bit mode) or YC separated (20-bit mode). In the ASI input mode, the ASI stream data comes in through the 10-bit data bus running at 27MHz.

Video Bit Mapping

The ISP to TW6872 port mapping depends on the mode used as described in the following. Figure 2 shows the timing relationship for the input clock and data.

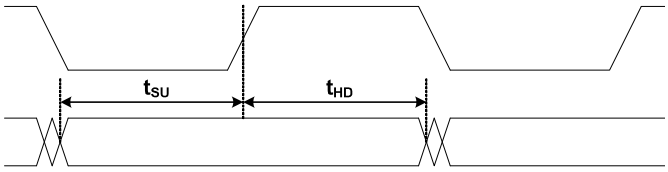


FIGURE 2. VD_CLK TO VD[19:0] TIMING

BT.656 MODE

In BT.656 mode, only 10-bit data is used by the SD video (NTSC/PAL). For either ASI or BT.656 formats, the 10-bit BT.656 video data use the lower word (bits 9:0) of the TW6872's 20-bit port and the upper word is not used per Figure 3.

The timing reference signals (TRS, consisting of SAV and EAV codes) are inserted in the data stream to indicate the active video time, as shown in Figure 4. The input timing is also illustrated in Figure 4. The SAV and EAV sequences are shown in Table 1.

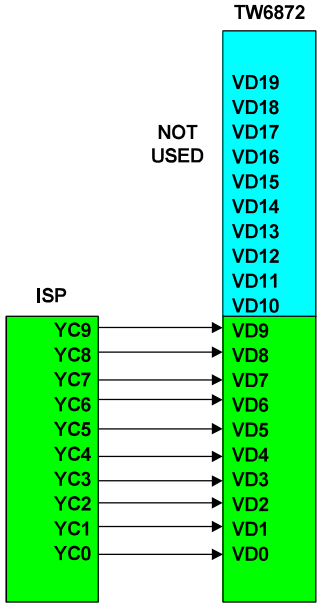


FIGURE 3. BT.656 MAPPING

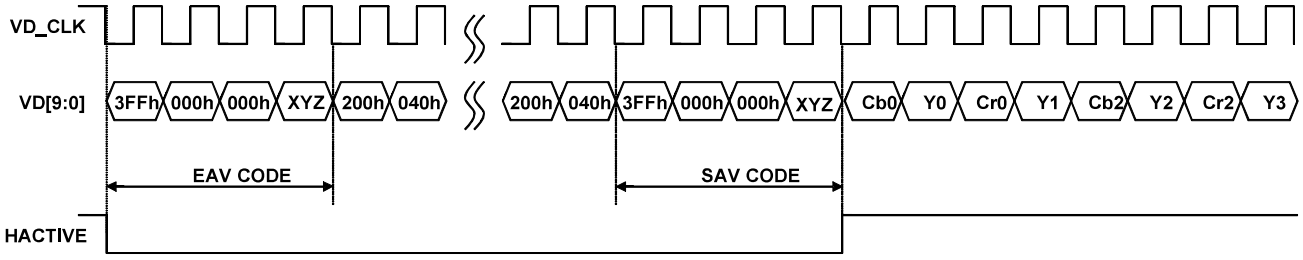


FIGURE 4. BT.656 FORMAT

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TABLE 1. SAV/EAV CODE SEQUENCE FOR BT.656 AND BT.1120 DATA

CONDITION			FVH VALUE			SAV/EAV CODE SEQUENCE			
FIELD	V_{TIME}	H_{TIME}	F	V	H	FIRST BYTE	SECOND BYTE	THIRD BYTE	FOURTH BYTE
EVEN	Blank	EAV	1	1	1	0x3FF	0x000	0x000	0x3C4
EVEN	Blank	SAV	1	1	0	0x3FF	0x000	0x000	0x3B0
EVEN	Active	EAV	1	0	1	0x3FF	0x000	0x000	0x368
EVEN	Active	SAV	1	0	0	0x3FF	0x000	0x000	0x31C
ODD	Blank	EAV	0	1	1	0x3FF	0x000	0x000	0x2D8
ODD	Blank	SAV	0	1	0	0x3FF	0x000	0x000	0x2AC
ODD	Active	EAV	0	0	1	0x3FF	0x000	0x000	0x274
ODD	Active	SAV	0	0	0	0x3FF	0x000	0x000	0x200

BT.1120 MODE

For HD/3G formats, the input data is 20-bit BT.1120 and all 20 bits of the TW6872's video input port are used. The Y and C pixels are placed separately. Y is input on the lower word (bits 9:0) and C is input on the upper word (bits 19:10) per Figure 5. If

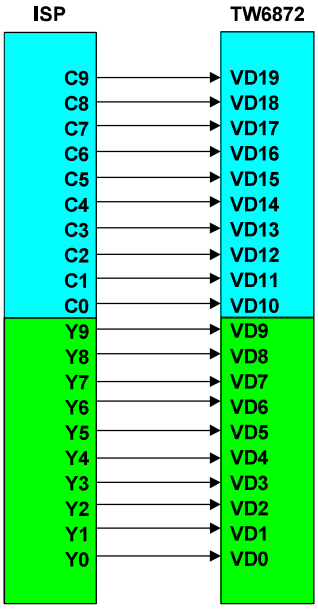


FIGURE 5. 20-BIT BT.1120 MAPPING

the parallel video source only outputs 16 bits, the configuration used in Figure 6 should be used.

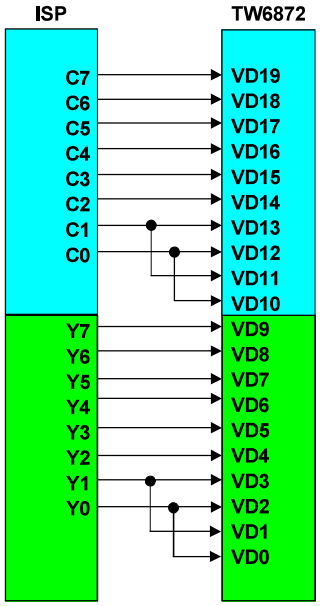


FIGURE 6. 16-BIT BT.1120 MAPPING

The SAV/EAV signals shown in Table 1 are inserted into both the Y and C bus, and are identical on both buses. The timing reference signals and input timing for BT.1120 mode are shown in Figure 7.

The video pixel data of BT.656 and BT.1120 internally run through a parallel-to-serial conversion and then a scrambler circuit before driving the SDI output pin.

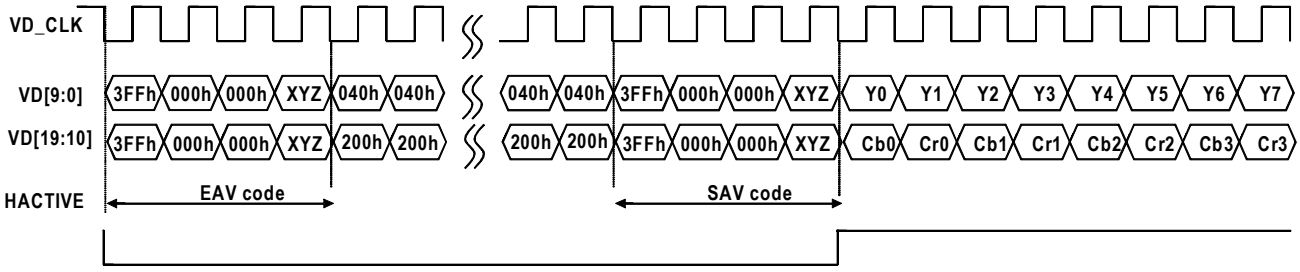


FIGURE 7. BT.1120 FORMAT

Master/Slave Mode

The TW6872 operates in either master or slave mode. In master mode the TW6872 generates a reference clock for the ISP (CLKO output). In slave mode it uses the ISP's video data clock (VD_CLK input) for its timing reference (CLKO is not used).

MASTER MODE

In master mode, the TW6872 generates a low jitter CLKO to drive the ISP master clock. In turn, the ISP device generates the VD_CLK to drive the BT.656/BT.1120 input. With the common clock basis, master mode provides the best performance with the lowest jitter. The TW6872 can generate the following CLKO frequencies:

- Serial data clock rate/10
  - 27MHz
  - 148.5MHz
  - 148.5/1.001MHz
- Serial data clock rate/20
  - 13.5MHz
  - 74.25MHz
  - 74.25/1.001MHz
  - 148.5MHz
  - 148.5/1.001MHz
- VC-2 compressed
  - 27MHz
  - 27/1.001MHz
  - 74.25MHz
  - 74.25/1.001MHz
- XTI clock rate
  - 27MHz

The previous CLKO frequencies are generated per the selected operating mode by setting ISPCLK_DIV10_SEL for a chosen data rate (SD/HD/3G). ISP_XTALCLK_SEL bypasses this divider and sends the XTI frequency onto CLKO. If the preceding clock frequencies are not suitable for the ISP, CLK108 can be used to generate a 108MHz clock. This clock maintains the same time base as CLKO and thus allows for master mode operation. This clock can be divided externally to generate other desired frequencies such as 54MHz.

SLAVE MODE

If ISP cannot accept an external master clock from CLKO, then the TW6872 must operate in slave mode. In slave mode, the ISP generates VD_CLK independently. If VD_CLK input may have higher jitter, TW6872 performance will be affected. CLKO is not used and can be powered down. When in slave mode, VD_CLK input must be present to use TW6872's internal pattern generator.

Asynchronous Serial Interface Mode

The Asynchronous Serial Interface takes the standard IEC 13818-1 compliant transport stream running at 27MHz into the 10-bit data bus. The incoming pre-compressed stream is converted from 10-bit parallel format into serial 270Mbps data, then driven out the SDI output pin.

SDI Video Output

The TW6872 serial data output (SDO) electrical specifications and data format are compliant to SMPTE 259M for SD-SDI, SMPTE ST-292 for HD-SDI, and SMPTE 424M for 3G-SDI standards, supporting both video and audio embedded in the serial stream. TW6872 also supports embedding of ancillary data packets that can be used for downstream information purposes. In addition, the TW6872 output driver integrates a programmable pre/de-emphasis feature. This feature is the intentional alteration of the amplitude vs frequency characteristics of the signal to reduce adverse effects of noise. For the maximum cable reach, the PCB layout must be optimized to ensure best signal integrity per the layout guidelines in "Layout Guidelines" on page 15.

SDI Video Standard Formats

The supported SDI video formats are:

- 270Mbps (SMPTE 259M Level C)
  - 525i/625i 50, 59.94 fields/s
- 1.485Gbps (SMPTE ST 292)
  - 720p 50, 60 frames/s
  - 1080p 24, 25, 30 frames/s
  - 1080i 50, 60 fields/s
- 1.485/1.001Gbps (SMPTE ST 292)
  - 720p 59.94 frames/s
  - 1080p 23.976, 29.97 frames/s
  - 1080i 59.94 fields/s
- 2.97Gbps (SMPTE 424M)
  - 1080p 50, 60 frames/s
- 2.97/1.001Gbps (SMPTE 424M)
  - 1080p 59.97 frames/s

Any of the above supported video formats can be output on SDO. The video streams are transmitted in 10-bit YCbCr 4:2:2 sampled format.

Cable Reach

The TW6872 SDI output driver is designed to work with various types of 75Ω coaxial cable including: RG6, RG59, and 3C-2V (SYV 75-3). Within each cable type, there are variations such as bare copper or copper-clad over steel or aluminum core. Actual cable reach is determined by a combination of the cable type, the SDI receiver and system implementation. In general, the TW6872 meets or exceeds cable reach as defined by the HDcctv Alliance version 1.0 SR specification.

Pre/De-Emphasis

To provide additional cable reach, the TW6872 output driver integrates a programmable pre/de-emphasis feature. Coaxial cable acts as a low-pass filter to the video signal, attenuating the high frequency components of the signal significantly more. The pre/de-emphasis feature boosts the high frequency component of the transmitted signal. Essentially, this means that transition bits have a larger amplitude than the following bits. Figure 8 depicts this graphically. The PREEMPH register controls the value.

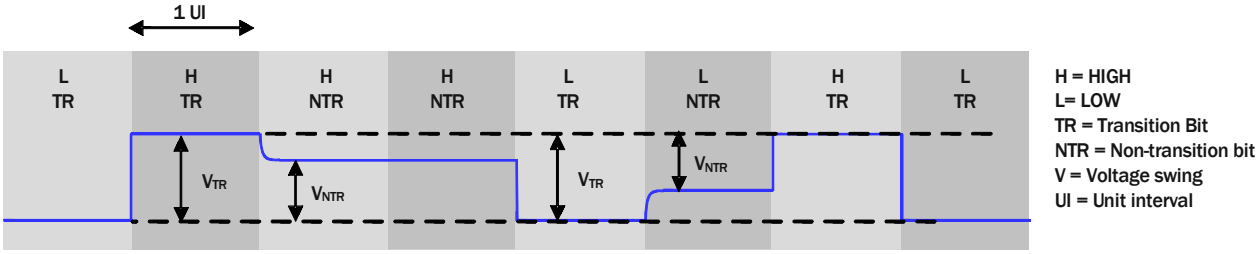


FIGURE 8. PRE/DE-EMPHASIS WAVEFORM. NO PRE/DE-EMPHASIS MEANS $V_{TR} = V_{NTR} = 800mV$

PRE-EMPHASIS

By using the driver in pre-emphasis mode, all bits except the transition bit have the nominal 800mV amplitude (V_{NTR}). The transition bit can be programmed to have up to ~1300mV amplitude (V_{TR}). Pre-emphasis is defined as:

$$\text{pre-emphasis} = 20 \bullet \log_{10}(V_{TR}/V_{NTR}) \quad \text{(EQ. 1)}$$

The allowed pre-emphasis range is 0 to 11.5dB. Due to voltage swing headroom limitations, pre-emphasis settings above 5dB hold V_{TR} to ~1300mV while reducing the V_{NTR} amplitude.

DE-EMPHASIS

By using the driver in de-emphasis mode, the transition bit has the nominal amplitude 800mV amplitude (V_{TR}). The non-transition bits can be programmed from ~350mV to 800mV (V_{NTR}). $V_{TR} = V_{NTR}$ means no pre/de-emphasis is applied. De-emphasis is defined as:

$$\text{de-emphasis} = 20 \bullet \log_{10}(V_{NTR}/V_{TR}) \quad \text{(EQ. 2)}$$

The allowed de-emphasis range is -7 to 0dB.

VC-2 Compressed Data

The TW6872 can optionally compress a I-frame subset of 1.485Gbps HD video data into 270Mbps SD video bit stream data using VC-2 Video Compression (also known as Dirac). Using this, Compressed HD video transmitted at 270Mbps achieves the same cable lengths as SD-SDI. The compressed video quality is visually lossless, and is completely satisfactory in applications such as video surveillance.

The TW6872 VC-2 option is compliant to SMPTE ST-2047-4 Level 65 format. The VC-2 Video Compression is specified in SMPTE ST 2042-1, with the level specified in SMPTE ST 2042-2. The carriage of Level 65 VC-2 compressed video data over SD-SDI is specified in SMPTE ST 2047-4.

The following compressed video formats are supported:

- VC-2 compressed 720p 50, 59.94 frames/s
- VC-2 compressed 1080p 25, 29.97 frames/s

Note: The incoming pixel clock for VC-2 PAL should be 74.25 MHz, while VC-2 NTSC input uses 74.25/1.001MHz.

Note: The incoming pixel clock for the uncompressed 25 and 50 frames/s should be 74.25MHz, while the clock for uncompressed 29.97 and 59.94 frames/s should be 74.25/1.001MHz. At the physical layer, the serial signal is SD-SDI compliant as specified in SMPTE 259M. Since the timing references signal (TRS) are those used in SD-SDI, the frame/field rate carried can only be 25/50 in PAL systems and 29.97/59.94 in NTSC systems. The ancillary audio and ancillary packet data remain embedded in the stream as they would for an SD-SDI stream. Because of this, in order to use the VC-2 compression feature, the incoming video needs to run at 25/50 frame rates for PAL systems and 29.97/59.94 frame rates for NTSC systems. 30/60 frame rates cannot be used for NTSC systems. For those ISPs supporting only 30/60 frame rates using a 27MHz crystal, the TW6872 is able to generate a CLKO frequency of 27/1.001MHz so that the ISP PLL does not need to do 1.001 division and generate 29.97/59.94 frame rate video.

Audio Input Interface

The audio subsystem in the TW6872 is composed of two Analog-to-Digital Converters (ADC) processing, an audio detector and digital serial audio interface. The TW6872 can receive two analog audio signals (for stereo left/right channels) or one stereo I2S digital serial audio stream. These audio streams are inserted into and transported by the SDI data stream.

Analog Audio

The TW6872 has an audio detector for each analog audio channel. There are two kinds of audio detection defined by AAMPMD. One is the detection of absolute amplitude and the second is of differential amplitude. For both detection methods, the accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH0/1 registers. Using the differential amplitude method is recommended. The status for audio detection is read by the AUD_STATE0/1 register for polling programming and it also makes an interrupt request through the IRQ pin for event driven programming.

The analog audio input signal gain for the AIN0/1 pins can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN0/1 registers before being sampled by the ADCs.

Analog audio is sampled at 48kHz by an internally generated sampling clock.

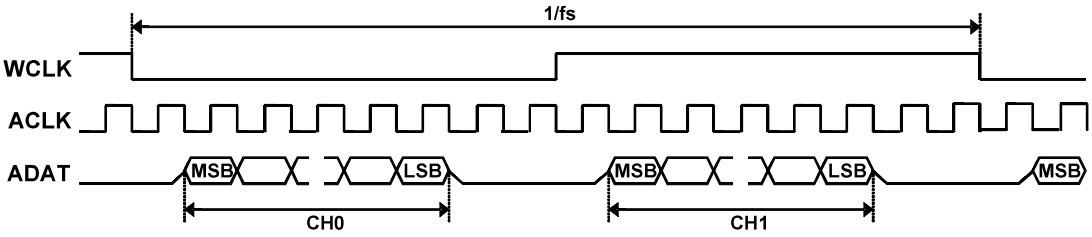


FIGURE 9. SERIAL AUDIO INTERFACE FORMAT

I2S Digital Audio

The digital serial audio interfaces follows a standard I2S interface as shown in Figure 9.

The ACLK, WCLK and ADAT pins from the I2S decoder block are used to receive digital serial audio input data. The I2S interface only operates in slave mode; these pins are always inputs.

SDI Ancillary Audio

Either the I2S or analog input audio is inserted into the SDI data stream in ancillary audio format. For 3G/HD-SDI, TW6872 ancillary audio follows the SMPTE ST 299-1 standard, using two 24-bit wide channels at 48kHz sampling frequency. For SD-SDI, TW6872 follows the SMPTE 272M standard, using two 20-bit wide channels at 48kHz sampling frequency.

Layout Guidelines

Specific printed circuit board (PCB) layout guidelines should be followed for optimal TW6872 performance. Special care should be given to the following subsections in order of layout priority:

- SDO routing
- Power supply routing
- Parallel video routing
- Power supply bypassing

These are each addressed in the following sections.

SDO Routing

The SDO/SDOb pins can toggle at up to 3Gbps with less than 135ps edge rates. Special care is required in designing the PCB interface for these pins, otherwise poor return loss and suboptimal cable reach will occur.

Typically, the SDO output will consist of: BNC connector, 1µF AC-coupling capacitor, return loss network (75Ω resistor in parallel with an inductor, or 0Ω resistor if the inductor is not installed), and 75Ω termination resistor to 3.3V (AVDDTERM). The SDOb output will be similar, except that it is terminated to 75Ω.

Since the termination networks are 75Ω, the PCB trace characteristic impedance must also be 75Ω single-ended. These traces should be on the top layer and not transition to any other layer, which would cause impedance discontinuities. The adjacent reference (ground) plane should be a solid, continuous copper plane.

A PCB stackup/spacing should be chosen such that the trace width to give 75Ω is approximately as wide as the component landing pads in order to minimize impedance discontinuities. In this regard, the physically smallest components should be used. 0201 size is recommended.

The 75Ω termination resistors (R1 and R3 in Figure 10) should be placed as close as possible to the TW6872's SDO/SDOb pins. The return loss network and AC-coupling cap should be adjacent to the termination resistor. SDO and SDOb should be isolated by a ground fill between the signal traces and termination components as shown in Figure 11.

A high quality BNC connector that is rated for 3Gbps operation should be chosen. Typically edge launch BNC connectors, such as the Samtec BNC7T-J-P-XX-ST-EM1, give better frequency response than right angle or vertical connectors. To optimize return loss, the total trace length from the BNC connector to SDO should be as short as possible.

It is advised to follow the reference layout to meet these criteria. Figures 10 and 11 show the reference schematic and layout meeting these requirements. The PCB stackup used in this design is:

- Layer 1: 75Ω signal
- Layer 2: Ground
- Layer 3: Power
- Layer 4: Power
- Layer 5: Ground
- Layer 6: Signal

A four layer stackup can be used to implement the design. However, if the signal return plane has other traces routed on it, it is important that the solid copper section under the high speed SDO traces not be cut and that it remains solid. Keep other traces away from this area.

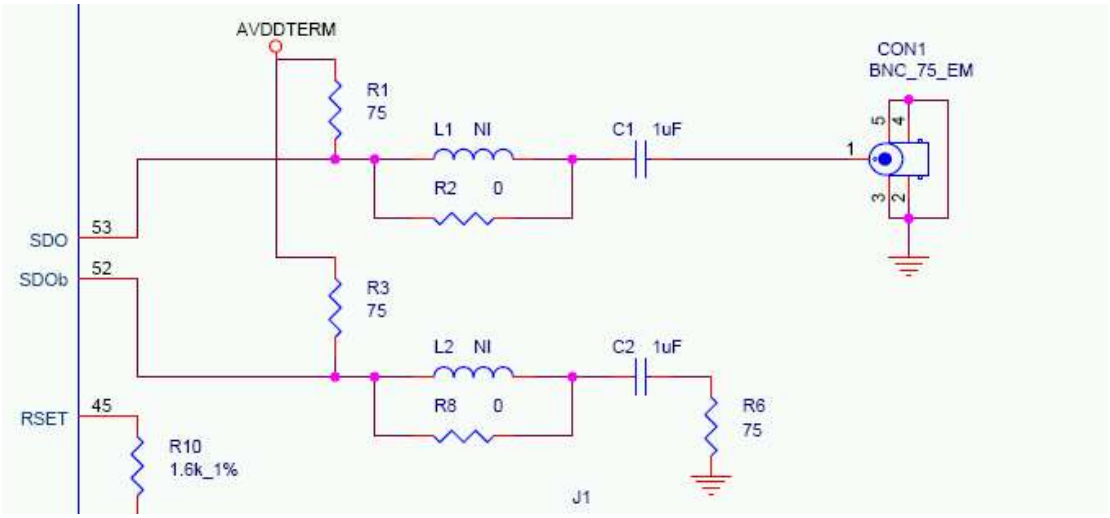


FIGURE 10. SDO/SDOb OUTPUT SCHEMATIC

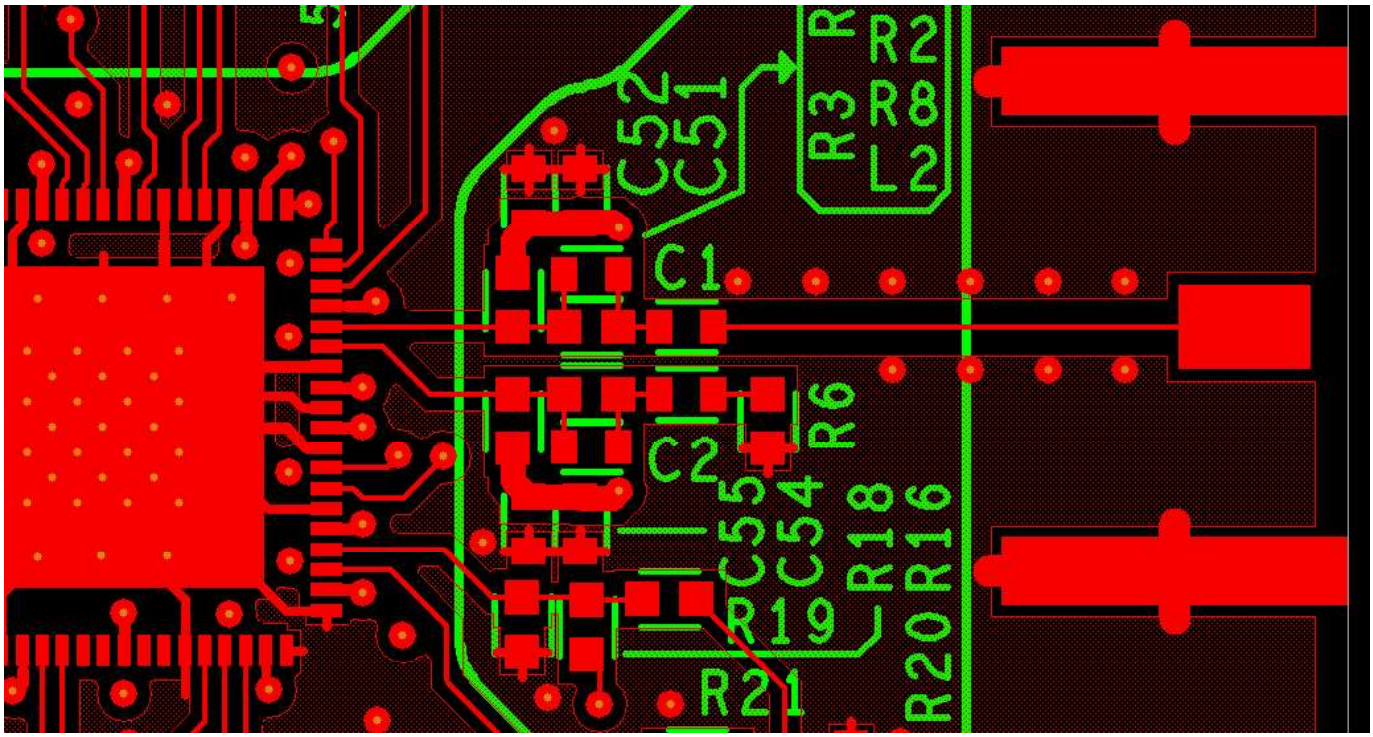


FIGURE 11. SDO/SDOb LAYOUT LAYER 1

Power Supply Routing

The TW6872 uses eight analog supply plans (one 3.3V pin for each domain) and two digital supply plans (two DVDDO 3.3V pins and five DVDDI 1.0V pins). The SDO output termination resistors also use a 3.3V supply (AVDDTERM). Switching regulators that generate a 3.3V and 1.0V rail can be used; an LDO for the analog 3.3V supply is not necessary.

For the 3.3V regulator, the AVDDTERM/AVDD_SDO pins should be grouped by one ferrite bead, the remaining seven AVDD pins should be isolated by another ferrite bead, and the two DVDDO pins should be isolated by a third ferrite bead. For DVDDI, a single ferrite bead can be used from the power regulator to the five pins. Figures 12 and 13 show the reference schematic for power supply routing.

Ideally a low impedance plane will route to each pin, but a wide trace can also be used. A single common ground can be used for the analog and digital grounds.

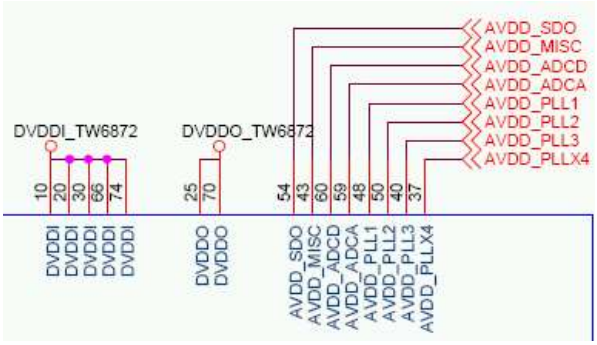
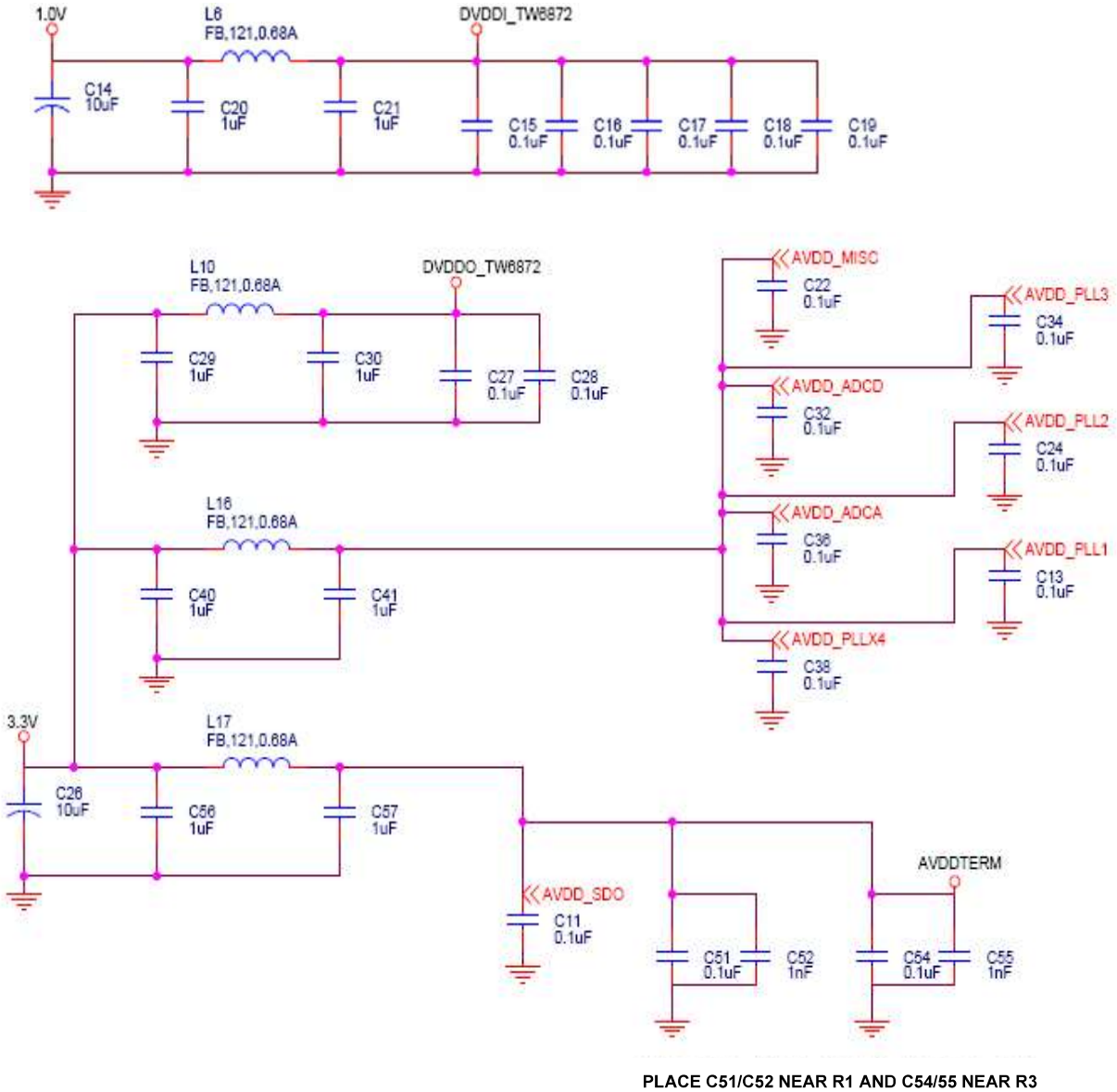


FIGURE 12. TW6872 POWER SUPPLY PINS



PLACE C51/C52 NEAR R1 AND C54/55 NEAR R3

FIGURE 13. POWER SUPPLY ROUTING AND BYPASSING SCHEMATIC

Parallel Video Routing

The parallel video input pins toggle up to a maximum frequency of 148.5MHz clock. The traces connected to these pins must be matched in length for all 20-bits plus clock.

The LVCMOS traces are typically routed as 50Ω single-ended, but it is not critical. The traces are also allowed to transition between layers for ease of routing. A 33Ω series termination should be placed near each of the ISP's LVCMOS driver pins. Series termination prevents overshoot and ringing, leading to improved EMI performance.

Power Supply Bypassing

It is important that the various supplies be well bypassed over a wide range of frequencies. A combination of different values of capacitors from 1000pF to 5µF or more with low ESR characteristics is generally required.

LOCAL BYPASS CAPACITORS

A physically small, low value capacitor should bypass each IC supply pin to ground. Capacitors of 0.1µF offer low impedance in the 10MHz to 20MHz region, and 1000pF capacitors in the 100MHz to 200MHz region. Minimize trace length and vias to minimize inductance and maximize noise rejection.

Figure 14 demonstrates a common but sub optimal PCB layout. The additional trace inductance between the bypass capacitor and the power supply/IC reduces its effectiveness. Figure 15 demonstrates a more optimal layout. In this case there is still series trace inductance (it is impossible to completely eliminate it), but now it is being put to good use, as part of a T-filter, attenuating supply noise before it gets to the IC, and reducing the amount of IC-generated noise that gets injected into the supply. Figures 16 and 17 show the same effect when the bypass capacitor must be placed on the opposite side of the PCB from the IC.

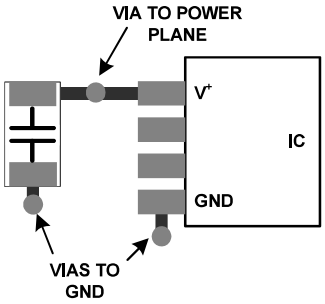


FIGURE 14. SUB-OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT - CAPACITOR AND IC ON SAME PCB LAYER

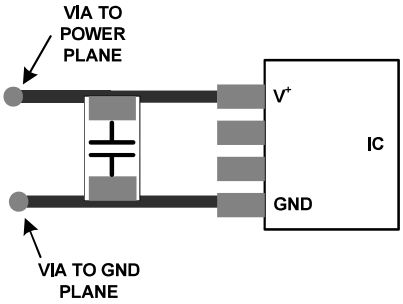


FIGURE 15. OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT - CAPACITOR AND IC ON SAME PCB LAYER (RECOMMENDED)

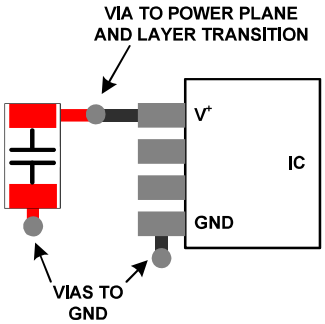


FIGURE 16. SUB-OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT - CAPACITOR AND IC ON OPPOSITE PCB LAYERS

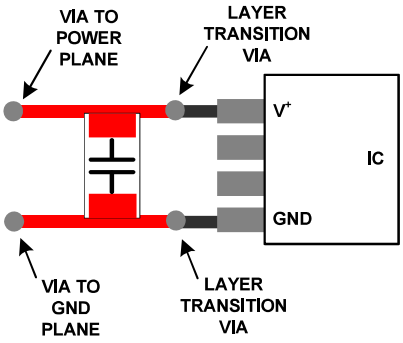


FIGURE 17. OPTIMAL LOCAL BYPASS CAPACITOR LAYOUT - CAPACITOR AND IC ON OPPOSITE PCB LAYERS (RECOMMENDED)

Other Information

Power Supply Sequencing

There are no power-up sequencing requirements. However, upon power-up or after a power glitch, and after the power supplies have settled, RSTB must be asserted for 1µs before the TW6872 can be used. For any operating mode change, soft reset followed by the appropriate register configuration must occur.

Ancillary Data

The TW6872 streams ancillary data such as line number, video payload identifier (VPID), error detection and handling (EDH) or other user defined data per SMPTE 291M. There are four lines per frame that carry ancillary data. ANC0/1/2/3 set the line number. ANCTYPE sets the blanking location. FIFO0/1/2/3CNT set the data byte count.

Audio data is also inserted into the ancillary data space from either the analog audio or I2S interface per SMPTE 299. See "Audio Input Interface" on page 14 for details on how to choose the analog or I2S interface for ancillary audio.

Hardware Interrupt

The TW6872 provides an interrupt request output using the IRQ pin. The hardware interrupt can be used to indicate when ancillary data has not been transmitted properly and check status of audio detection.

There are four lines per frame to carry ancillary data (not audio), either in HD or SD mode. Whenever an ancillary packet is not completely sent out and is truncated at the end of an ancillary line, an "ancillary data packet miss interrupt" is generated.

ANCTXERRORMASK is used to mask out the four HD mode ancillary line miss, and four SD mode ancillary line miss interrupts. If these are not masked, then an interrupt will be generated if the ancillary packet has been truncated. ANCTXERROR indicates where the failure occurred.

Crystal and Clock Oscillator

The TW6872 requires an external 27MHz crystal or oscillator. The crystal connects to the XTI/XTO pins. A low ESR, CL = 18pF, 50ppm is recommended.

Link Checker

The TW6872 has an integrated pseudo random binary sequence (PRBS) 7/23 generator which can be used for bit error rate testing. A bit error would cause one pixel to be the incorrect color for one frame. That wouldn't be noticeable if it only happened once every hour, but might be noticeable if it happened once every minute.

Bit error testing can be used to optimize operation between the TW6872 and the receiver (TW6874 or any other receiver with PRBS 7/23 checker) over the coaxial cable interface. For example, the pre/de-emphasis setting on the TW6872 and/or the receiver's equalizer settings can be adjusted to obtain minimum bit errors, indicating the best settings for that link has been obtained.

Test Patterns

The TW6872 can generate audio and video test patterns to ease system design. One such pattern is the Checkfield as shown in Figure 18. This pathological image contains two different patterns that can be used to test the link performance in case a PRBS checker is unavailable at the receiver.

FIGURE 18. CHECKFIELD PATTERN

I²C Communication Interface

The TW6872 uses a 2-wire serial bus for communication with its host. The TW6872 operates as a bus slave. SCL is the Serial Clock line, driven by the host, and SDA is the Serial Data line, which can be driven by any device on the bus. SDA is open-drain to allow multiple devices to share the same bus simultaneously. An external pull-up resistor (typically 2.2kΩ to 4.7kΩ) is required for SDA and SCL.

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high (Figure 20). The TW6872 continuously monitors the SDA and SCL lines for the START condition and will not respond to any command until this condition has been met. The host then transmits the 7-bit slave address plus a R/$\overline{W}$ bit, indicating if the next transaction will be a Read (R/$\overline{W}$ = 1) or a Write (R/$\overline{W}$ = 0).

After transmitting the device address and the R/$\overline{W}$ bit, the host must release the SDA line while holding SCL low, and wait for an acknowledgment from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDA line low to acknowledge (ACK) the condition (Figure 21). The host will then continue with the next 8-bit transfer. If no device on the bus responds (NACK, where SDA is kept high during the 9th SCL pulse), the host transmits a STOP condition where SDA rises while SCL is high and ends the cycle (Figure 20). Notice that a successful transfer always includes nine SCL pulses.

Once the slave address has been transmitted and acknowledged, one byte of information can be written to or read from the slave. Data on the serial bus must be valid for the entire time SCL is high (Figure 22). Communication with the selected device in the selected direction (read or write) is ended by a STOP command, or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

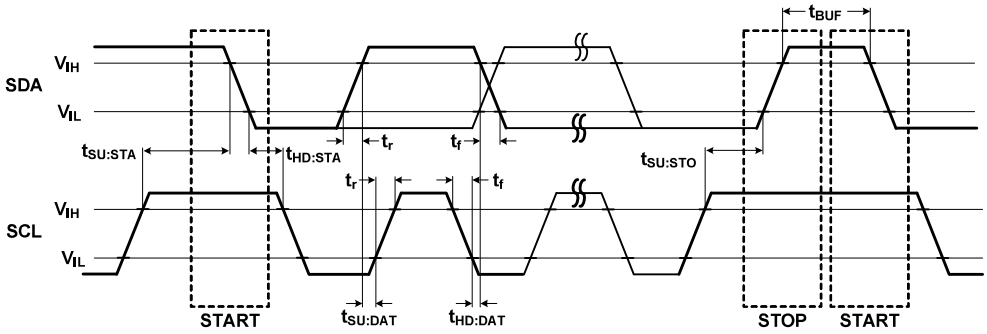


FIGURE 19. I²C TIMING DEFINITIONS

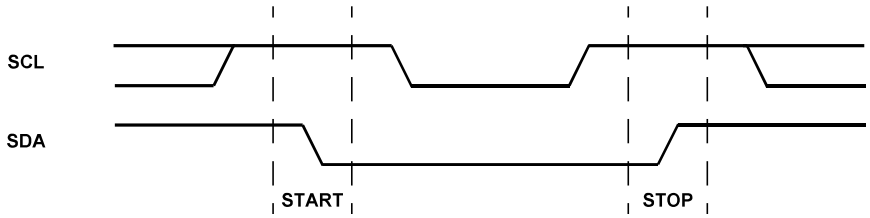


FIGURE 20. VALID START AND STOP CONDITIONS

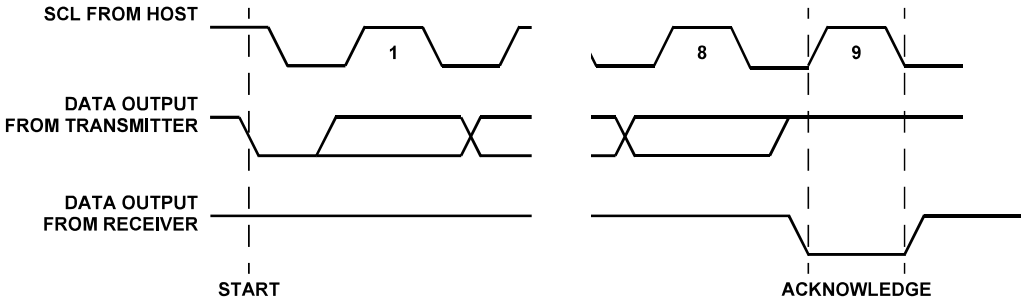


FIGURE 21. ACKNOWLEDGE RESPONSE FROM RECEIVER

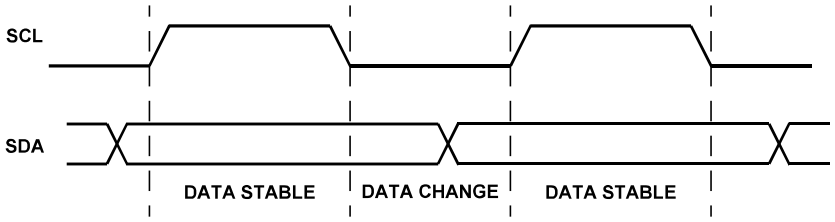


FIGURE 22. VALID DATA CHANGES ON THE SDA BUS

Configuration Register Write

After receiving the acknowledge bit corresponding to the desired TW6872's slave address byte with R/$\overline{W}$ = 0, the host sends the desired register address where data is to be written. An internal index register points to this address. After receiving the acknowledge bit corresponding to the desired register address byte, the host sends the data byte to be written. The TW6872 loads the data byte to the register pointed by the internal index register. The TW6872 acknowledges the data write and automatically increments the pointer register to point to the next register address. The host can thus write to sequential ascending register addresses. After each transfer, the TW6872 acknowledges the receipt with an acknowledge pulse. To end all transfers to the TW6872 the host issues a STOP condition.

To write to separate or non-sequential register locations, a full I^2C START, Device Address (R/$\overline{W}$ = 0), Register Address, Data Write/slave ACK..., STOP sequence must be used for each register location.

Figure 23 shows two views of the steps necessary to write one byte to the Configuration Register.

Configuration Register Read

A TW6872 read cycle has two phases. The first phase is a write to select the desired internal index register. The second phase is the read from the data register. Note that no data is actually written during the first phase.

After receiving the acknowledge bit corresponding to the desired TW6872's slave address byte with R/$\overline{W}$ = 0, the host sends the desired register address from where data is to be read. An internal index register points to this address. After receiving the acknowledge bit corresponding to the desired register address byte, the host sends either a STOP/START or a REPEATED START condition.

The host then sends the same slave address with R/$\overline{W}$ = 1 to indicate a read. The TW6872 transfers the contents of the desired register during eight SCL pulses (controlled by the host). After transferring the byte, the TW6872 releases SDA and the host acknowledges receipt of the data. The TW6872 automatically increments the pointer register to point to the next register address. The host can thus read from sequential ascending register addresses. The host acknowledges receipt of each byte. To end the read, the host does not acknowledge data receipt, and then issues a STOP condition.

To read from separate or non-sequential register locations, a full I^2C START, Device Address (R/$\overline{W}$ = 0), Register Address, STOP, START, Device Address (R/$\overline{W}$ = 1), Data Read/host ACK..., host NACK, STOP sequence must be used for each register location.

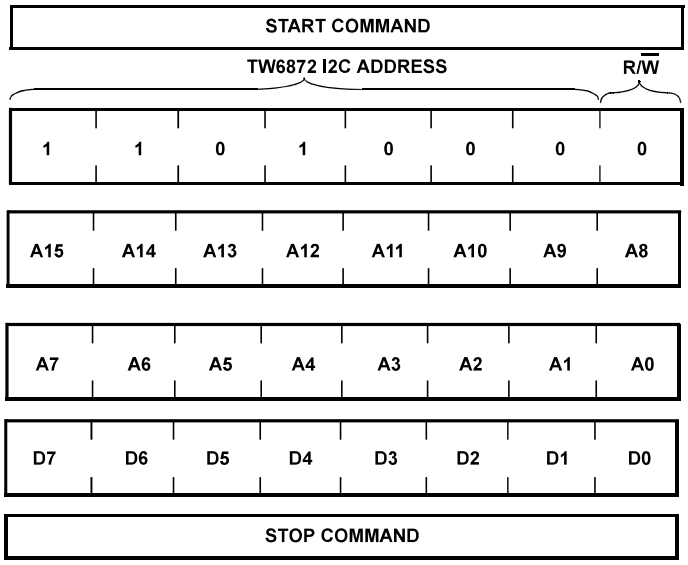
Figure 24 shows two views of the steps necessary to read one byte from the Configuration Register.

I^2C Slave Address

The TW6872 7-bit I^2C slave address is 1101000 (binary). The final 8 bit address word transmitted is 1101000r (binary) where "r" is the R/$\overline{W}$ bit indicating the direction of the next byte(s).

Register Address

Each configuration register is accessed via a 12-bit address. The upper four bits is the page; the lower byte is the address on the page. The upper four bits of the page is always 0 and should be padded as such to make a full byte. The register map lists each register address in a 12-bit format, for example: 0x123. Hence, this register address's MSB is 0x01 and its LSB is 0x23.



Signals the beginning of an I²C transaction

TW6872 Device Select Address Write

The first 7 bits of the first byte select the TW6872 on the I²C bus. R/$\overline{W}$ = 0, indicating that the next transaction will be a write.

TW6872 Register Address MSB Write

This is the address MSB of the TW6872's internal configuration register that the following data byte will be written to.

TW6872 Register Address LSB Write

This is the address LSB of the TW6872's internal configuration register that the following data byte will be written to.

TW6872 Register Data Write

This is the data to be written to the selected configuration register.

Signals the ending of the I²C transaction

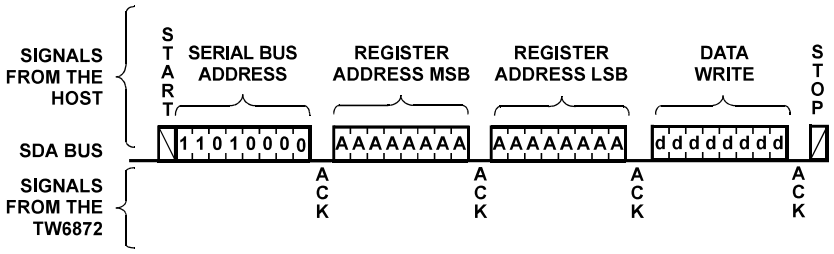
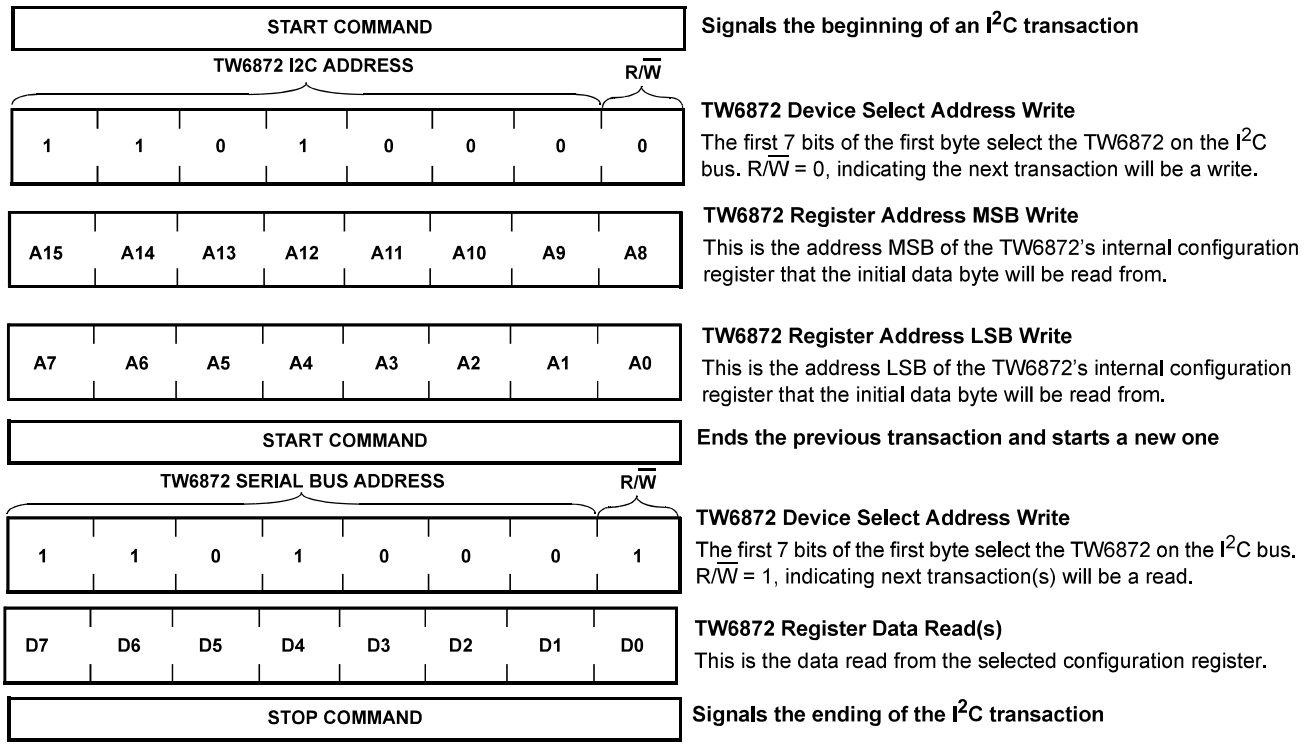


FIGURE 23. CONFIGURATION REGISTER WRITE



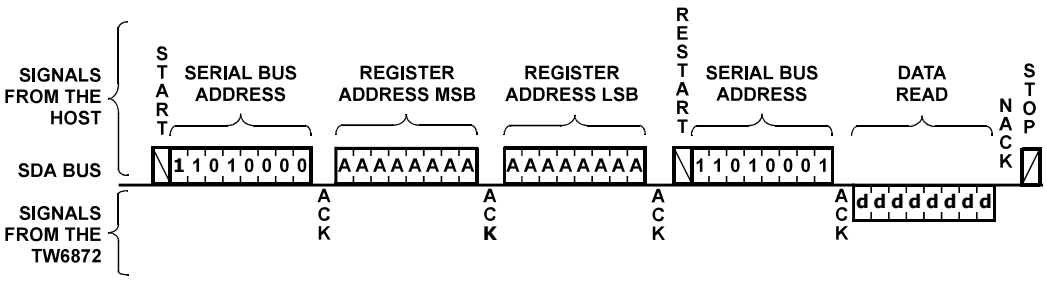


FIGURE 24. CONFIGURATION REGISTER READ

Register Map

General

TABLE 2. VIN_CTRL: VIDEO INPUT CONTROL . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x010

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	FORMAT	Set video format: 0x0: 720p59.94/60 0x1: 720p50 0x2: 1080i59.94/60 0x3: 1080i50 0x4: 1080p59.94/60 0x5: 1080p50 0x6: 1080p29.97/30 0x7: 1080p25 0x8 NTSC 0x9: PAL 0xA-0xF: reserved	0x0
3	SWAP	YC swap on VD input pins 0: Not swapped 1: Swapped	0
2	RESERVED	Reserved	0
1	VC2ENABLE	VC2 compression 0: Not enabled 1: Enabled	0
0	PATGEN	Selects video source at input 0: External BT.1120 source 1: Internal pattern generator	0

TABLE 3. TX_CTRL: TRANSMIT CONTROL . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x011

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0
1:0	RATE	Set TX link speed 0: HD 1: SD/VC2 2: 3G 3: Reserved	0

TABLE 4. SRST_CTRL: SYSTEM RESET CONTROL . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x012

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	RESERVED	Reserved	0x0
4	TXRST	Reset SDI TX and PRBS generator blocks. Not self cleared. 0: Normal operation 1: Reset	0
3:2	RESERVED	Reserved	0x0
1	VC2RST	Reset VC2 encoder. Not self cleared. 0: Normal operation 1: Reset	0
0	PIXRST	Reset pattern generator and ASI blocks. Not self cleared. 0: Normal operation 1: Reset	0

TABLE 5. DBG_CTRL: DEBUG CONTROL . . . . . READ-WRITE, DEFAULT=0x30, ADDR=0x013

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6	EDH	Insert EDH into SDI stream 0: Do not insert EDH 1: Insert EDH	0
5	LINE	Insert line number into SDI stream 0: Do not insert line number 1: Insert line number	1
4	CRC	Insert CRC into SDI stream 0: Do not insert CRC 1: Insert CRC	1
3:1	RESERVED	Reserved	0x0
0	INTPOL	Interrupt polarity 0: Interrupt is active low 1: Interrupt is active high	0

TABLE 6. CLK_CTRL: CLOCK CONTROL . . . . . .READ-WRITE, DEFAULT=0x00, ADDR=0x014

BIT	NAME	BIT DEFINITION	DEFAULT
7	VDCLKSEL	Video clock selection 0: Input clock from ISP (VD_CLK) 1: Clock internally generated by TW6872 (CLKO). For test purpose only.	0
6	VDCLKINV	Video clock invert 0: Do not invert video clock 1: Invert video clock	0
5	AADCCLKINV	Audio ADC clock invert 0: Do not invert audio ADC clock 1: Invert audio ADC clock	0
4	SDICLKINV	SDI clock invert 0: Do not invert SDI clock 1: Invert SDI clock	0
3	RESERVED	Reserved	0
2	AMCLKPD	AMCLK power-down. This is an internal audio ADC clock. 0: Normal operation 1: Power-down	0
1	CLKOPD	CLKO power-down 0: Normal operation 1: Power-down	0
0	CLK108PD	CLK108 power-down 0: Normal operation 1: Power-down	0

TABLE 7. PATGEN_CTRL_0: PATTERN GENERATOR CONTROL 0 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x015

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RP219OPT	Select RP 219 color bar option	0x0
5:4	PATSEL	Pattern select 0: RP 219 color bar 1: RP 198 check field 2: 75% color bar 3: Reserved	0x0
3:1	RESERVED	Reserved	0x0
0	PATGENEN	Pattern generator enable 0: Normal operation 1: Enable pattern generator	0

TABLE 8. MISC_CTRL: MISCELLANEOUS CONTROL . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x016

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RESERVED	Reserved	0
5	ALT10EN	Enable 1-0-1-0 pattern 0: Normal operation 1: Enable 1-0-1-0 pattern	0
4	PRBSRATE	Select PRBS rate 0: HD/3G 1: SD	0
3	PRBSPAT	Select PRBS polynomial 0: PRBS23 1: PRBS7	0
2	PRBSEN	Enable PRBS pattern 0: Normal operation 1: Enable PRBS pattern	0
1	DATATHRU	Enable data through mode (data is not SDI encoded) 0: Normal operation 1: Enable data through mode	0
0	ASIEN	Enable ASI 0: Normal operation 1: Enable ASI	0

TABLE 9. ACLK_CTRL: AUDIO CLOCK CONTROL . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x017

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0x0
1	ACLKINV	Audio clock invert 0: Not inverted 1: Inverted	0
0	ACLKSEL	Audio clock selection 0: ACLK pin is audio clock input 1: Use internally generated audio clock	0

TABLE 10. VC2_CTRL: VC2 CONTROL . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x018

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	RESERVED	Reserved	0x0

TABLE 11. STATUS: STATUS . . . . . READ-ONLY, ADDR=0x01F

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	RESERVED	Reserved	0x0
0	VC2STATE	Live state of OPT_DIRAC_PD pin	0

TABLE 12. PLL_CTRL: PLL CONTROL . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x080

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6	INPLL_REFSEL	Selects INPLL clock source 0: From XTI input 1: From divided VD_CLK input	0
5	PCLK_DIV10_SEL	Sets PISO clock divider relationship to the SDI transmit clock 0: Divide by 20 1: Divide by 10	0
4	VC2_CLKSEL	Select the SDI shift register clock from INPLL or TXPLL 0: Select TXPLL clock 1: Select INPLL 270MHz clock	0

TABLE 12. PLL_CTRL: PLL CONTROL. . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x080 (Continued)

BIT	NAME	BIT DEFINITION	DEFAULT
3	ISPCLK_DIV10_SEL	Selects CLKO divider relationship 0: Divide by 20 1: Divide by 10	0
2	ISPCLK_XTALCLK_SEL	Select XTI clock on to ISP clock 0: Select Div10/20 transmit clock for ISP clock 1: Select XTI clock for ISP clock	0
1:0	IFPLL_REFSEL	Selects the IFPLL reference from the XTI input, INPLL output, or from divided VD_CLK	0x0

TABLE 13. IFPLLMDIV: INTERMEDIATE PLL M DIVIDER . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x081

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6:0	IFPLLM2DIV	IFPLL M-divider from 9 to 128	0x0

TABLE 14. TXPLLPDIV: TRANSMIT PLL POST DIVIDER . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x082

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6:0	TXPLLP2DIV	Transmit PLL post divider from 1 to 128	0x0

TABLE 15. IFD: INTERMEDIATE FREQUENCY . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x083

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6:0	IFD	Divider to select the intermediate frequency in the TXPLL if two PLLs are used for cascading to improve performance. This is used as both the P-divider of the IFPLL and the M-divider of the TXPLL. Because of this, the IFPLL and TXPLL VCO are always running at the same frequency, unless one of them is turned off. Valid values are 9 to 128.	0x0

TABLE 16. PLLTRIM_0: PLL TRIM 0 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x084

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	PLLTRIM0	PLL trim 0. PLLTRIM[7:0]. Recommend setting PLLTRIM[7] = 1.	0x0

TABLE 17. PLLTRIM_1: PLL TRIM 1 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x085

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6:4	INPLLNDIV	INPLL N (reference input) divider. Used to divide the VD_CLK input before applying it as a reference for the INPLL.	0x0
3	RESERVED	Reserved	0
2:0	PLLTRIM1	PLL trim 1. PLLTRIM[10:8]. Recommend setting PLLTRIM[10:8] = 0x7.	0x0

TABLE 18. INPLLMDIV: INPUT PLL M DIVIDER . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x086

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6:0	INPLLM1DIV	Input PLL M-divider from 9 to 128	0x0

TABLE 19. INPLLPDIV: INPUT PLL POST DIVIDER . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x087

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6:0	INPLLP1DIV	Input PLL post divider from 9 to 128	0x0

TABLE 20. INPLLPDIVVC2: INPUT PLL POST DIVIDER FOR VC2 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x088

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6:0	INPLLP1DIVVC2	Input PLL post divider used in VC2 mode from 9 to 128	0x0

TABLE 21. ANATOP_TRIM_0: ANALOG TOP TRIM 0 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x089

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANATOP_TRIM0	General trim signals for analog top blocks. ANATOP_TRIM[7:0] ANATOP_TRIM[3] controls TXPLL power down. Set to 1 to power down. ANATOP_TRIM[2] controls IFPLL power down. Set to 1 to power down.	0x0

TABLE 22. ANATOP_TRIM_1: ANALOG TOP TRIM 1 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x08A

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANATOP_TRIM1	General trim signals for analog top blocks. ANATOP_TRIM[15:8] Recommend setting ANATOP_TRIM[15:8] = 0x33.	0x0

TABLE 23. ANATOP_TRIM_2: ANALOG TOP TRIM 2 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x08B

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANATOP_TRIM2	General trim signals for analog top blocks. ANATOP_TRIM[23:16]	0x0

TABLE 24. ANATOP_TRIM_3: ANALOG TOP TRIM 3 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x08C

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANATOP_TRIM3	General trim signals for analog top blocks. ANATOP_TRIM[31:24]	0x0

TABLE 25. PLL_PD_RESET: PLL POWER DOWN AND RESET . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x08D

BIT	NAME	BIT DEFINITION	DEFAULT
7	INPLL_PD	Power-down INPLL 0: Normal operation 1: Power-down	0
6:4	RESERVED	Reserved	0x0
3	SDITX_PD	Power-down SDI cable driver 0: Normal operation 1: Power-down	0
2:0	PLL_RESET	PLL reset; each bit resets its corresponding PLL. Not self-cleared. 0: Normal operation 1: Resets ring oscillator IFPLL 2: Resets ring oscillator INPLL	0x0

TABLE 26. PRE/DE-EMPHASIS SETTINGS

SETTING: DE (-) OR PRE (+) EMPHASIS GAIN (dB)	SETTING: DE (-) OR PRE (+) EMPHASIS GAIN (dB)
0: -7.1	8: +1.8
1: -5.4	9: +2.8
2: -4.0	10: +3.6
3: -2.8	11: +4.4
4: -1.8	12: +5.7
5: -0.9	13: +7.2
6: +0.0 (no pre/de-emphasis)	14: +9.1
7: +0.8	15: +11.5

TABLE 27. PREEMPH_BG: PRE-EMPHASIS AND BANDGAP . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x08E

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	PREEMPH	See Table 26 for settings.	0x0

TABLE 27. PREEMPH_BG: PRE-EMPHASIS AND BANDGAP .....READ-WRITE, DEFAULT=0x00, ADDR=0x08E

BIT	NAME	BIT DEFINITION	DEFAULT
3:0	BG_TRIM	Bandgap reference trim settings	0x0

TABLE 28. PLL_LOCK: PLL LOCK STATUS ..... READ-ONLY, ADDR=0x08F

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
2	INPLL_LOCK	INPLL lock status 0: Not locked 1: Locked	0
1	IFPLL_LOCK	IFPLL lock status 0: Not locked 1: Locked	0
0	TXPLL_LOCK	TXPLL lock status 0: Not locked 1: Locked	0

TABLE 29. DRV_TRIM_0: DRIVER TRIM 0..... READ-WRITE, DEFAULT=0x00, ADDR=0x090

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	DRV_TRIM0	Driver module trim. DRV_TRIM[7:0]	0x0

TABLE 30. DRV_TRIM_1: DRIVER TRIM 1..... READ-WRITE, DEFAULT=0x00, ADDR=0x091

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6:5	TXPLL_SRC	Select ISPCLK_DIV10_SEL clock source	0x0
4:0	DRV_TRIM1	Driver module trim. DRV_TRIM[12:8]	0x0

TABLE 31. ATMUX_CTRL: ANALOG TEST MUX CONTROL ..... READ-WRITE, DEFAULT=0x00, ADDR=0x092

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3:0	ATMUX_CTRL	Analog test mux control. For internal use only.	0x0

TABLE 32. DTMUX_CTRL: DIGITAL TEST MUX CONTROL..... READ-WRITE, DEFAULT=0x00, ADDR=0x093

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3	DRV_TRIM2	Driver module trim. DRV_TRIM[13]	0
2:0	RESERVED	Reserved	0x0

TABLE 33. VR_TRIM_0: VOLTAGE REGULATOR TRIM 0..... READ-WRITE, DEFAULT=0x00, ADDR=0x094

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VR_TRIM0	Voltage regulator trim. VR_TRIM[7:0] Recommend setting VR_TRIM[7:0] = 0x33.	0x0

TABLE 34. VR_TRIM_1: VOLTAGE REGULATOR TRIM 1..... READ-WRITE, DEFAULT=0x00, ADDR=0x095

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	VR_TRIM1	Voltage regulator trim. VR_TRIM[15:8] Recommend setting VR_TRIM[15:8] = 0x33.	0x0

TABLE 35. PLLX4_CTRL_0: PLLX4 CONTROL 0 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x098

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0x0
1	PPLOE	PPL output enable 0: Enabled 1: Disabled	0
0	PLLX4PD	PLLX4 power down 0: Normal operation 1: Power down	0

TABLE 36. PLLX4_CTRL_1: PLLX4 CONTROL 1 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x099

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3:1	CPX	CPX	0x0
0	IREF	IREF	0

TABLE 37. CHIP_REV: CHIP REVISION . . . . . READ-WRITE, DEFAULT=0x1A, ADDR=0x0FF

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	CHIP_REV	Chip revision number	0x1A

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TABLE 38. AUD_CTRL_0: AUDIO CONTROL 0 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x100

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RESERVED	Reserved	0x0
5	ASYNAUDSEL	Asynchronous audio select 0: Not selected 1: Selected	0
4	RESERVED	Reserved	0
3	AUDHDMODE	Audio HD mode select 0: Not selected 1: Selected	0
2	AUDSDMODE	Audio SD mode select 0: Not selected 1: Selected	0
1	RESERVED	Reserved	0
0	AUDEN	Audio enable 0: Disable. All audio state machines are reset. 1: Enable	0

TABLE 39. AUD_FLAG: AUDIO FLAG. . . . . READ-WRITE, DEFAULT=0x03, ADDR=0x101

BIT	NAME	BIT DEFINITION	DEFAULT
7	AUDSWAP	Audio channel swap 0: Normal operation 1: Swap channels	0
6	AUDMUTE1	Audio channel 1 mute 0: Normal operation 1: Mute	0
5	AUDMUTE0	Audio channel 0 mute 0: Normal operation 1: Mute	0

TABLE 39. AUD_FLAG: AUDIO FLAG. . . . . READ-WRITE, DEFAULT=0x03, ADDR=0x101

BIT	NAME	BIT DEFINITION	DEFAULT
4:2	AUDRATE	Audio sample rate 0: 48kHz (TW6872 only supports 48kHz) 1: 44.1kHz 2: 32kHz	0x0
1	AUDACT1	Audio channel 1 active flag 0: Not active 1: Active	1
0	AUDACT0	Audio channel 0 active flag 0: Not active 1: Active	1

TABLE 40. AUD_DID0: AUDIO ANC DID 0 . . . . . READ-WRITE, DEFAULT=0xFF, ADDR=0x103

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	AUD_DID0	Audio ANC DID 0. AUD_DID[7:0]	0xFF

TABLE 41. AUD_DID0: AUDIO ANC DID 1 . . . . . READ-WRITE, DEFAULT=0x02, ADDR=0x104

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0x0
1:0	AUD_DID1	Audio ANC DID 1. AUD_DID[9:8]	0x2

TABLE 42. AUD_CTRLPKT_0: AUDIO ANC CONTROL PACKET 0 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x107

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	AUD_CTRLPKT_0	Audio ANC control 0. AUD_CTRLPKT[7:0]	0x0

TABLE 43. AUD_CTRLPKT_1: AUDIO ANC CONTROL PACKET 1 . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x108

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0x0
1:0	AUD_CTRLPKT_1	Audio ANC control 1. AUD_CTRLPKT[9:8]	0x2

TABLE 44. AUD_CTRL: AUDIO CONTROL . . . . . READ-WRITE, DEFAULT=0x07, ADDR=0x109

BIT	NAME	BIT DEFINITION	DEFAULT
7	BITORDER	Select LSB first 0: MSB first 1: LSB first	0
6	LEFTJUST	Left justify 0: Right justify 1: Left justify	0
5:4	WIDTH	Audio word width 0: 16-bit 1: 20-bit 2: 24-bit	0x0
3	RESERVED	Reserved	0
2	INTERLACE	Video interlaced 0: Video is not interlaced 1: Video is interlaced	1
1:0	LINERST	Reset line counter 0: Reset on VAV rising edge 1: Reset on field rising edge 2: Reset on field falling edge 3: Reset on both edges of field	0x3

TABLE 45. AUD_MAXPKT: MAXIMUM AUDIO PACKET COUNT ..... READ-WRITE, DEFAULT=0x00, ADDR=0x10A

BIT	NAME	BIT DEFINITION	DEFAULT
7:5	RESERVED	Reserved	0x0
4:0	AUD_MAXPKT	Maximum number of ANC audio packets per line	0x0

TABLE 46. SWFD0_0: FIELD 0 SWITCH 0 ..... READ-WRITE, DEFAULT=0x07, ADDR=0x10B

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SWFD0_0	Switch line number for progressive video or field 0 for interlaced video. AUD_SWFD0[7:0]	0x7

TABLE 47. SWFD0_1: FIELD 0 SWITCH 1 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x10C

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	RESERVED	Reserved	0x0
2:0	SWFD0_1	Switch line number for progressive video or field 0 for interlaced video. AUD_SWFD0[10:8]	0x0

TABLE 48. SWFD1_0: FIELD 1 SWITCH 0 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x10D

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	SWFD1_0	Switch line number for field 1 for interlaced video. Not used for progressive video. AUD_SWFD1[7:0]	0x0

TABLE 49. SWFD1_1: FIELD 1 SWITCH 1 .....READ-WRITE, DEFAULT=0x00, ADDR=0x10E

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	RESERVED	Reserved	0x0
2:0	SWFD1_1	Switch line number for field 1 for interlaced video. Not used for progressive video. AUD_SWFD1[10:8]	0x0

TABLE 50. ANCLOC: ANC DATA LOCATION ..... READ-WRITE, DEFAULT=0x00, ADDR=0x111

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3	VIDMODE	Select PAL or NTSC format 0: NTSC 1: PAL	0
2	RESERVED	Reserved	0
1	I2SINWIDTH	Selects I2S audio input width 0: 32-bit 1: 16-bit	0
0	AUDLOC	ANC audio packet insertion location 1: Insert audio packet 4 bytes after EAV	0

TABLE 51. ANCEN: ENABLE ANC DATA PACKET ..... READ-WRITE, DEFAULT=0x00, ADDR=0x112

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3	ANC3EN	ANC packet3 enable 0: Not enabled 1: Enabled	0
2	ANC2EN	ANC packet2 enable 0: Not enabled 1: Enabled	0
1	ANC1EN	ANC packet2 enable 0: Not enabled 1: Enabled	0

TABLE 51. ANCEN: ENABLE ANC DATA PACKET ..... READ-WRITE, DEFAULT=0x00, ADDR=0x112

BIT	NAME	BIT DEFINITION	DEFAULT
0	ANC0EN	ANC packet1 enable 0: Not enabled 1: Enabled	0

TABLE 52. ANCDAT0: ANC FIFO DATA 0 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x120

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANCDAT0	Ancillary data for FIFO0	0x0

TABLE 53. ANCDAT1: ANC FIFO DATA 1 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x121

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANCDAT1	Ancillary data for FIFO1	0x0

TABLE 54. ANCDAT2: ANC FIFO DATA 2 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x122

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANCDAT2	Ancillary data for FIFO2	0x0

TABLE 55. ANCDAT3: ANC FIFO DATA 3 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x123

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANCDAT3	Ancillary data for FIFO3	0x0

TABLE 56. ANCFIFO: ANC FIFO ..... READ-WRITE, DEFAULT=0x00, ADDR=0x124

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	RESERVED	Reserved	0x0
0	ANCFIFORST	ANC FIFO write pointer reset 0: Normal operation 1: Reset	0

TABLE 57. ANCLINE0_0: ANC PACKET0 LINE NUMBER 0 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x125

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANCLINE0_0	Line number for ANC data packet0. ANCLINE0[7:0]	0x0

TABLE 58. ANCLINE0_1: ANC PACKET0 LINE NUMBER 1 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x126

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	RESERVED	Reserved	0x0
2:0	ANCLINE0_1	Line number for ANC data packet0. ANCLINE0[10:8]	0x0

TABLE 59. ANCLINE1_0: ANC PACKET1 LINE NUMBER 0 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x127

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANCLINE1_0	Line number for ANC data packet1. ANCLINE1[7:0]	0x0

TABLE 60. ANCLINE1_1: ANC PACKET1 LINE NUMBER 1 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x128

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	RESERVED	Reserved	0x0
2:0	ANCLINE1_1	Line number for ANC data packet1. ANCLINE1[10:8]	0x0

TABLE 61. ANCLINE2_0: ANC PACKET2 LINE NUMBER 0 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x129

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANCLINE2_0	Line number for ANC data packet2. ANCLINE2[7:0]	0x0

TABLE 62. ANCLINE2_1: ANC PACKET2 LINE NUMBER 1 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x12A

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	RESERVED	Reserved	0x0
2:0	ANCLINE2_1	Line number for ANC data packet2. ANCLINE2[10:8]	0x0

TABLE 63. ANCLINE3_0: ANC PACKET3 LINE NUMBER 0 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x12B

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ANCLINE3_0	Line number for ANC data packet3. ANCLINE3[7:0]	0x0

TABLE 64. ANCLINE3_1: ANC PACKET3 LINE NUMBER 1 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x12C

BIT	NAME	BIT DEFINITION	DEFAULT
7:3	RESERVED	Reserved	0x0
2:0	ANCLINE3_1	Line number for ANC data packet3. ANCLINE3[10:8]	0x0

TABLE 65. FIFO0CNT_0: FIFO0 BYTE COUNT 0 ..... READ-WRITE, DEFAULT=0x00, ADDR=0x12D

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	FIFO0CNT_0	Byte count in ANC FIFO0. FIFO0CNT[7:0]	0x0

TABLE 66. FIFO0CNT_1: FIFO0 BYTE COUNT 1 .....READ-WRITE, DEFAULT=0x00, ADDR=0x12E

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0x0
1:0	FIFO0CNT_1	Byte count in ANC FIFO0. FIFO0CNT[1:0]	0x0

TABLE 67. FIFO1CNT: FIFO1 BYTE COUNT .....READ-WRITE, DEFAULT=0x00, ADDR=0x12F

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	FIFO1CNT	Byte count in ANC FIFO1	0x0

TABLE 68. FIFO2CNT: FIFO2 BYTE COUNT. ..... READ-WRITE, DEFAULT=0x00, ADDR=0x130

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	FIFO2CNT	Byte count in ANC FIFO2	0x0

TABLE 69. FIFO3CNT: FIFO3 BYTE COUNT. ..... READ-WRITE, DEFAULT=0x00, ADDR=0x131

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	FIFO3CNT	Byte count in ANC FIFO3	0x0

TABLE 70. ANCTYPE: ANC DATA TYPE. ..... READ-WRITE, DEFAULT=0x00, ADDR=0x132

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3	ANCTYPE3	ANC type for FIFO3 0: VANC 1: HANC	0
2	ANCTYPE2	ANC type for FIFO2 0: VANC 1: HANC	0

TABLE 70. ANCTYPE: ANC DATA TYPE. . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x132

BIT	NAME	BIT DEFINITION	DEFAULT
1	ANCTYPE1	ANC type for FIFO1 0: VANC 1: HANC	0
0	ANCTYPE0	ANC type for FIFO0 0: VANC 1: HANC	0

TABLE 71. AUDSRC: AUDIO SOURCE . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x140

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	RESERVED	Reserved	0x0
0	AUDSRC	Audio source select 0: I2S 1: Analog ADC	0

TABLE 72. AUDPAT: AUDIO PATTERN CONTROL. . . . . .READ-WRITE, DEFAULT=0x00, ADDR=0x141

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	AUDFREQ1	Audio pattern sine wave frequency for ch1 0: 1kHz 1: 1/6kHz 2: 1/3kHz 3: 1/2kHz	0x0
5:4	AUDFREQ0	Audio pattern sine wave frequency for ch0 0: 1kHz 1: 1/6kHz 2: 1/3kHz 3: 1/2kHz	0x0
3:2	I2SPAT	I2S input pattern format 0: 1/4 audio gain 1: 1/2 audio gain 2: 1/1 audio gain 3: Audio data is 10-bit incremental count	0x0
1	RESERVED	Reserved	0
0	PATSEL	I2S audio source select 0: I2S input 1: Pattern generator	0

TABLE 73. I2STX_CTRL: I2S TX CONTROL. . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x142

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0x0
1	I2SMASTER	I2S master mode select 0: Slave 1: Master	0
0	I2STXEN	I2S TX data output enable 0: Not enabled 1: Enabled	0

TABLE 74. AUDFIFO: AUDIO FIFO STATUS . . . . . READ-ONLY, ADDR=0x143

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RESERVED	Reserved	0x0
5	SDFIFOALMOSTEMPTY	SD audio FIFO almost empty. Sticky bit cleared on read. 0: FIFO not almost empty 1: FIFO almost empty	0

TABLE 74. AUDFIFO: AUDIO FIFO STATUS . . . . . READ-ONLY, ADDR=0x143 (Continued)

BIT	NAME	BIT DEFINITION	DEFAULT
4	SDFIFOALMOSTFULL	SD audio FIFO almost full. Sticky bit cleared on read. 0: FIFO not almost full 1: FIFO almost full	0
3	SDFIFOEMPTY	SD audio FIFO empty. Sticky bit cleared on read. 0: FIFO not empty 1: FIFO empty	0
2	SDFIFOFULL	SD audio FIFO full. Sticky bit cleared on read. 0: FIFO not full 1: FIFO full	0
1	HDFIFOEMPTY	HD audio FIFO empty. Sticky bit cleared on read. 0: FIFO not empty 1: FIFO empty	0
0	HDFIFOFULL	HD audio FIFO full. Sticky bit cleared on read. 0: FIFO not full 1: FIFO full	0

TABLE 75. AUDBLANK: AUDIO BLANK LINE FLAG . . . . . READ-ONLY, ADDR=0x1F0

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0x0
1	HDBLANK	HD audio blank line encountered. Sticky bit cleared on read. 0: Blank line not encountered 1: Blank line encountered	0
0	SDBLANK	SD audio blank line encountered. Sticky bit cleared on read. 0: Blank line not encountered 1: Blank line encountered	0

TABLE 76. ANCTXERROR: ANCILLARY SEND ERROR . . . . . READ-ONLY, ADDR=0x1F1

BIT	NAME	BIT DEFINITION	DEFAULT
7	ANCHDTXERR3	ANC data in FIFO3 failed to complete transmit in HD mode. Sticky bit cleared on read. 0: Did not fail TX 1: Failed TX	0
6	ANCHDTXERR2	ANC data in FIFO2 failed to complete transmit in HD mode. Sticky bit cleared on read. 0: Did not fail TX 1: Failed TX	0
5	ANCHDTXERR1	ANC data in FIFO1 failed to complete transmit in HD mode. Sticky bit cleared on read. 0: Did not fail TX 1: Failed TX	0
4	ANCHDTXERR0	ANC data in FIFO0 failed to complete transmit in HD mode. Sticky bit cleared on read. 0: Did not fail TX 1: Failed TX	0
3	ANCSDTXERR3	ANC data in FIFO3 failed to complete transmit in SD mode. Sticky bit cleared on read. 0: Did not fail TX 1: Failed TX	0
2	ANCSDTXERR2	ANC data in FIFO2 failed to complete transmit in SD mode. Sticky bit cleared on read. 0: Did not fail TX 1: Failed TX	0
1	ANCSDTXERR1	ANC data in FIFO1 failed to complete transmit in SD mode. Sticky bit cleared on read. 0: Did not fail TX 1: Failed TX	0
0	ANCSDTXERR0	ANC data in FIFO0 failed to complete transmit in SD mode. Sticky bit cleared on read. 0: Did not fail TX 1: Failed TX	0

TABLE 77. AUDBLANKMASK: AUDIO BLANK LINE MASK . . . . . READ-WRITE, DEFAULT=0x03, ADDR=0x1FE

BIT	NAME	BIT DEFINITION	DEFAULT
7:2	RESERVED	Reserved	0x0
1	HDBLANKMASK	HD audio blank line encountered interrupt masked. 0: Not masked 1: Masked	1
0	SDBLANKMASK	SD audio blank line encountered interrupt masked. 0: Not masked 1: Masked	1

TABLE 78. ANCTXERRORMASK: ANCILLARY SEND ERROR MASK . . . . . READ-WRITE, DEFAULT=0xFF, ADDR=0x1FF

BIT	NAME	BIT DEFINITION	DEFAULT
7	ANCHDTXERRMASK3	ANC data in FIFO3 failed to complete transmit in HD mode masked. 0: Not masked 1: Masked	1
6	ANCHDTXERRMASK2	ANC data in FIFO2 failed to complete transmit in HD mode masked. 0: Not masked 1: Masked	1
5	ANCHDTXERRMASK1	ANC data in FIFO1 failed to complete transmit in HD mode masked. 0: Not masked 1: Masked	1
4	ANCHDTXERRMASK0	ANC data in FIFO0 failed to complete transmit in HD mode masked. 0: Not masked 1: Masked	1
3	ANCSDTXERRMASK3	ANC data in FIFO3 failed to complete transmit in SD mode masked. 0: Not masked 1: Masked	1
2	ANCSDTXERRMASK2	ANC data in FIFO2 failed to complete transmit in SD mode masked. 0: Not masked 1: Masked	1
1	ANCSDTXERRMASK1	ANC data in FIFO1 failed to complete transmit in SD mode masked. 0: Not masked 1: Masked	1
0	ANCSDTXERRMASK0	ANC data in FIFO0 failed to complete transmit in SD mode masked. 0: Not masked 1: Masked	1

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TABLE 79. AUDIO GAIN SETTINGS

SETTING: GAIN	SETTING: GAIN
0: 0.25 1: 0.31 2: 0.38 3: 0.44 4: 0.50 5: 063 6: 0.75 7: 0.88	8: 1.00 9: 1.25 10: 1.50 11: 1.75 12: 2.00 13: 2.25 14: 2.50 15: 2.75

TABLE 80. ADCGAIN: AUDIO ADC GAIN CONTROL . . . . . READ-WRITE, DEFAULT=0x88, ADDR=0x200

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	ADC1GAIN	Audio ADC1 gain. See Table 79 for gain settings.	0x8
3:0	ADC0GAIN	Audio ADC0 gain. See Table 79 for gain settings.	0x8

TABLE 81. ADCCLK: ADC CLOCK CONTROL . . . . . READ-WRITE, DEFAULT=0x22, ADDR=0x20B

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6	ADCCLKEN	Audio ADC clock enable 0: Not enabled 1: Enabled	1
5:2	RESERVED	Reserved	0x0
1	I2SCLKEN	I2S WCLK output enable 0: Enabled 1: Not enabled	1
0	CLKSOURCE	ACLK source selection 0: ACLK is input to the ACLKR pin 1: ACLK is output from the ACLKR pin	0

TABLE 82. ADCCLKPHASE: ADC CLOCK PHASE. . . . . .READ-WRITE, DEFAULT=0x00, ADDR=0x210

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6	ADCCLKPHASE	Invert ADC clock 0: Not inverted 1: Inverted	0
5:0	RESERVED	Reserved	0x0

TABLE 83. AUDDET_0: AUDIO DETECTION CONTROL 0. . . . . .READ-WRITE, DEFAULT=0xF0, ADDR=0x211

BIT	NAME	BIT DEFINITION	DEFAULT
7	AUDDETMODE	Audio detection mode 0: Absolute amplitude is greater than threshold 1: Differential amplitude is greater than threshold (recommended)	1
6:4	AUDDETFILTER	Audio detection filter 0 (narrower) through 7 (wider)	0x7
3:2	RESERVED	Reserved	0x0
1	ADC1TH_1	ADC1 audio detection threshold ADC1TH[4]	0
0	ADC0TH_1	ADC0 audio detection threshold ADC0TH[4]	0

TABLE 84. AUDDET_1: AUDIO DETECTION CONTROL 1. . . . . READ-WRITE, DEFAULT=0x33, ADDR=0x212

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	ADC1TH_0	ADC1 audio detection threshold ADC1TH[3:0]	0x3
3:0	ADC0TH_0	ADC0 audio detection threshold ADC0TH[3:0]	0x3

TABLE 85. ACKI_0: ACLKI INCREMENT 0 . . . . . READ-WRITE, DEFAULT=0x23, ADDR=0x214

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ACKI_0	ACKI clock increment in ACKG block. ACKI[7:0]	0x23

TABLE 86. ACKI_1: ACLKI INCREMENT 1 . . . . . READ-WRITE, DEFAULT=0x48, ADDR=0x215

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ACKI_1	ACKI clock increment in ACKG block. ACKI[15:8]	0x48

TABLE 87. ACKI_2: ACLKI INCREMENT 2. . . . . .READ-WRITE, DEFAULT=0x07, ADDR=0x216

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RESERVED	Reserved	0x0
5:0	ACKI_2	ACKI clock increment in ACKG block. ACKI[21:16]	0x7

TABLE 88. SCLKDIV: SERIAL CLOCK DIVIDER ..... READ-WRITE, DEFAULT=0x00, ADDR=0x21A

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RESERVED	Reserved	0x0
5:0	SDIV	Serial clock divider in ACKG block	0x0

TABLE 89. ACKG_CTRL: ACKG CONTROL .....READ-WRITE, DEFAULT=0xC4, ADDR=0x21C

BIT	NAME	BIT DEFINITION	DEFAULT
7	ACKG_0	Loop control in ACKG block	1
6:4	ACKG_1	Loop control in ACKG block	0x4
3	RESERVED	Reserved	0
2	ACKG_2	Loop control in ACKG block 0: Closed loop (special purpose only) 1: Open loop (normal operation)	1
1:0	RESERVED	Reserved	0x0

TABLE 90. ACLK_CTRL_0: AUDIO CLOCK CONTROL 0..... READ-WRITE, DEFAULT=0x10, ADDR=0x21D

BIT	NAME	BIT DEFINITION	DEFAULT
7	ACKGREF	ACKG reference input (refin) selection (test purpose). When ACPL=1, this register has no effect. 0: Use video VRST refin input selected by VRSTSEL 1: Use audio WCLK	0
6:5	RESERVED	Reserved	0x0
4	AUDSYSCLKFREQ	Audio system clock frequency select 0: 27MHz 1: 36MHz	1
3:0	RESERVED	Reserved	0x0

TABLE 91. ACLK_CTRL_1: AUDIO CLOCK CONTROL 1.....READ-WRITE, DEFAULT=0x00, ADDR=0x21E

BIT	NAME	BIT DEFINITION	DEFAULT
7	LOWAUD	When analog input is less than ADET_TH, output PCM data will be 0x0000 (0x00). 0: No effect 1: Enabled	0
6:5	RESERVED	Reserved	0x0
4	ADCPD	Audio ADC power-down 0: Normal operation 1: Power-down	0
3:0	RESERVED	Reserved	0x0

TABLE 92. ADC_TEST: AUDIO ADC TEST CONTROL .....READ-WRITE, DEFAULT=0x07, ADDR=0x224

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6	ADC_RST_CLK	Audio ADC and clock soft reset 0: Reset 1: Normal operation	0
5	ADC_RST_OUT	Audio ADC digital output reset 0: Normal operation 1: Reset	0
4	ADC_RST_DIV	Audio ADC divider reset (test purpose) 0: Normal operation 1: Reset	0

TABLE 92. ADC_TEST: AUDIO ADC TEST CONTROL . . . . . READ-WRITE, DEFAULT=0x07, ADDR=0x224

BIT	NAME	BIT DEFINITION	DEFAULT
3	ADC_CAL	Audio ADC calibration (test purpose) 0: Normal operation 1: Calibrate	0
2:0	ADC_SAVE	Audio ADC SAVE mode test 7: Normal operation other: Test mode	0x7

TABLE 93. ADC_OFFSET: ADC OFFSET . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x225

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3:2	ADCOFFSET1_1	ADC1 input data offset. ADCOFFSET1[9:8]	0x0
1:0	ADCOFFSET0_1	ADC0 input data offset. ADCOFFSET0[9:8]	0x0

TABLE 94. ADC0_OFFSET: ADC0 OFFSET . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x226

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADCOFFSET0_0	ADC0 input data offset. ADCOFFSET0[7:0]	0x0

TABLE 95. ADC1_OFFSET: ADC1 OFFSET . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x227

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	ADCOFFSET1_0	ADC1 input data offset. ADCOFFSET1[7:0]	0x0

TABLE 96. NOISERED: NO INPUT NOISE REDUCTION . . . . . READ-WRITE, DEFAULT=0x20, ADDR=0x22A

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RESERVED	Reserved	0x0
5	NOISERED	No input noise reduction 0: Noise reduction on (test purpose) 1: Noise reduction off	1
4:0	RESERVED	Reserved	0x0

TABLE 97. ADCSIGNREV: ADC SIGN REVERSE . . . . . READ-WRITE, DEFAULT=0x01, ADDR=0x22B

BIT	NAME	BIT DEFINITION	DEFAULT
7:1	RESERVED	Reserved	0x0
0	ADCSIGNREV	Reverse ADC data sign 0: Not reversed 1: Reversed	1

TABLE 98. ADCTSTPATFRQ: ADC TEST PATTERN FREQUENCY . . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x22E

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3:2	ADC1TSTPATFRQ	Audio ADC1 test pattern since wave frequency 0: 6kHz 1: 1kHz 2: 2kHz 3: 3kHz	0x0
1:0	ADC0TSTPATFRQ	Audio ADC0 test pattern since wave frequency 0: 6kHz 1: 1kHz 2: 2kHz 3: 3kHz	0x0

TABLE 99. ADC_CTRL_1: ADC CONTROL 1. . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x230

BIT	NAME	BIT DEFINITION	DEFAULT
7:6	RESERVED	Reserved	0x0
5	ACLKINV	ACLK input invert 0: Not inverted 1: Inverted	0
4	RESERVED	Reserved	0
3	AFAUTO	Select auto or manual (ACKI) setup. Effective only if ACLKRMASTER==1. 0: Manual configuration of ACKI 1: Auto setup of ACKI per AFMD	0
2:0	AFMD	AFAUTO sampling frequency selection 0: 8kHz 1: 16kHz 2: 32kHz 3: 44.1kHz 4: 48kHz others: not used	0x0

TABLE 100. ADC_CTRL_2: ADC CONTROL 2. . . . . .READ-WRITE, DEFAULT=0x40, ADDR=0x231

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6	MASCKMD	Audio clock master ACLK duty cycle 0: high period is one 36MHz clock period 1: almost 50% duty cycle. If 1, then ACKI needs to be doubled. Normally used with SDIV=0.	1
5:0	RESERVED	Reserved	0x0

TABLE 101. AUDFXCTRL: AUDIO SAMPLING MODE CONTROL. . . . . READ-WRITE, DEFAULT=0x00, ADDR=0x234

BIT	NAME	BIT DEFINITION	DEFAULT
7	RESERVED	Reserved	0
6	ACLK32	ACLKR clock output mode for special 2-word output interface. Effective for ACLKRMASTER==1 only. 0: ACLKR is normal 1: 32ACLKR clocks per sample	0
5	ACLK128	ACLKR clock output mode for special 16x8-bit (128-bit total) data interface 0: ACLKR output is normal 1: 128 ACLKR clocks per sample. Effective when I2S_8BIT==1 (special purpose 8-bit mode).	0
4	ACLK64	ACLKR clock output mode for special 4-word output interface. Effective for ACLKRMASTER==1 only. 0: ACLKR is normal 1: 64 ACLKR clocks per sample	0
3	AFS384	Special audio sampling mode. ACLKR runs at: 0: Normal sampling mode. If AIN5MD==0: 256*Fs 1: 384*Fs	0
2	AIN5MD	Audio input process mode 0: four channel (AIN0/AIN1/AIN2/AIN3) audio input processing only. If AFS384==0: 256*Fs. In this mode, AIN4 is not processed. 1: five channel (AIN0/AIN1/AIN2/AIN3/AIN4) audio input processing. If AFS384==0: 320*Fs.	0
1:0	RESERVED	Reserved	0x0

TABLE 102. AUDADCDATA: AUDIO ADC DATA. . . . . READ-ONLY, ADDR=0x245

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0

TABLE 102. AUDADCDATA: AUDIO ADC DATA. . . . . READ-ONLY, ADDR=0x245

BIT	NAME	BIT DEFINITION	DEFAULT
3:2	AUDADC1DAT_1	Audio ADC1 data. AUDADC1DAT[9:8]	0x0
1:0	AUDADC0DAT_1	Audio ADC0 data. AUDADC0DAT[9:8]	0x0

TABLE 103. AUDADC0DATA: AUDIO ADC0 DATA . . . . . READ-ONLY, ADDR=0x246

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	AUDADC0DAT_0	Audio ADC0 data. AUDADC0DAT[7:0]	0x0

TABLE 104. AUDADC1DATA: AUDIO ADC1 DATA . . . . . READ-ONLY, ADDR=0x247

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	AUDADC1DAT_0	Audio ADC1 data. AUDADC1DAT[7:0]	0x0

TABLE 105. AUDADCDATAOFFSET: AUDIO ADC DATA WITH OFFSET . . . . . READ-ONLY, ADDR=0x24A

BIT	NAME	BIT DEFINITION	DEFAULT
7:4	RESERVED	Reserved	0x0
3:2	AUDADC1DATOFFSET_1	Audio ADC1 data with offset. AUDADC1DATOFFSET[9:8]	0x0
1:0	AUDADC0DATOFFSET_1	Audio ADC0 data with offset. AUDADC0DATOFFSET[9:8]	0x0

TABLE 106. AUDADC0DATAOFFSET: AUDIO ADC0 DATA WITH OFFSET. . . . . READ-ONLY, ADDR=0x24B

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	AUDADC0DAT_0	Audio ADC0 data with offset. AUDADC0DATOFFSET[7:0]	0x0

TABLE 107. AUDADC1DATAOFFSET: AUDIO ADC1 DATA WITH OFFSET . . . . . READ-ONLY, ADDR=0x24C

BIT	NAME	BIT DEFINITION	DEFAULT
7:0	AUDADC1DAT_0	Audio ADC1 data with offset. AUDADC1DATOFFSET[7:0]	0x0

Document Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 23, 2014	FN8616.0	Initial Release.

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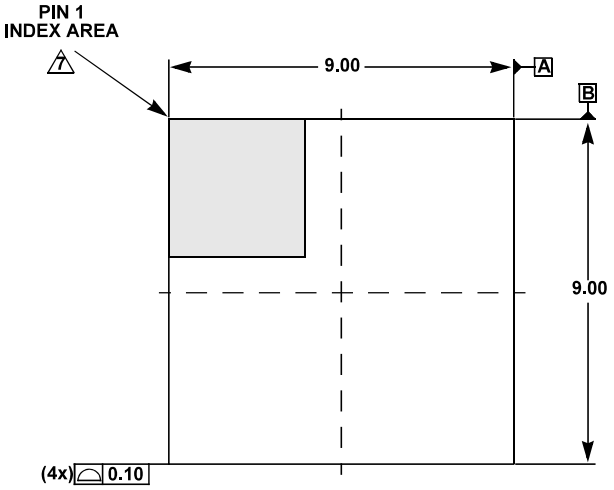
Package Outline Drawing

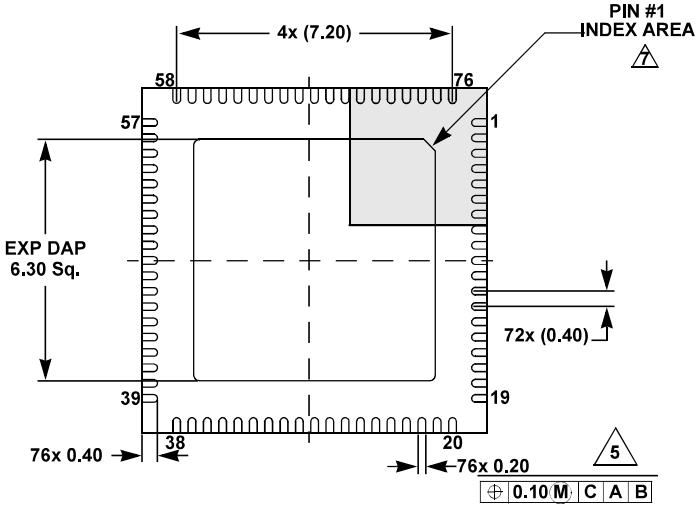
L76.9x9

76 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (QFN)

Rev 0, 5/13



TOP VIEW



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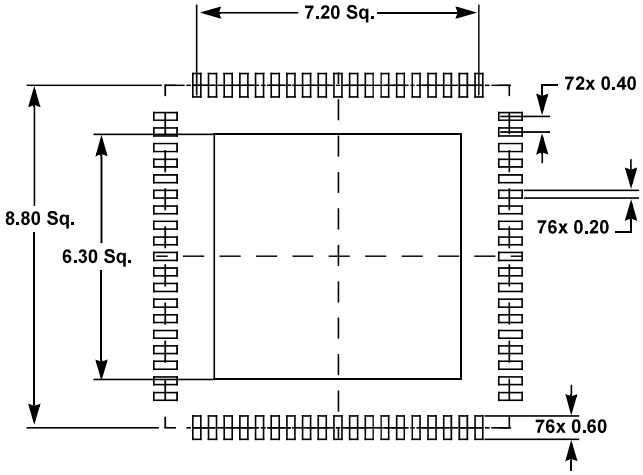
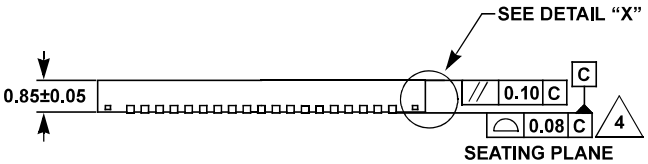
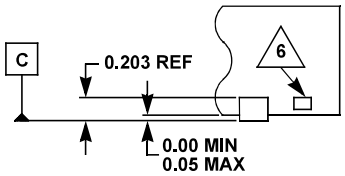


TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ANSI Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Package warpage Max 0.08mm.
5. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. Tiebar shown (if present) is a non-functional feature.
7. The configuration of the pin #1 identifier is optional, but must be lcated within the zone indicated. The pin 1 identifier may be ither a mold or mark feature.