ISL68200DEMO1Z

Demonstration Board User Guide

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The ISL68200 is a single-phase synchronous buck PWM controller featuring Intersil's proprietary R4™ Technology, which has extremely fast transient performance, accurately regulated frequency control, and all internal compensation. The ISL68200 supports a wide 4.5V to 24V input voltage range and a wide 0.5V to 5.5V output range. It includes programmable functions and telemetries for easy use and high system flexibility using SMBus, PMBus, or I^2C interface. See the ISL68200 datasheet for more details.

The ISL68200DEMO1Z is a 6-layer board demonstrating a compact 17mmx17mm 20A synchronous buck converter. Transient performance, fault protections, DC/AC regulations, PMBus programming, power sequencing, margining, and other features can be evaluated using this board.

The PMBus dongle (ZLUSBEVAL3Z USB-to-PMBus adapter) and USB cable are included with the demonstration board. Intersil's evaluation software can be installed from Intersil's website and be used to evaluate the full PMBus functionality of the part using a PC running Microsoft Windows.

Related Literature

- For a full list of related documents, visit our website
  - ISL68200 product page
- Intersil's PowerNavigator User Guide

Key Features

- 20A synchronous buck converter with PMBus control
- On-board transient load with adjustable di/dt
- Configurable through resistor pins
- Cascadeable PMBus connectors
- Integrated LDOs for a single rail solution
- Enable switch and power-good indicator
- All ceramics solution with SP capacitor footprint option

Target Specifications

- V_{IN} = 4.75V to 14.5V
- V_{OUT} = 1V/20A full load
- f_{SW} = 400kHz
- Peak efficiency:
  - 89% at 12A/1V_{OUT}/12V_{IN}
  - 94% at 6A/1.8V_{OUT}/5V_{IN}
- Output regulation: 1V ±8mV
- I/O capacitor rating: C_{IN} - 16V; C_{OUT} - 4V
- Compact size: 17mmx17mm
- With or without PMBus, SMBus, and I^2C Capability

Ordering Information

PART NUMBER	DESCRIPTION
ISL68200DEMO1Z	ISL68200 Demonstration Board (Items shipped: Demonstration board, dongle, USB cable)

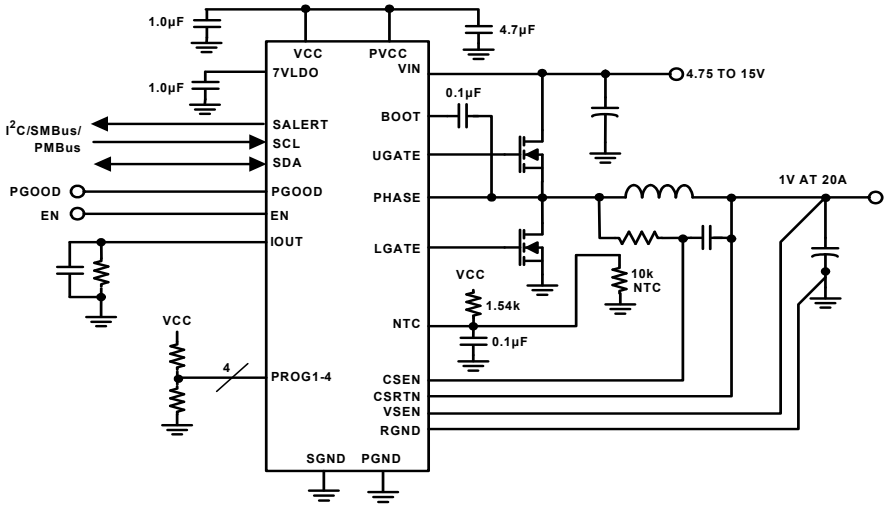

FIGURE 1. ISL68200DEMO1Z SIMPLIFIED SCHEMATIC

FIGURE 2. DEMONSTRATION BOARD TOP VIEW

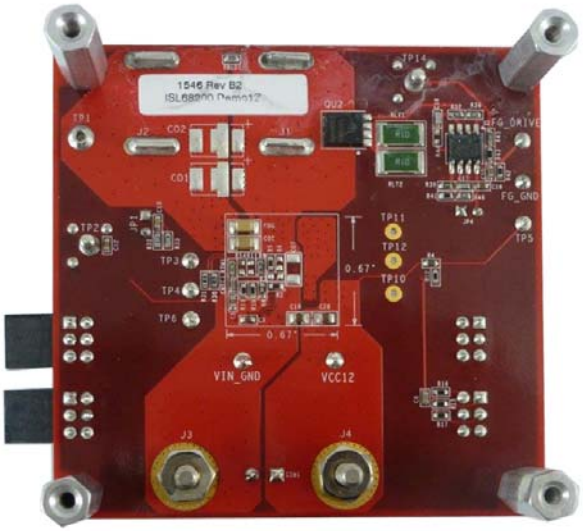

FIGURE 3. DEMONSTRATION BOARD BOTTOM VIEW

Demonstration Board Description

The ISL68200DEMO1Z provides all circuitry required to demonstrate the key features of the ISL68200. A majority of the features of the ISL68200, such as optimal transient response with Intersil's R4 Modulator, 8-bit programmable boot voltage levels, selectable switching frequency in continuous conduction mode, selectable PFM operation option for improved light-load efficiency, power-good monitor for soft-start and fault detection, over-temperature protection, output overcurrent and short-circuit protection, and output overvoltage protection are available on this demonstration board.

Figure 1 shows a simplified schematic diagram of the ISL68200DEMO1Z board. Figure 6 shows the detailed 20A buck solution schematics, while Figure 7 shows the I/O connectors, auxiliary circuits and on-board transient circuits. Figures 8 through 30 show typical performance data and Figures 31 through 36 show the PCB board layout. The default programming pins setting is given on the upper right corner of Figure 7, and the Bill of Materials (BOM) is included for reference beginning on page 9.

The ISL68200DEMO1Z board can run by itself without a serial bus communication. The operational configuration is fully programmable using programming pins (PROG1-4).

The ISL68200 however, uses the PMBus/SMBus/I^2C protocol and provides the flexibility for digital power management and performance optimization before finalizing the hardware configuration on the programming pins.

The buck regulator in the ISL68200DEMO1Z board is a single input rail design, that is, everything is biased by the input supply (typically 12V). The resistor divider on the EN pin (R_4 and R_{12}) can set the input supply undervoltage protection level and its hysteresis. The "ENABLE" switch is a hardware operational control, alternately, the serial bus ON_OFF_CONFIG and OPERATION commands can be used for software operational control.

Furthermore, an on-board transient load, as shown in Figure 7, with both di/dt and load step amplitude is controlled by a function generator. Because this auxiliary circuit draws more than 10A of bias current, the jumper on JP5 should be removed for accurate efficiency measurement.

Intersil's PowerNavigator evaluation software is compatible with Windows operating systems and can be used to evaluate the serial bus functionality of the ISL68200. The software and user guide can be found at: http://www.intersil.com/powernavigator

Quick Start Guide

Stand-Alone Operation

1. Set the ENABLE switch to the "OFF" position.
2. Connect a power supply (off) to input connectors (J4-VIN and J3-GND).
3. Set the input power supply voltage level (no more than 15V) and current limiting (no more than 1A for 0A load).
4. Turn the power supply on.
5. Set the ENABLE switch to the "ON" position.
6. Increase the power supply current limit enough to support more than the full load.
7. Apply load to the output connectors (J1-VOUT and J2-SGND).
8. Monitor operation using an oscilloscope.

PMBus Operation

1. Connect the supplied dongle to J8.
2. Connect the supplied USB cable from the computer to the dongle.
3. After the input power supply turns on, open the PowerNavigator™ evaluation software.
4. Select the detected ISL68200 device (Address - 60h) and follow Intersil's PowerNavigator operation guide.
5. Monitor and configure the board using PMBus commands in the evaluation software.

Configuration

The default programming pins setting of the ISL68200DEMO1Z board can be found at the resistor reader table on the upper right corner of "ISL68200DEMO1Z Schematics" on page 7 or read back using the PowerNavigator software. Each PMBus command can be loaded or programmed through the PowerNavigator software. Note that ISL68200 does not have NVM to store the operational configuration, which can however be set by the resistor programming pins (PROG1-4) or programmed by the serial bus master before powering up. If a serial bus master is available in the system, the ISL68200-based rail can be fully controlled using the software for the power-up/down sequencing and operational configuration without a soldering iron.

Load Transient

The on-board transient load can be controlled by a function generator, whose inputs are connected to FG_DRIVE2 and FG_GND2. The function generator's output is terminated by R42 at the input terminal, while its amplitude and dV/dt set the load amplitude and di/dt on the 50mΩ load ($R_{LT1}//R_{LT2}$). The transient load can be monitored with a scope probe on TP15. Note that the duty cycle of applied load should be less than 10% duty cycle with <10ms pulse width to keep the average power of R_{LT1}/R_{LT2} less than its power rating.

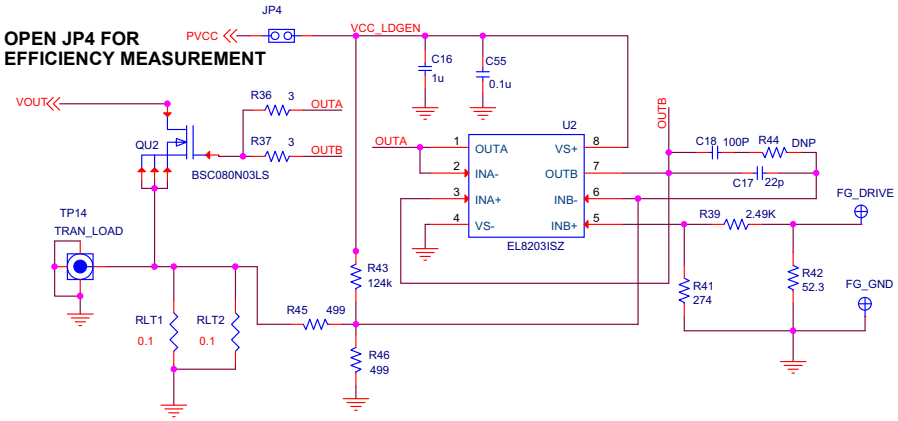

FIGURE 4. LOAD TRANSIENT

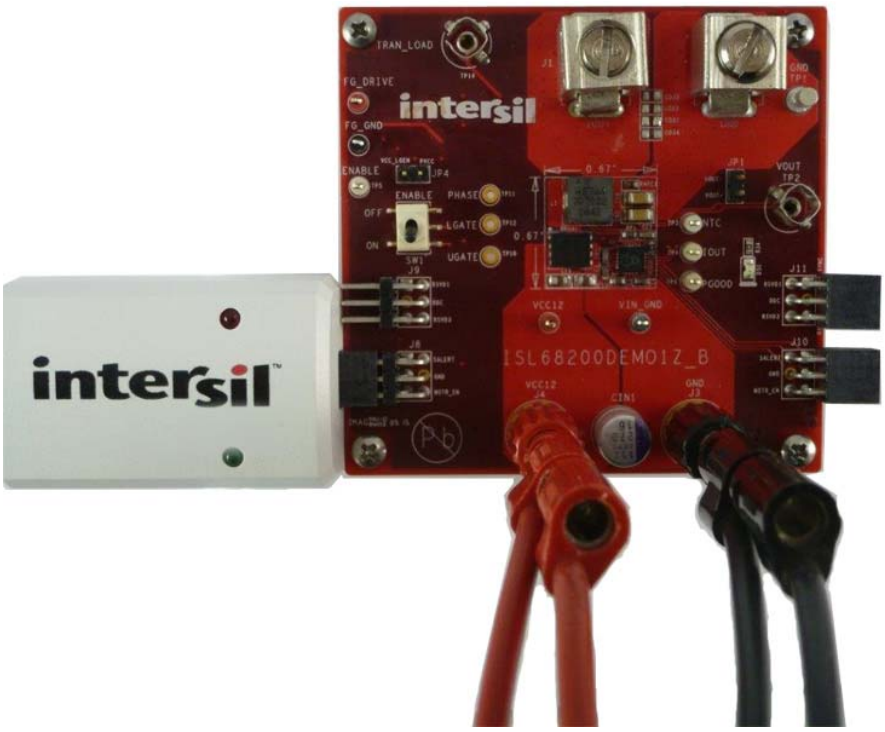

FIGURE 5. ISL68200 DEMONSTRATION BOARD SETUP

Design Modifications

Any modifications to the design will require new L/DCR matching for a different inductor, a divider on the PROG pins for a different operational configuration, RSEN1 for OCP, and an IOUT network for accurate digital IOUT, a higher input capacitor rating to support higher than 16V input, and a higher output capacitor rating to support higher than 4V output. Refer to the ISL68200 datasheet and PowerNavigator software for proper design modifications including L/DCR matching, thermal compensation, OCP, and digital I_{OUT} fine-tuning.

Two examples are provided in Table 1, showing the recommended design modifications to accommodate the application cases with 5V and 3.3V output voltages. Some fine-tuning might be needed depending upon the rework and final layout design.

For the 5V input voltage applications with $4.5V < V_{IN} < 5.5V$ requirement, the VIN, VCC, PVCC, and 7VLDO pins should be shorted together, to connect with the input supply for optimal performance; R_{12} should be removed as well.

Note that all devices in the same bus should set different addresses for unique identification and proper communication. JP2, JP3, JP9, and JP10 connectors are designed to cascade many Intesil's solutions for easy communication and system evaluation before the system integration and design.

TABLE 1. DESIGN EXAMPLES

REFERENCE DESIGNATOR	5.0V AT 16A	3.3V AT 16A	3.3V AT 30A	COMMENTS
L1	680nH, 1.72mΩ Vendor: Wurth Electronic; Part Number: 744334006		470nH, 0.165mΩ Vendor: Wurth Electronic; Part Number: 744309047	Reduce Output ripple current; typically higher voltage output needs higher inductance.
CO5, CO6, CO8, CO9	100µF/X5R/6.3V/1206 Vendor: Murata; Part Number: GRM21BR60J107ME11			Increase C_{OUT} rating to support higher V_{OUT}. Also capacitance of ceramic capacitors decreases with increased output voltage.
PROG1 (DC)	DFh	BFh	BFh	Set correct $V_{BOOT} = V_{OUT}$
R_3	147k, 1%	105k, 1%	105k, 1%	
PROG2 (DD)	A0h	BFh	BFh	Set Different PMBus Addresses as needed T_{COMP} = 15 PFM DISABLED
R_5	105k, 1%	DNP	DNP	
R_6	DNP	105k, 1%	105k, 1%	
PROG3 (DE)	0Dh	0Dh	0Dh	Set AV = 13 f_{SW} = 500kHz OCP = Retry 25kHz Clamp Disabled
R_8	24.3k, 1%	24.3k, 1%	24.3k, 1%	
R_9	16.9k, 1%	16.9k, 1%	16.9k, 1%	
PROG4 (DF)	08h	08h	08h	Set RR = 400k SS = 1.25mV/µs AVMLTI = 1 x
R_{10}	15k, 1%	15k, 1%	15k, 1%	
R_{11}	29.4k, 1%	29.4k, 1%	29.4k, 1%	
R_{P1}	4.99k, 1%	4.99k, 1%	3.57k, 1%	L/DCR Matching
R_{SEN1}	536, 1%	536, 1%	62, 1%	Set OCP
R_{13}	11k, 1%	11k, 1%	15k, 1%	Set I_{OUT} to 1A/1A Slope
R_{14}	TBD	TBD	TBD	Pull-up value depends upon final layout design

NOTE:

1. Some fine-tuning might be needed depending upon the rework and final layout design.

Design and Layout Considerations

To ensure a first pass design, the schematics design must be done correctly and the board must be carefully laid out.

As a general rule, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board or internal layers. The ground-plane layer should be in between the power layers and the signal layers to provide shielding, often the layer below the top and the layer above the bottom should be the ground layers.

There are two sets of components in a DC/DC converter, the power components and the small signal components. The power components are the most critical because they switch large amount of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first and these include MOSFETs, input and output capacitors, and the inductor. Keeping the distance between the power train and the control IC short helps keep the gate drive traces short. These drive signals include the LGATE, UGATE, GND, PHASE, and BOOT.

When placing MOSFETs, try to keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as thermally possible. Input high frequency capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. High frequency output decoupling capacitors (ceramic) should be placed as close as possible to the decoupling target, making use of the shortest connection paths to any internal planes. Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals, phase node signals, and the VIN plane.

Tables 2 and 3 provide design and layout checklist that the designer must pay attention to.

TABLE 2. DESIGN AND LAYOUT CHECKLIST

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
EN	Yes	There is an internal 1µs filter. Decoupling the capacitor is NOT needed, but if needed, use a low time constant one to avoid too large a shutdown delay.
VIN	Yes	Place 16V+ X7R 1µF in close proximity to the VIN pin and the system ground plane.
7VLDO	Yes	Place 10V+ X7R 1µF in close proximity to the 7VLDO pin and the system ground plane.
VCC	Yes	Place X7R 1µF in close proximity to the VCC pin and the system ground plane.

TABLE 2. DESIGN AND LAYOUT CHECKLIST (Continued)

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
SCL, SDA	Yes	50kHz to 1.25MHz signal when the SMBus, PMBus, or I^2C is sending commands. Pairing up with SALERT and routing carefully back to SMBus, PMBus, or I^2C master. 20 mils spacing within SDA, SALERT, and SCL; and more than 30 mils to all other signals. Refer to the SMBus, PMBus, or I^2C design guidelines and place proper terminated (pull-up) resistance for impedance matching. Tie them to GND when not used.
SALERT	No	Open-drain and high dv/dt pin during transitions. Route it in the middle of SDA and SCL. Tie it to GND when not used.
PGOOD	No	Open-drain pin. Tie it to ground when not used.
RGND, VSEN	Yes	Differential pair routed to the remote sensing points with sufficient decoupling ceramics capacitors and not across or go above/under any switching nodes (BOOT, PHASE, UGATE, LGATE) or planes (VIN, PHASE, VOUT) even though they are not in the same layer. At least 20 mils spacing from other traces. DO NOT share the same trace with CSRTN.
CSRTN	Yes	Connect to the output rail side of the output inductor or current sensing resistor pin with a series resistor in close proximity to the pin. The series resistor sets the current gain and should be within 40Ω and 3.5kΩ. Decoupling (~0.1µF/X7R) on the output end (not the pin) is optional and might be required for long sense trace and a poor layout.
CSEN	Yes	Connect to the phase node side of the output inductor or current sensing resistor pin with L/DCR or ESL/R_{SEN} matching network in close proximity to the CSEN and CSRTN pins. Differentially routing back to the controller with at least 20 mils spacing from other traces. Should NOT cross or go above/under the switching nodes [BOOT, PHASE, UGATE, LGATE] and power planes (VIN, PHASE, VOUT) even though they are not in the same layer.
NTC	Yes	Place NTC 10k (Murata, NCP15XH103J03RC, β = 3380) in close proximity to the output inductor's output rail, not close to MOSFET side; the return trace should be 20 mils away from other traces. Place 1.54kΩ pull-up and decoupling capacitor (typically 0.1µF) in close proximity to the controller. The pull-up resistor should be exactly tied to the same point as the VCC pin, not through an RC filter. If not used, connect this pin to VCC.
IOUT	Yes	Scale R such that the IOUT pin voltage is 2.5V at 63.875A load. Place R and C in general proximity to the controller. The time constant of RC should be sufficient as an averaging function for the digital IOUT. An external pull-up resistor to VCC is recommended to cancel the IOUT offset at 0A load.

TABLE 2. DESIGN AND LAYOUT CHECKLIST (Continued)

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
PROG1-4	No	Resistor divider must be referenced to the VCC pin and the system ground; they can be placed anywhere. DO NOT use decoupling capacitors on these pins.
GND	Yes	Directly connect to low noise area of the system ground. The GND PAD should use at least four vias. Separate analog ground and power ground with a 0Ω resistor is highly NOT recommended.
LGATE	No	Low-side driver output and short and wide trace in between this pin and the MOSFET gate pin as possible. High dV/dt signals should not be close to any sensitive signals.
UGATE	No	High-side driver output and short and wide trace in between this pin and the MOSFET gate pin as possible. High dV/dt signals should not be close to any sensitive signals.
BOOT, PHASE	Yes	Place X7R 0.1µF or 0.22µF in proximity to the BOOT and PHASE pins. High dV/dt signals should not be close to any sensitive signals.
PVCC	Yes	Place X7R 4.7µF in proximity to the PVCC pin and the system ground plane.

TABLE 3. TOP LAYOUT TIPS

NUMBER	DESCRIPTION
1	The layer next to controller (top or bottom) should be a ground layer. Separate analog ground and power ground with a 0Ω resistor is highly NOT recommended. Directly connect GND PAD to low noise area of the system ground with at least four vias.
2	Never place controller and its external components above or under the VIN plane or any switching nodes.
3	Never share CSRTN and VSEN on the same trace.
4	Place the input rail decoupling ceramic capacitors closely to the high-side FET. Never use only one via and a trace to connect the input rail decoupling ceramics capacitors; must connect to the VIN and GND planes.
5	Place all decoupling capacitors in close proximity to the controller and the system ground plane.
6	Connect remote sense (VSEN and RGND) to the load and ceramic decoupling capacitors nodes; never run this pair below or above switching noise plane.
7	Always double check critical component pinout and their respective footprints.

ISL68200DEMO1Z Schematics

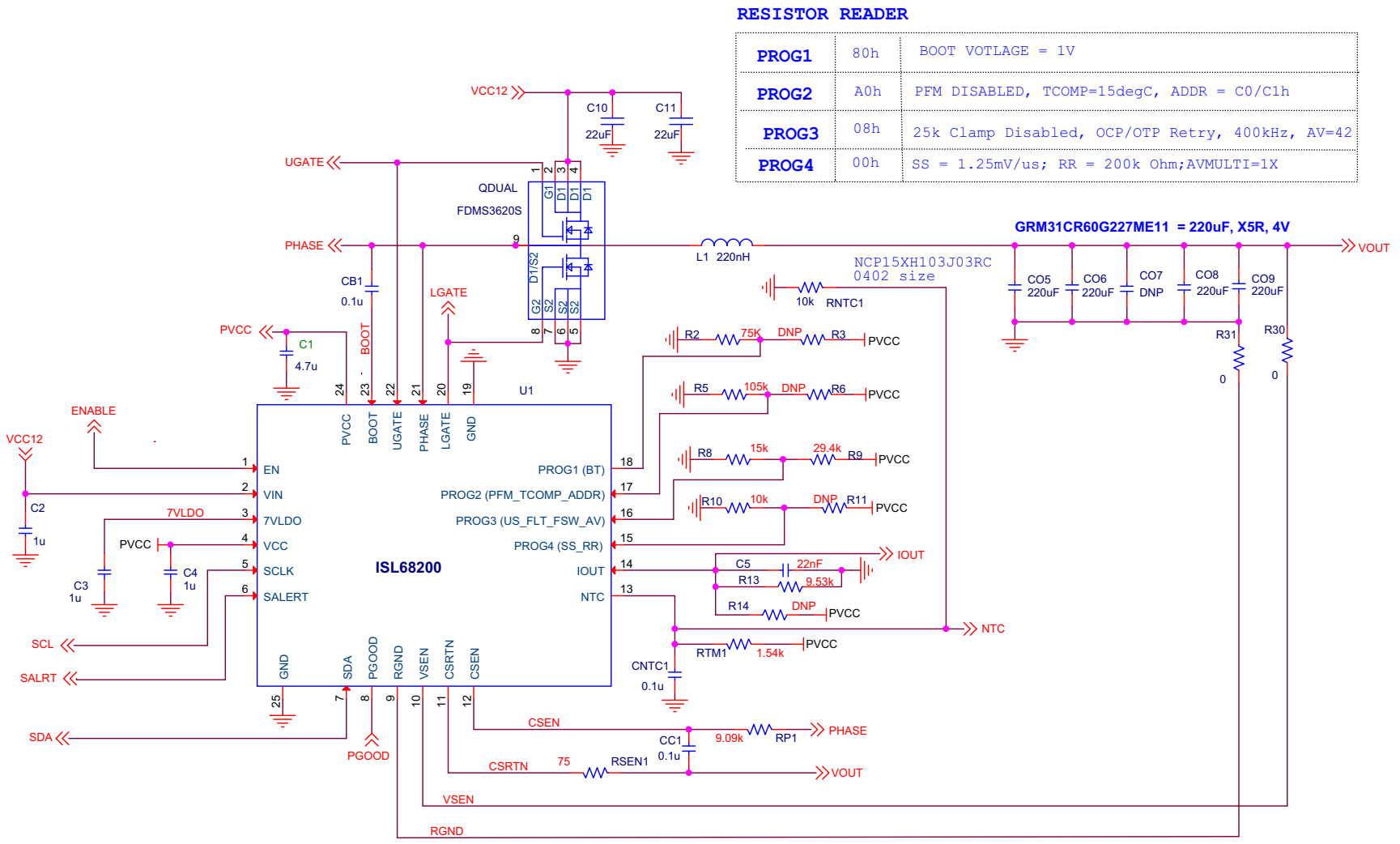

FIGURE 6. ISL68200DEMO1Z 1V AT 20A BUCK SOLUTION SCHEMATICS

ISL68200DEMO1Z Schematics (Continued)

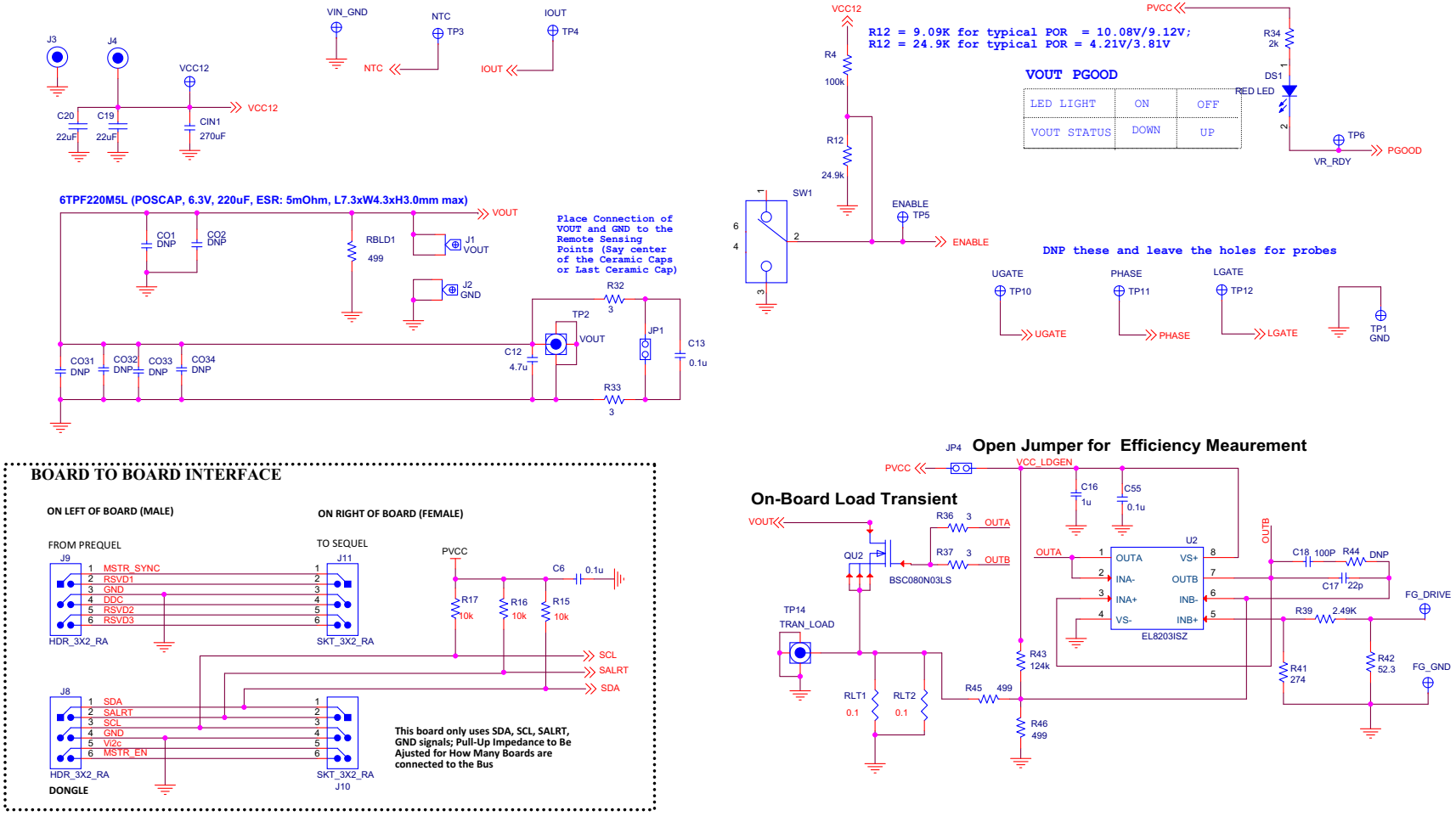

FIGURE 7. I/O CONNECTORS, AUXILIARY CIRCUITS AND ON-BOARD TRANSIENT LOAD SCHEMATICS

Bill of Materials

QTY	REFERENCE DESIGNATOR	DESCRIPTION	PCB FOOTPRINT	MANUFACTURER	PART NUMBER
1	U1	R4 Wrapper with Driver	QFN24_157X157_197_EPC	INTERSIL	ISL68200IRZ-REVD
1	CIN1	270µF/16V/8x9/10mΩ	CAPR_315X275_150_P	SANYO	16SEPC270MX
1	C1	4.7µF/6.3V/X5R	SM0603	VENKEL	C0603X5R6R3-475KNE
2	C2, C3	1.0µF/16V/X7R	SM0603	TDK	C1608X7R1C105K
1	C4	1µF/6.3V/X5R	SM0603	PANASONIC	ECJ1VB0J105K
1	C5	22nF/50V/X7R	SM0603	VENKEL	C0603X7R500-223KNE
4	C6, CB1, CC1, CNTC1	0.1µF/16V/X7R	SM0603	MURATA	GRM39X7R104K016AD
4	C10, C11, C19, C20	22µF/16V/X5R	SM0805	VENKEL	C0805X5R160-226KNE
4	CO5, CO6, CO8, CO9	220µF/4V/X5R	SM1206	MURATA	GRM31CR60G227ME11
1	L1	220nH, 0.29mΩ	ind_we_744302010	Wurth Electronics	744307022
1	QDUAL	Dual FET	pqfn_5x6_dual	INFINEON	BSC0910NDI
1	R2	75kΩ, 1%	SM0603	VENKEL	CR0603-10W-7502FT
1	R4	100kΩ, 1%	SM0603	VENKEL	CR0603-10W-1003FT
1	R5	105kΩ, 1%	SM0603	PANASONIC	ERJ-3EKF1053V
1	R8	15kΩ, 1%	SM0603	PANASONIC	ERJ-3EKF1502V
1	R9	29.4kΩ, 1%	SM0603	YAGEO	RC0603FR-0729K4L
4	R10, R15, R16, R17	10kΩ, 1%	SM0603	VENKEL	CR0603-10W-1002FT
1	R12	24.9kΩ, 1%	SM0603	PANASONIC	ERJ-3EKF2492V
1	R13	9.53kΩ, 1%	SM0603	YAGEO	9C06031A9531FKHFT
2	R30, R31	0Ω	SM0603	VENKEL	CR0603-10W-000T
1	RBLD1	121Ω, 1%	SM0603	VISHAY/DALE	CRCW0603121RFKTA
1	RNTC1	10kΩ NTC, 5%, β = 3380	SM0402	MURATA	NCP15XH103J03RC
1	RP1	9.09kΩ, 1%	SM0603	YAGEO	RC0603FR-079K09L
1	RSEN1	75Ω, 1%	SM0603	PANASONIC	ERJ-3EKF75R0V
1	RTM1	1.54kΩ, 1%	SM0603	YAGEO	RC0603FR-071K54L
DEMONSTRATION BOARD SPECIFIC AUXILIARY PARTS BILL OF MATERIALS					
1	U2	Dual Amp/500MHz/5V	SOIC8	INTERSIL	EL8203ISZ
1	QU2	8mΩ N-MOSFET	LFPAK	INFINEON	BSC080N03LS G
1	DS1	LED/RED/0805/CLEAR	SM0805	WURTH ELEKTRONIK	150080RS75000
1	SW1	Enable Switch	GT11SC	C&K DIVISION	GT11MSCBE
1	C12	4.7µF/6.3V/X5R	SM0603	VENKEL	C0603X5R6R3-475KNE
2	C13, C55	0.1µF/16V/X7R	SM0603	MURATA	GRM39X7R104K016AD
1	C16	1µF/6.3V/X5R	SM0603	PANASONIC	ECJ1VB0J105K
1	C17	22pF/50V/C0G	SM0603	VENKEL	C0603C0G500-220JNE
1	C18	100pF/50V/C0G	SM0603	PANASONIC	ECJ-1VC1H101J
2	J1, J2	Screw Terminal	B2C-PCB	INTERNATIONAL HYDRAULICS INC	B2C-PCB
1	J3	Female Banana Jack, Black	111-07xx-001	JOHNSON COMPONENTS	111-0703-001

Bill of Materials (Continued)

QTY	REFERENCE DESIGNATOR	DESCRIPTION	PCB FOOTPRINT	MANUFACTURER	PART NUMBER
1	J4	Female Banana Jack, Red	111-07xx-001	JOHNSON COMPONENTS	111-0702-001
2	J8, J9	CONN-HEADER, 2X3, BRKAWY, 2.54mm,TIN	CONN6	SAMTEC	TSW-103-08-T-D-RA
2	J10, J11	CONN-SOCKET STRIP,TH,2X3, 2.54mm,TIN	CONN6	SAMTEC	SSQ-103-02-T-D-RA
2	JP1, JP4	2-pin 0.1" spacing Jumper	CONN2	BERG/FCI	69190-202HLF
1	TP1	Probe Ground	TP-150C100P-RTP	KEYSTONE	1514-2
2	TP2, TP14	Probe Jack	TEK131-4353-00	TEKTRONIX	131-4353-00
4	TP3, TP4, TP5, TP6	Test Point	MTP500x	KEYSTONE	5002
2	VCC12, FG_DRIVE	Test Point RED	MTP500x	KEYSTONE	5000
2	VIN_GND, FG_GND	Test Point BLACK	MTP500x	KEYSTONE	5001
4	R32, R33, R36, R37	3Ω, 1%	SM0603	VENKEL	CR0603-10W-03R0FT
1	R34	2kΩ, 1%	SM0603	KOA	RK73H1JTTD2001F
1	R39	2.49kΩ, 1%	SM0603	KOA	RK73H1JTTD2491F
1	R42	52.3Ω, 1%	SM0603	PANASONIC	ERJ-3EKF52R3V
1	R41	274Ω, 1%	SM0603	VENKEL	CR0603-10W-2740FT
1	R43	124kΩ, 1%	SM0603	YAGEO	9C06031A1243FKHFT
2	R45, R46	499Ω, 1%	SM0603	VENKEL	CR0603-10W-4990FT
2	RLT1, RLT2	0.1Ω, 1%	SM2512	CTS RESISTOR	73L7R10J

Measured Data

The following data was acquired using a ISL68200DEMO1Z board.

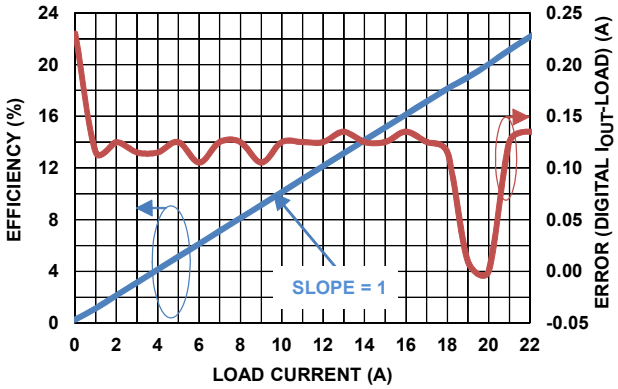

FIGURE 8. TYPICAL DIGITAL OUTPUT CURRENT MEASUREMENT

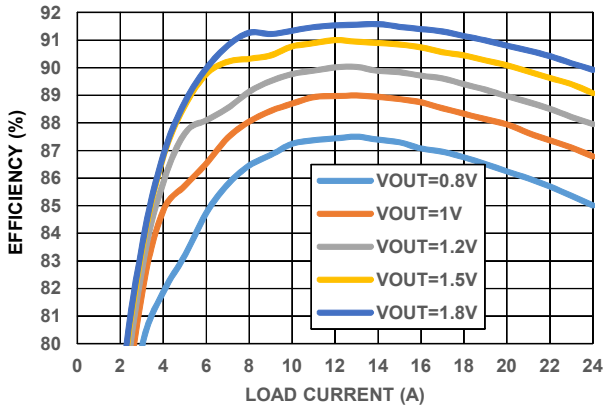

FIGURE 9. EFFICIENCY, V_{IN} = 12V, f_{SW} = 400kHz

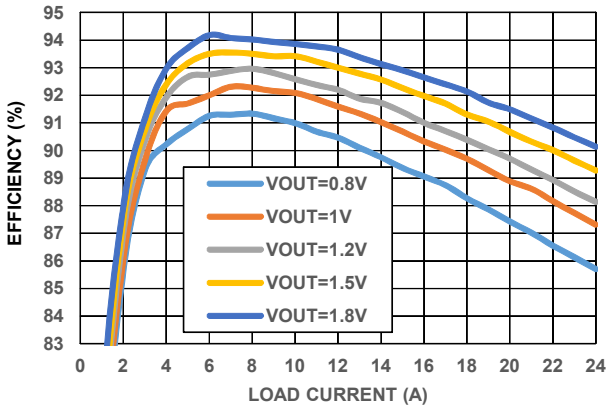

FIGURE 10. EFFICIENCY, V_{IN} = 5V, f_{SW} = 400kHz

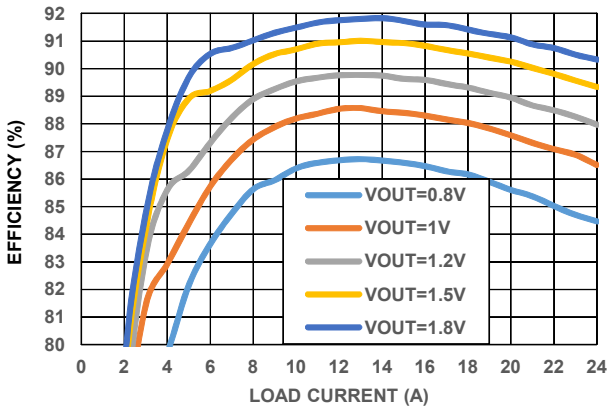

FIGURE 11. EFFICIENCY, V_{IN} = 12V, f_{SW} = 500kHz

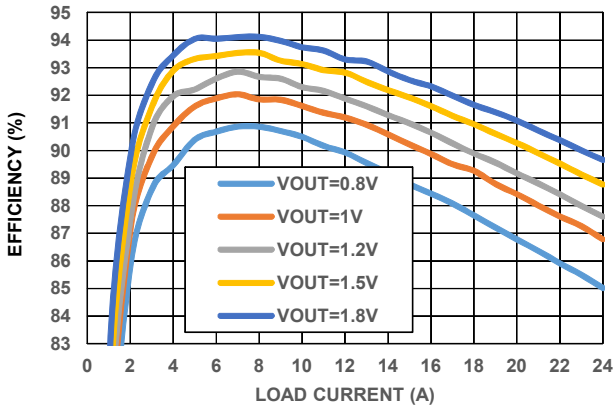

FIGURE 12. EFFICIENCY, V_{IN} = 5V, f_{SW} = 500kHz

Measured Data The following data was acquired using a ISL68200DEMO1Z board. (Continued)

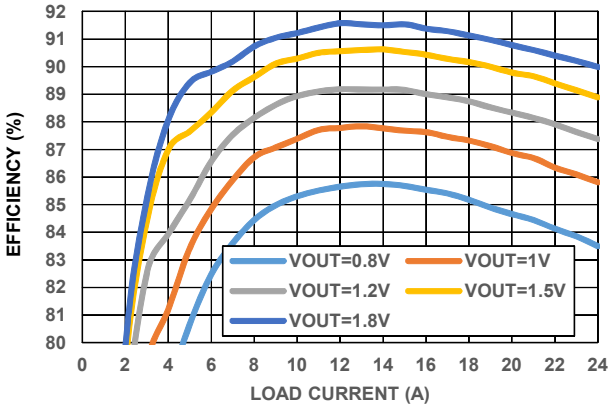

FIGURE 13. EFFICIENCY, V_{IN} = 12V, f_{SW} = 600kHz

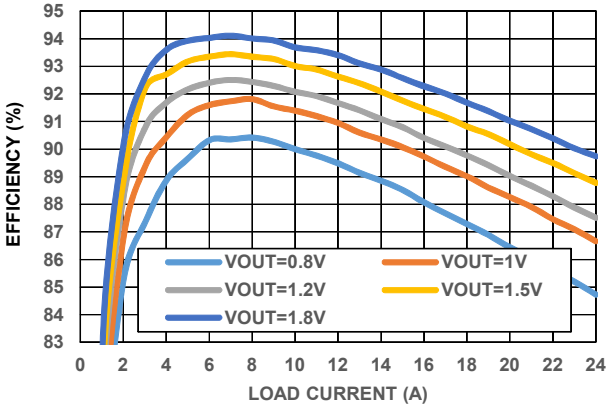

FIGURE 14. EFFICIENCY, V_{IN} = 5V, f_{SW} = 600kHz

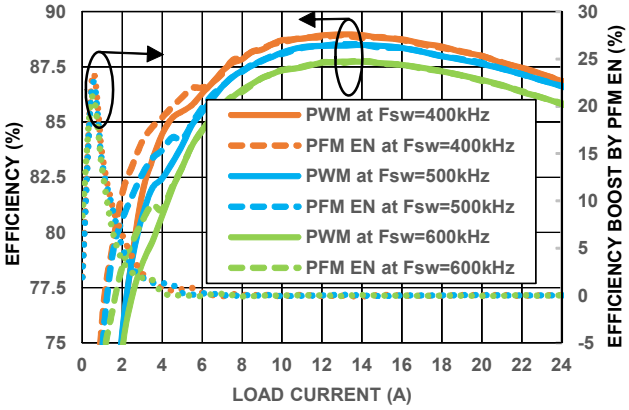

FIGURE 15. EFFICIENCY COMPARISON OF PWM MODE AND PFM ENABLED MODE, V_{IN} = 12V, V_{OUT} = 1V

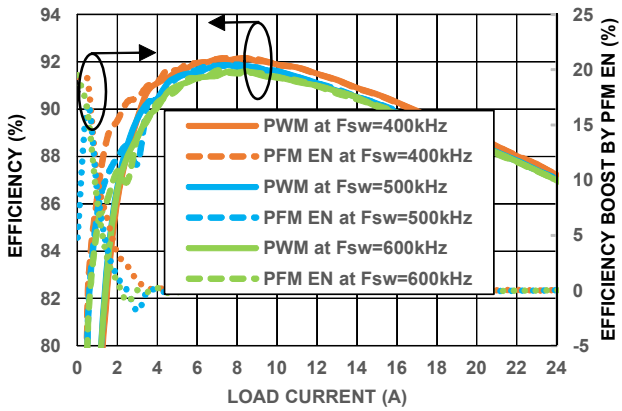

FIGURE 16. EFFICIENCY COMPARISON OF PWM MODE AND PFM ENABLED MODE, V_{IN} = 5V, V_{OUT} = 1V

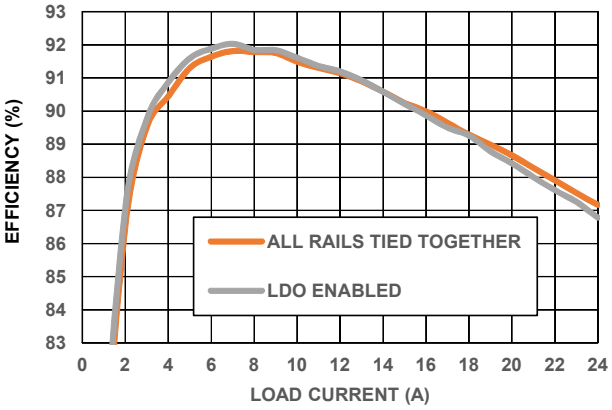

FIGURE 17. EFFICIENCY COMPARISON OF LDO ENABLED AND BYPASSED, V_{IN} = 5V, V_{OUT} = 1V, f_{SW} = 500kHz

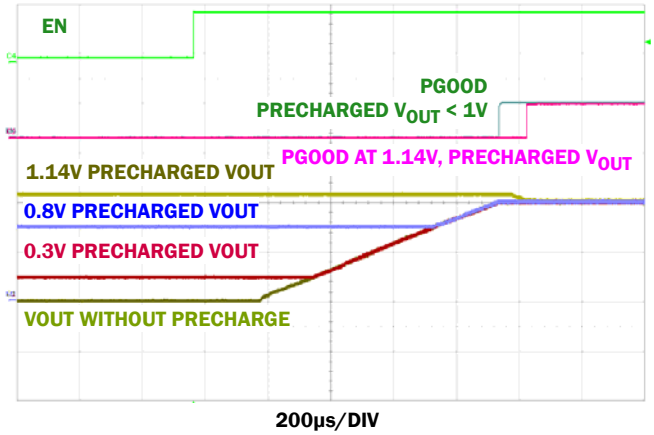

FIGURE 18. POWER-UP WITH/WITHOUT PRECHARGE AT 1A LOAD

Measured Data The following data was acquired using a ISL68200DEMO1Z board. (Continued)

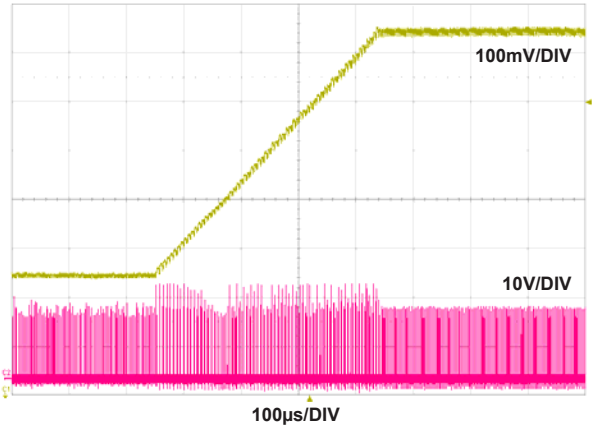

FIGURE 19. V_{OUT} RAMP-UP FROM 0.5V TO 1V IN PWM MODE (CH1-V_{OUT}, CH2-PHASE)

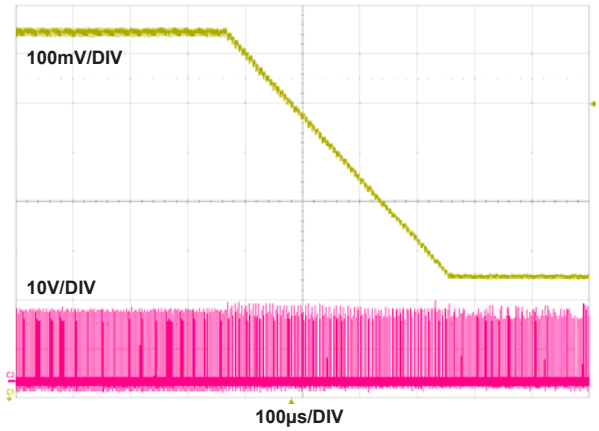

FIGURE 20. V_{OUT} RAMP-DOWN FROM 1V TO 0.5V IN PWM MODE (CH1-V_{OUT}, CH2-PHASE)

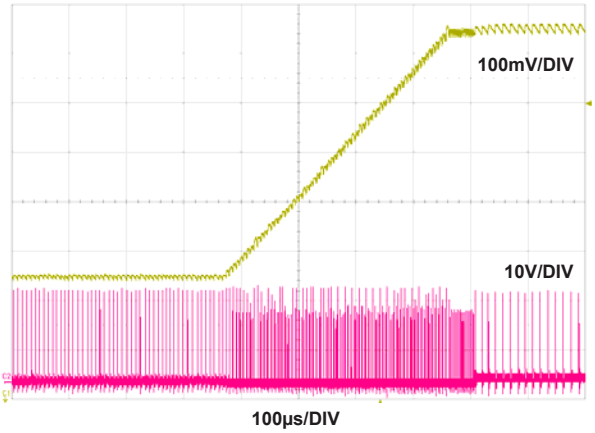

FIGURE 21. V_{OUT} RAMP-UP FROM 0.5V TO 1V IN PFM MODE (CH1-V_{OUT}, CH2-PHASE)

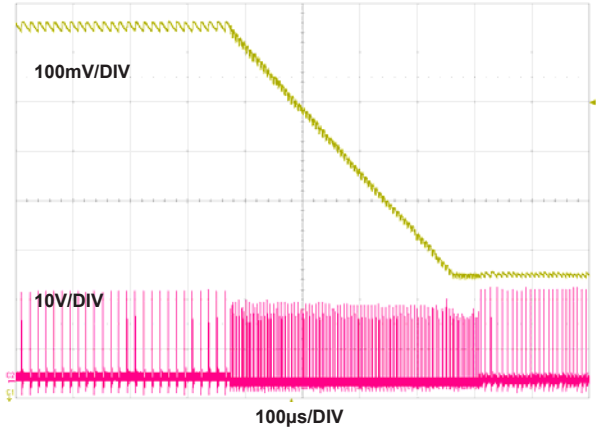

FIGURE 22. V_{OUT} RAMP-DOWN FROM 1V TO 0.5V IN PFM MODE (CH1-V_{OUT}, CH2-PHASE)

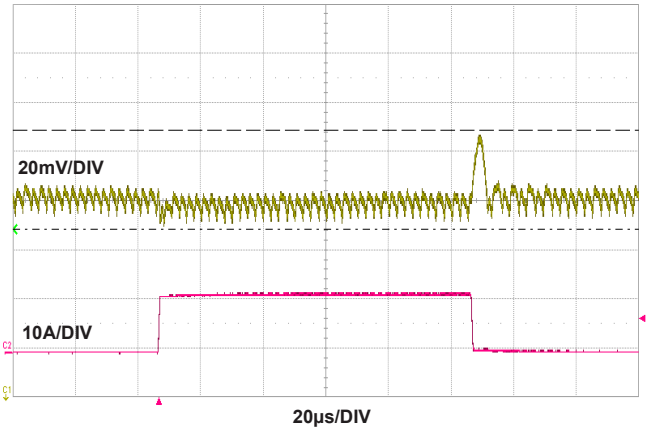

FIGURE 23. STEP RESPONSE AT PWM MODE, V_{OUT} = 1V, f_{SW} = 400kHz, LOAD PROFILE: 0.25A TO 12.75A AT 25A/µs (CH1-VOUT, CH2-LOAD)

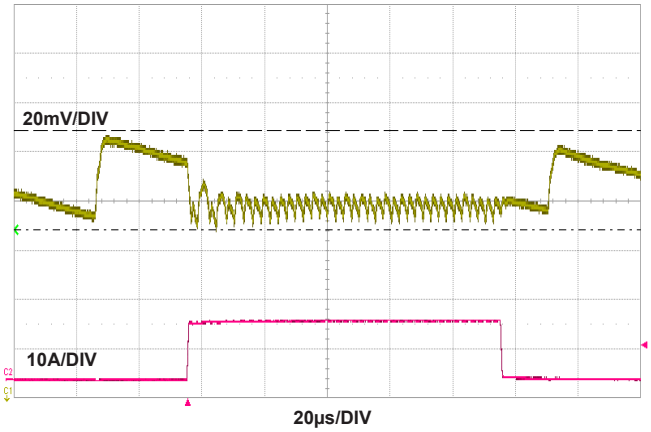

FIGURE 24. STEP RESPONSE AT PFM ENABLED MODE, V_{OUT} = 1V, f_{SW} = 400kHz, LOAD PROFILE: 0.25A TO 12.75A AT 25A/µs (CH1-VOUT, CH2-LOAD)

Measured Data The following data was acquired using a ISL68200DEMO1Z board. (Continued)

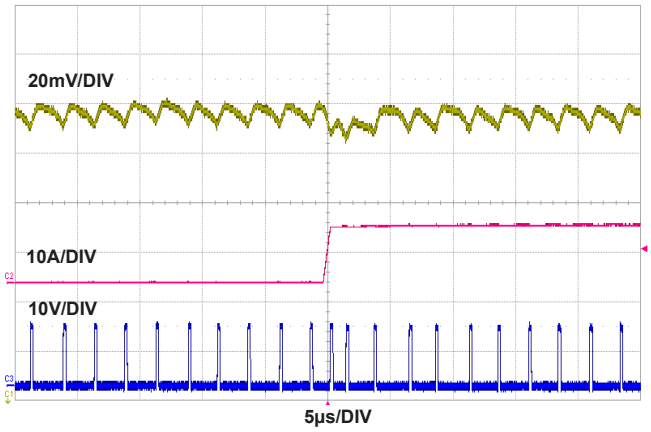

FIGURE 25. STEP RESPONSE TO LOAD STEP AT PWM MODE, V_{OUT} = 1V, f_{SW} = 400kHz, LOAD PROFILE: 0.25A TO 12.75A AT 25A/µs (CH1-V_{OUT}, CH2-LOAD, CH3-PHASE)

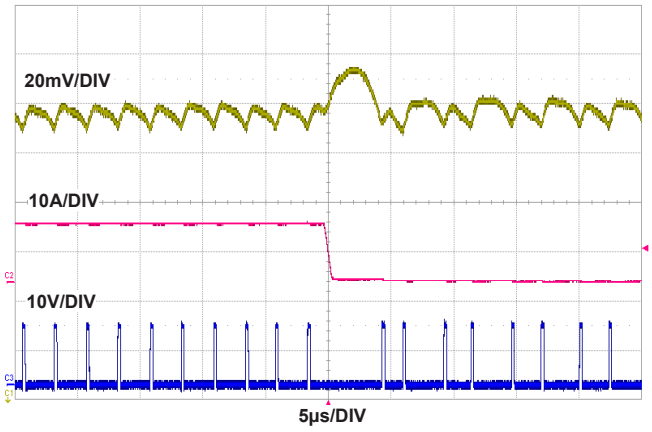

FIGURE 26. STEP RESPONSE TO LOAD RELEASE AT PWM MODE, V_{OUT} = 1V, f_{SW} = 400kHz, LOAD PROFILE: 0.25A TO 12.75A AT 25A/µs (CH1-V_{OUT}, CH2-LOAD, CH3-PHASE)

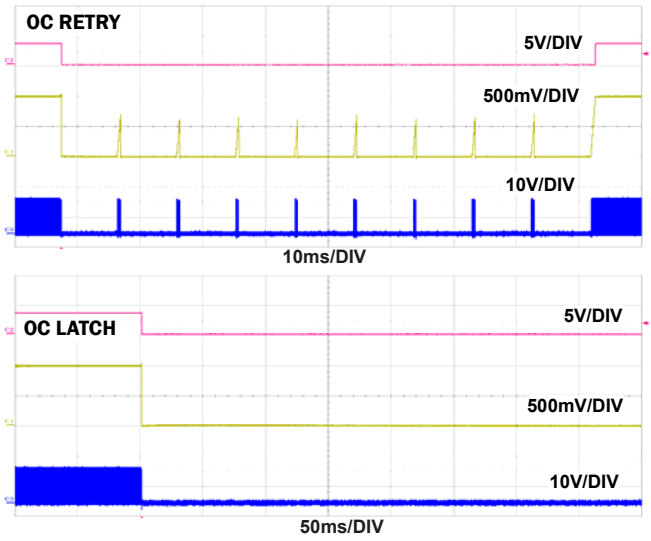

FIGURE 27. OVERCURRENT PROTECTION (CH1-V_{OUT}, CH2-PGOOD, CH3-PHASE)

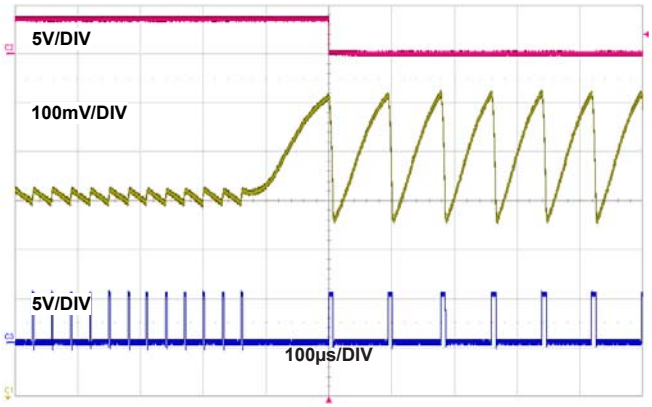

FIGURE 28. OVERVOLTAGE PROTECTION (CH1-V_{OUT}, CH2-PGOOD, CH3-LGATE)

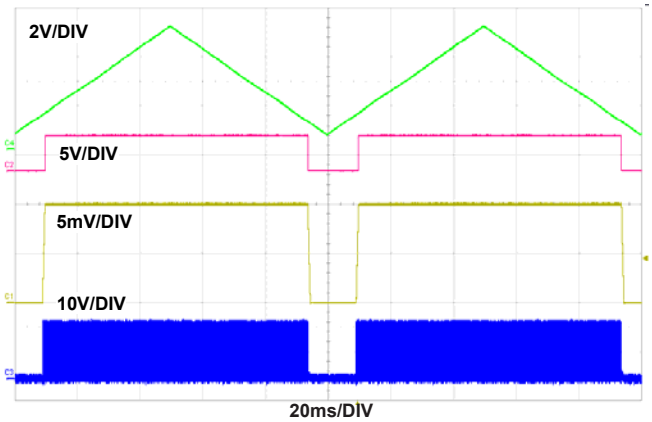

FIGURE 29. OVER-TEMPERATURE PROTECTION AT 1A LOAD (CH1-V_{OUT}, CH2-LOAD, CH3-PHASE, CH4-NTC)

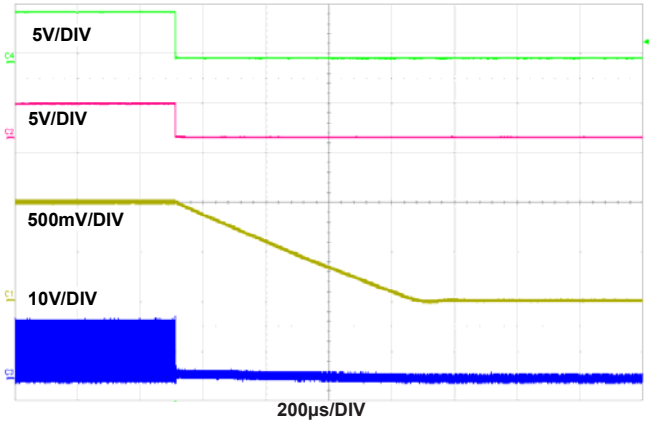

FIGURE 30. POWER-DOWN AT V_{OUT} = 1V, 1A LOAD (CH1-V_{OUT}, CH2-PGOOD, CH3-PHASE, CH4-EN)

ISL68200DEMO1Z Board Layout

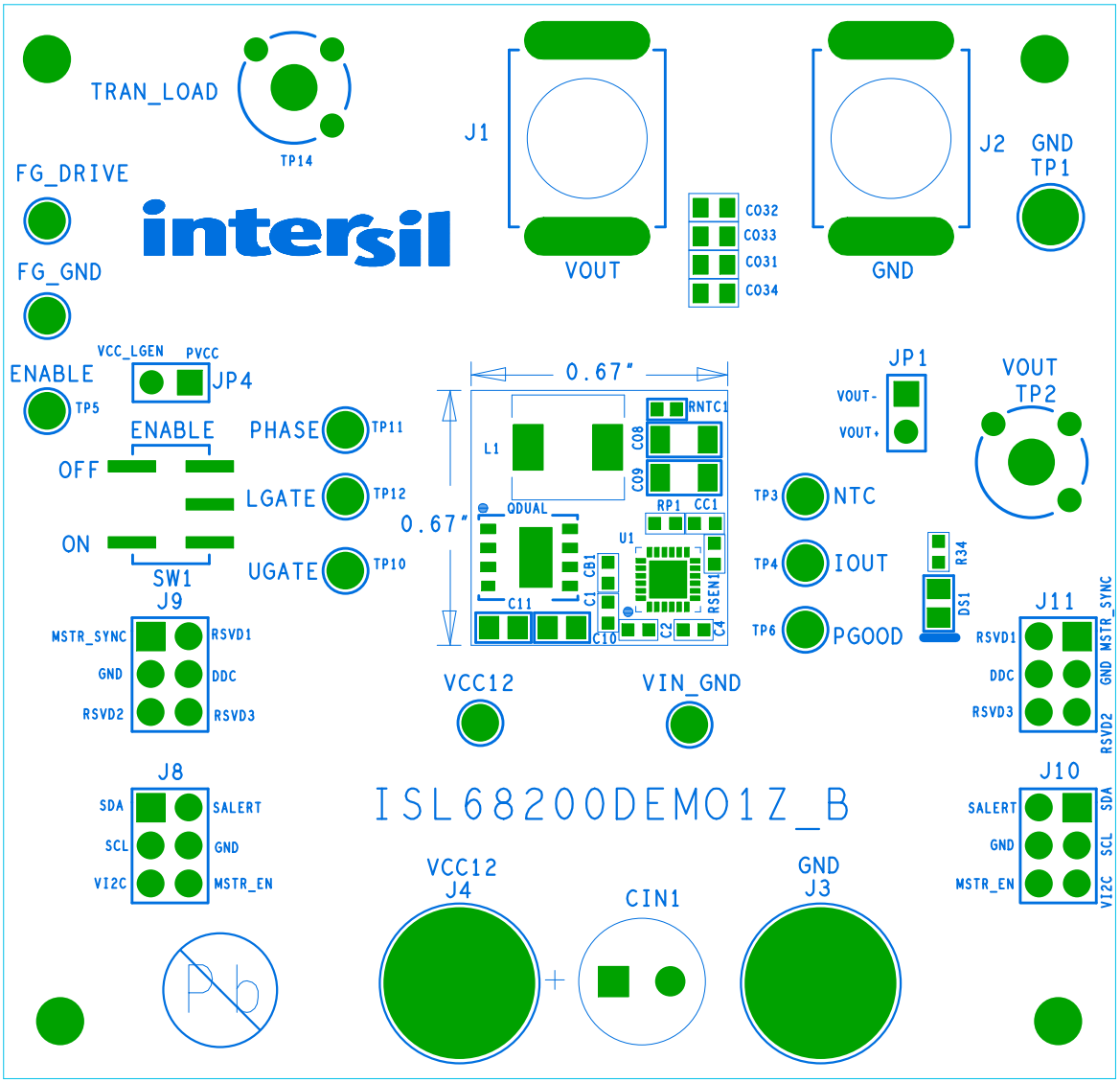

FIGURE 31. PCB - TOP ASSEMBLY

ISL68200DEMO1Z Board Layout (Continued)

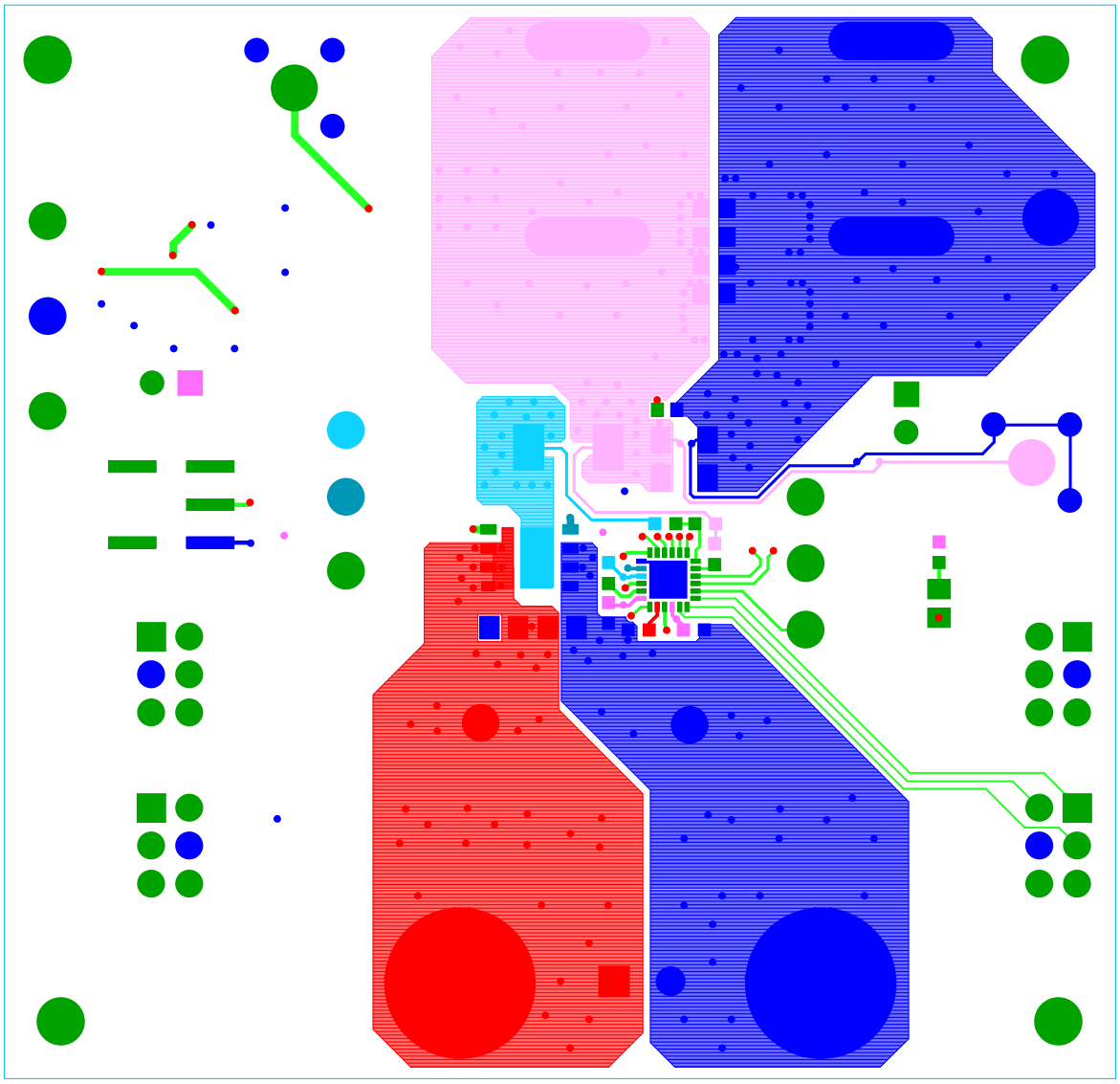

FIGURE 32. PCB - TOP LAYER

ISL68200DEMO1Z Board Layout (Continued)

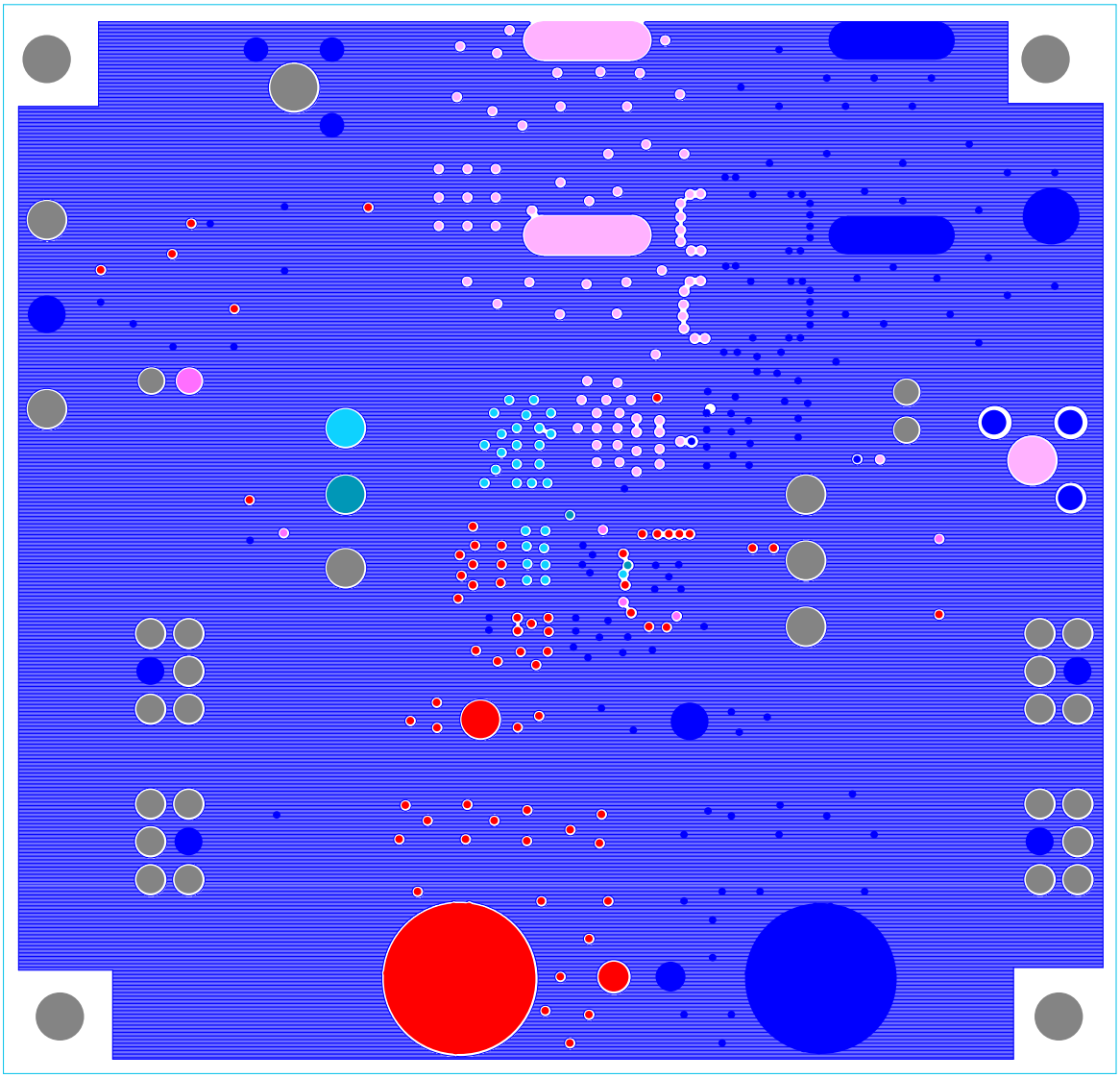

FIGURE 33. PCB - INNER LAYER 2 (TOP VIEW)

ISL68200DEMO1Z Board Layout (Continued)

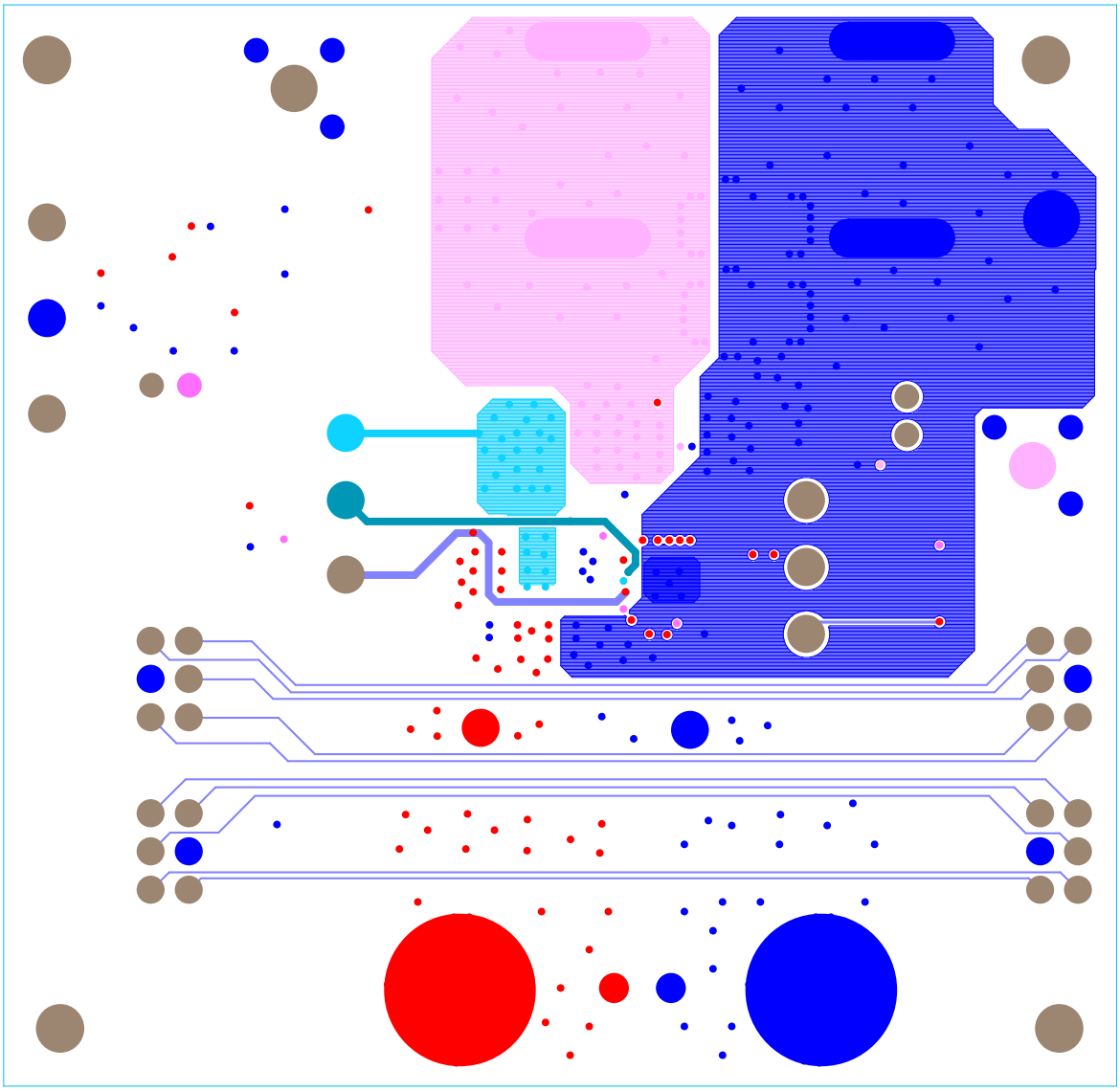

FIGURE 34. PCB - INNER LAYER 3 (TOP VIEW)

ISL68200DEMO1Z Board Layout (Continued)

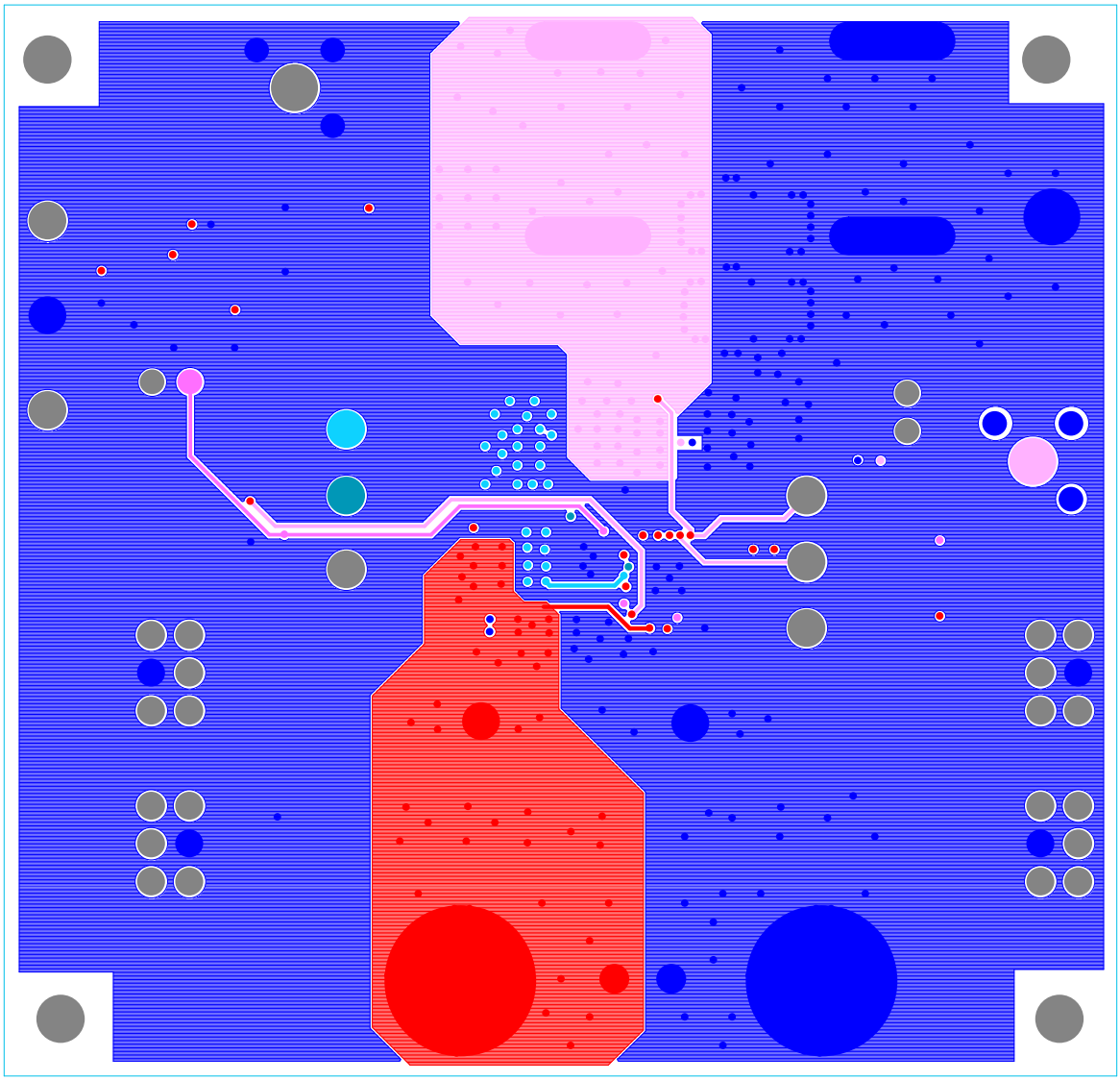

FIGURE 35. PCB - INNER LAYER 4 (TOP VIEW)

ISL68200DEMO1Z Board Layout (Continued)

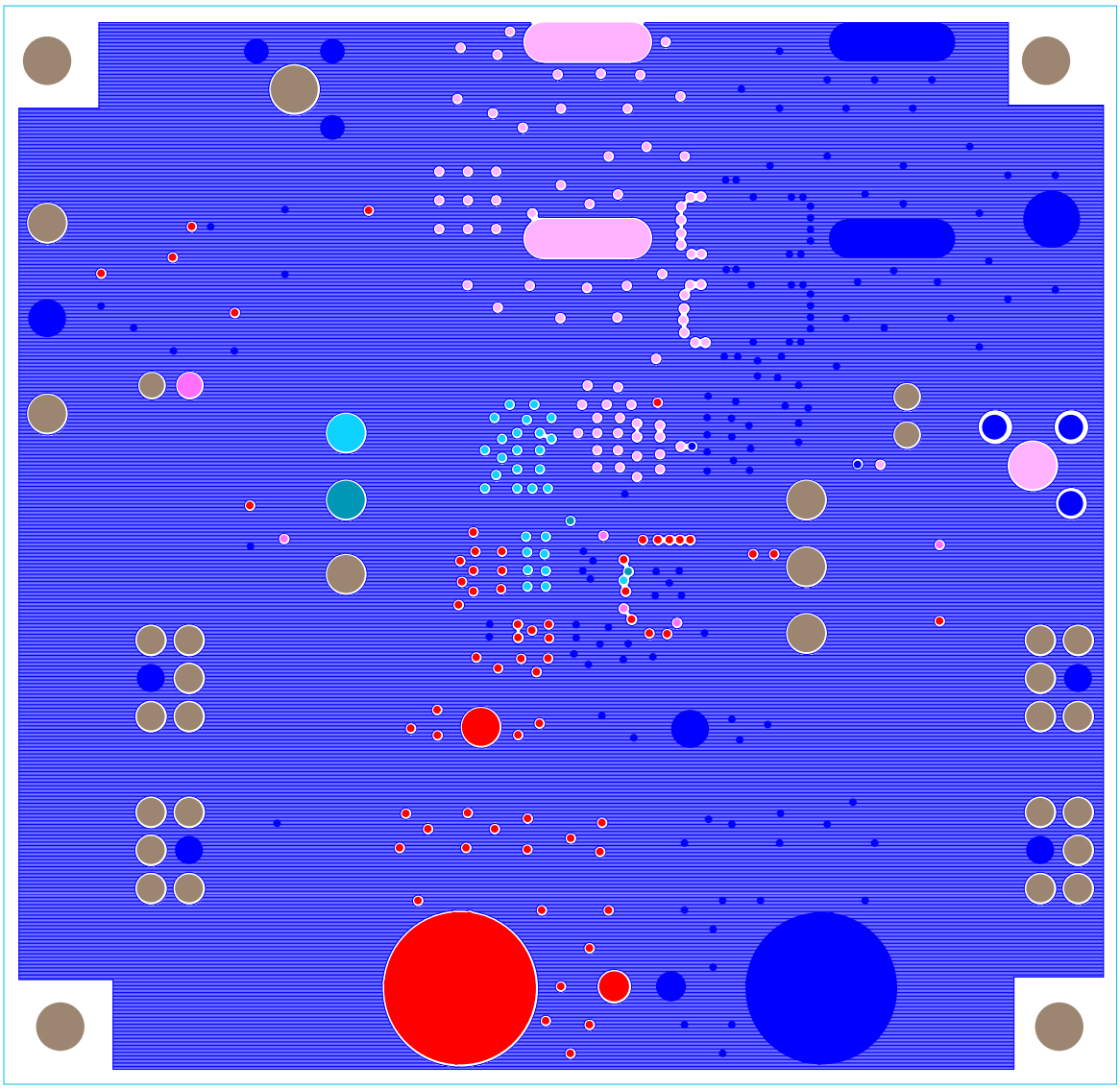

FIGURE 36. PCB - INNER LAYER 5 (TOP VIEW)

ISL68200DEMO1Z Board Layout (Continued)

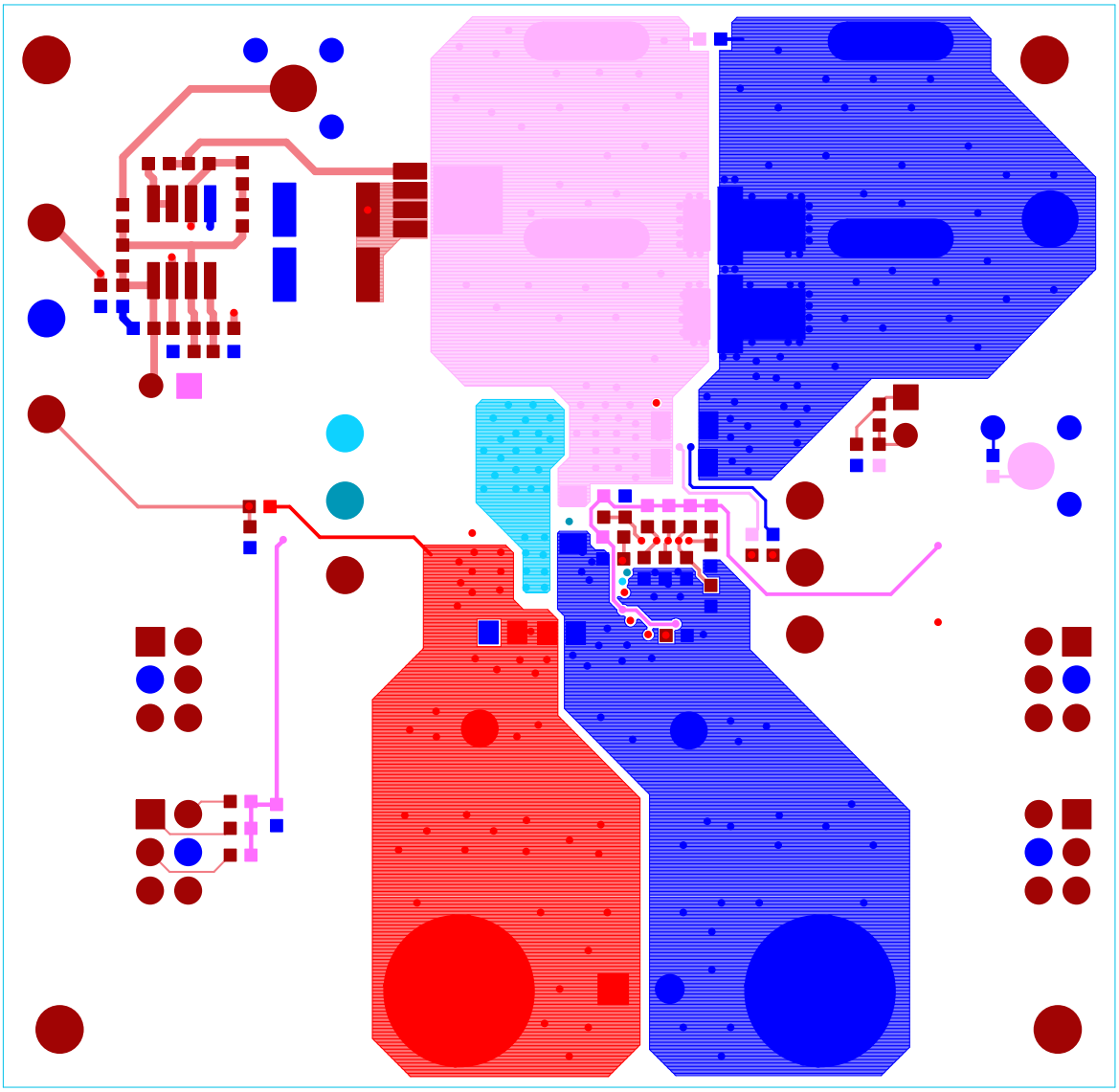

FIGURE 37. PCB - BOTTOM LAYER (TOP VIEW)

ISL68200DEMO1Z Board Layout (Continued)

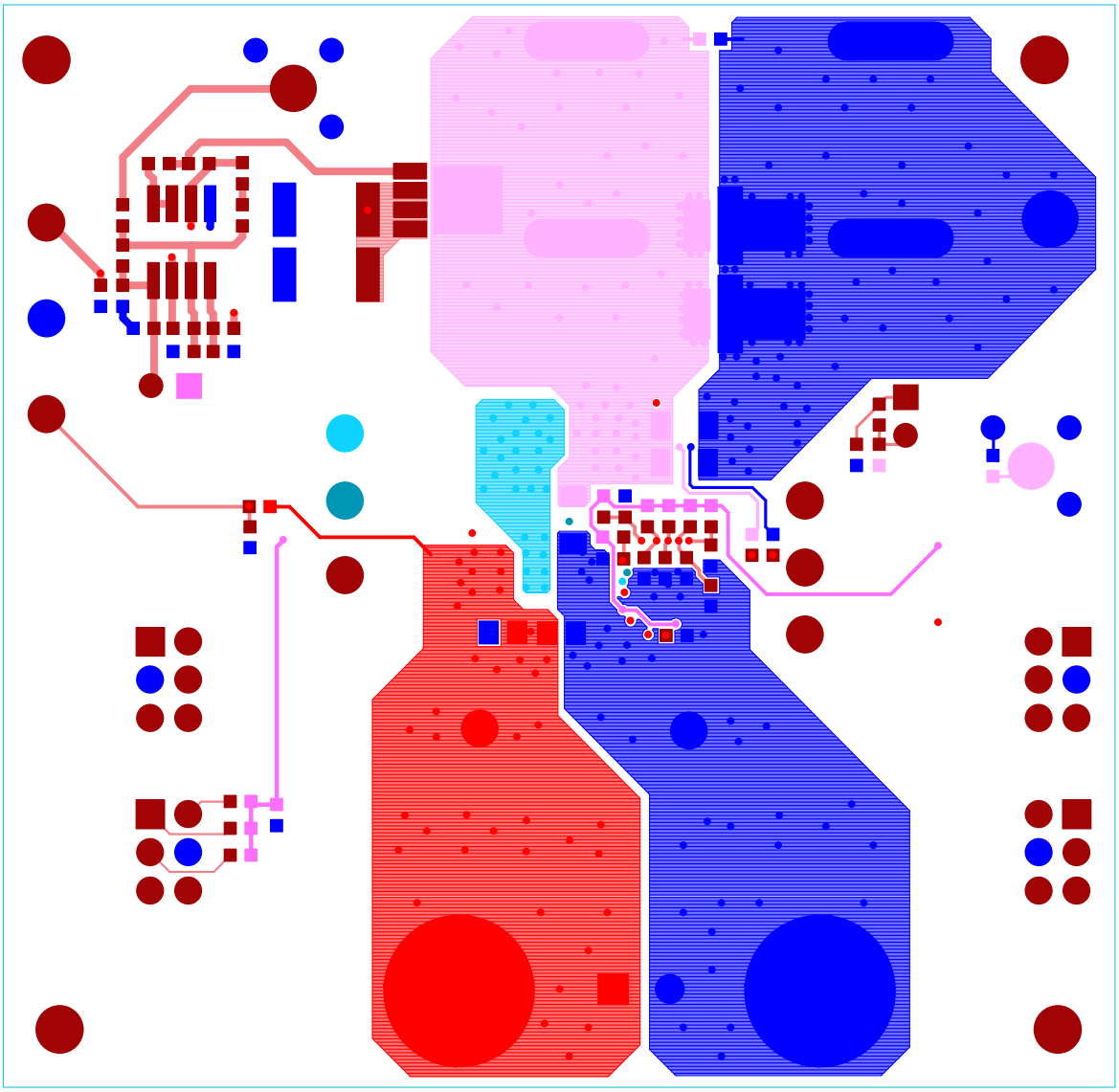

FIGURE 38. PCB - BOTTOM ASSEMBLY (TOP VIEW)