ISL22346WM

Quad Digitally Controlled Potentiometers (XDCP™) Low Noise, Low Power I^2C Bus, 128 Taps

FN6624
Rev 1.01
Apr 9, 2020

The ISL22346WMVEP integrates four digitally controlled potentiometers (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. Each potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up, the device recalls the contents of the two DCP's IVR to the corresponding WRs.

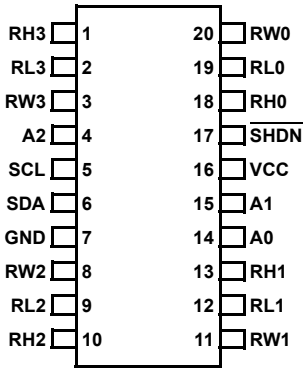
The DCPs can be used as a three-terminal potentiometers or as a two-terminal variable resistors in a wide variety of applications including control, parameter adjustments and signal processing.

Device Information

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Logistics Agency (DLA). "Hot-links" to the applicable VID and other supporting application information are provided on our website.

Pinout

ISL22346WMVEP
(20 LD TSSOP)
TOP VIEW



Features

- Specifications per DSCC VID V62/08605-01XB
- Full Mil-Temp Electrical Performance from -55°C to +125°C
- Controlled Baseline with One Wafer Fabrication Site and One Assembly/Test Site
- Full Homogeneous Lot Processing in Wafer Fab
- No Combination of Wafer Fabrication Lots in Assembly
- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification
- Enhanced Obsolescence Management
- Eliminates Need for Up-Screening a COTS Component
- Four Potentiometers in One Package
- 128 Resistor Taps
- I^2C Serial Interface
  - Three Address Pins, Up To Eight Devices/Bus
- Non-volatile Storage of Wiper Position
- Wiper Resistance: 70Ω Typical at 3.3V
- Shutdown Mode
- Shutdown Current 5µA Max
- Power Supply: 2.7V to 5.5V
- 10kΩ Total Resistance
- High Reliability
  - Endurance: 1,000,000 Data Changes Per Bit Per Register
  - Register Data Retention:
    - 10 years at T ≤ +125°C
    - 15 years at T ≤ +90°C
    - 50 years at T ≤ +55°C
- 20 Ld TSSOP

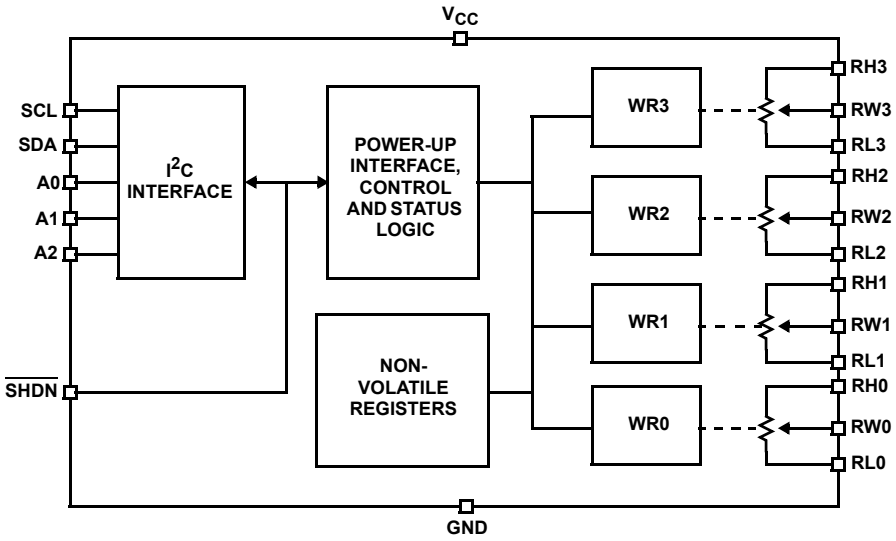
Ordering Information

VENDOR PART NUMBER (Notes 1, 2)	VENDOR ITEM DRAWING	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL22346WMVEP	V62/08605-01XB	22346 WMVEP	10	-55 to +125	20 Ld TSSOP	M20.173

NOTES:

1. Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Devices must be procured to the VENDOR PART NUMBER.

Block Diagram



Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	RH3	“High” terminal of DCP3
2	RL3	“Low” terminal of DCP3
3	RW3	“Wiper” terminal of DCP3
4	A2	Device address input for the I^2C interface
5	SCL	Open drain I^2C interface clock input
6	SDA	Open drain Serial data I/O for the I^2C interface
7	GND	Device ground pin
8	RW2	“Wiper” terminal of DCP2
9	RL2	“Low” terminal of DCP2
10	RH2	“High” terminal of DCP2
11	RW1	“Wiper” terminal of DCP1
12	RL1	“Low” terminal of DCP1
13	RH1	“High” terminal of DCP1
14	A0	Device address input for the I^2C interface
15	A1	Device address input for the I^2C interface
16	VCC	Power supply pin
17	$\overline{SHDN}$	Shutdown active low input
18	RH0	“High” terminal of DCP0
19	RL0	“Low” terminal of DCP0
20	RW0	“Wiper” terminal of DCP0

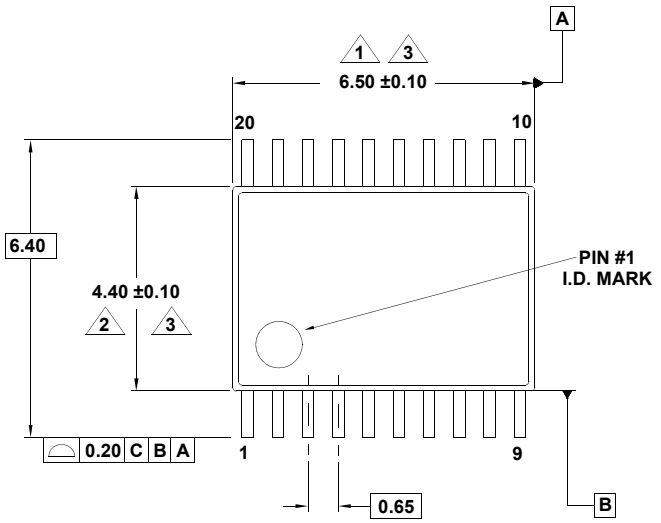
Revision History

REV.	DATE	DESCRIPTION
1.01	Apr 9, 2020	Updated vendor drawing number in ordering information table and the features bullet. Added Revision History Updated POD to the latest revision, changes are as follows: -Converted to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes.

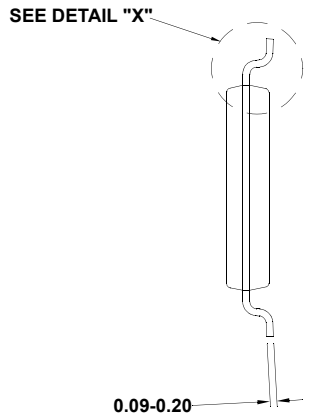
Package Outline Drawing

For the most recent package outline drawing, see M20.173.

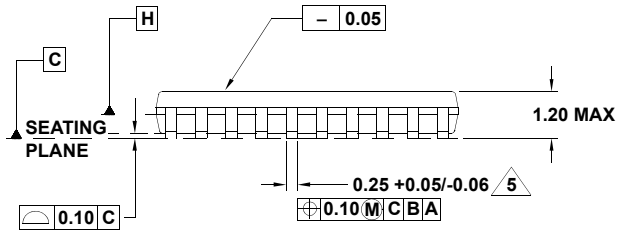
M20.173
20 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



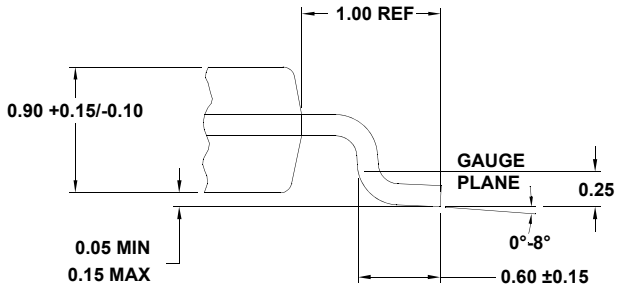
TOP VIEW



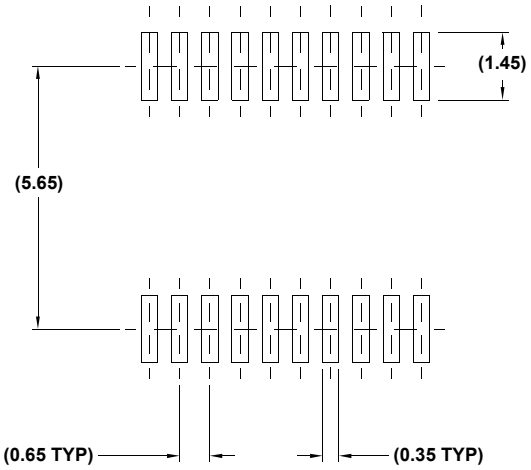
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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