ICM7245

8-Character, 16-Segment, Microp[illegible]mpatible, LED Display Decoder Driver

FN8587
Rev 0.00
October 29, 2013

The ICM7245 is an 8-character, alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 16-segment display with internal pull-up resistors. It is primarily intended for use in microprocessor systems, where it minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, 8x6 memory, high power character and segment drivers, and the multiplex scan circuitry.

6-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Sequential** (MODE = 1) or **Random** access mode (MODE = 0). In the **Sequential Access** mode the first entry is stored in the lowest location and displayed in the “left-most” character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate “right” of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading devices together. A $\overline{\text{CLR}}$ pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

Features

- Single supply +3.3V operation
- 16-Segment fonts with decimal point
- Up to 8 character display driver
- Has internal pull-up resistors of 136Ω Typical
- Microprocessor compatible
- Directly drives LED common cathode displays
- Cascadable without additional hardware
- Standby feature turns display off; puts chip in low power mode
- Sequential entry or random entry of data into display
- Character and segment drivers, All MUX scan circuitry, 8x6 static memory and 64-character ASCII font generator included on-chip
- Pb-free (RoHS compliant)

Ordering Information

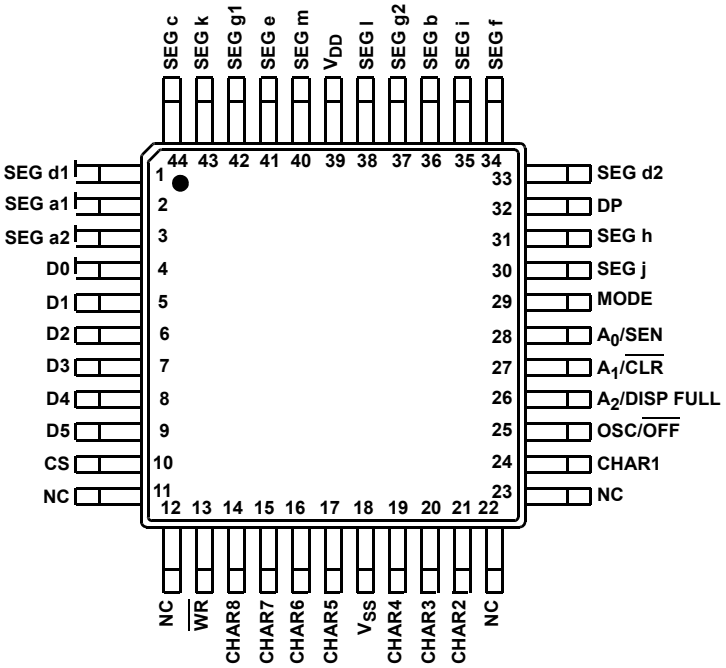
PART NUMBER (Note 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ICM7245AIM44Z	ICM7245 AIM44Z	-25°C to +85°C	44 Ld MQFP	Q44.10x10
ICM7245AIM44ZT (Note 1)	ICM7245 AIM44Z	-25°C to +85°C	44 Ld MQFP (Tape and Reel)	Q44.10x10

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ICM7245. For more information on MSL, please see tech brief TB363.

Pin Configuration

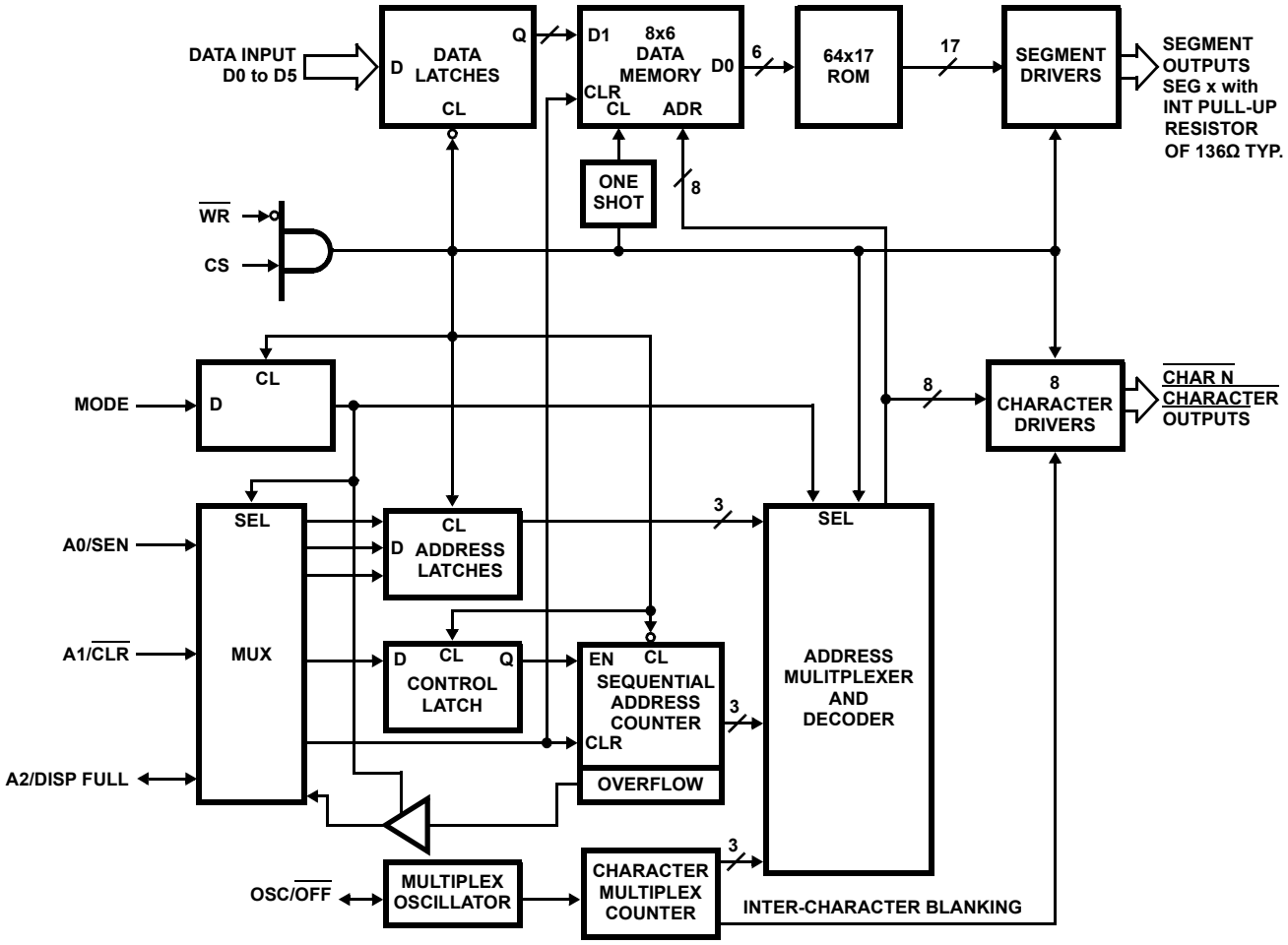
ICM7245 (16-SEGMENT CHARACTER)
(44 LD MQFP)
TOP VIEW



Pin Descriptions

SIGNAL	PIN	FUNCTION
D0 - D5	4 thru 9	6-Bit ASCII Data input pins (active high).
CS	10	Chip Select from µP address decoder, etc.
$\overline{WR}$	13	WRite pulse input pin (active low). For an active high write pulse, CS can be used.
MODE	29	Selects data entry MODE. High selects **Sequential Access (SA)** mode where first entry is displayed in “leftmost” character and subsequent entries appear to the “right”. Low selects **Random Access (RA)** mode where data is displayed on the character addressed via A0 thru A2 Address pins.
A0/SEN	28	In **RA** mode it is the LSB of the character Address. In **SA** mode it is used for cascading devices for displays of more than 8 characters (active high enables device controller).
A1/$\overline{CLR}$	27	In **RA** mode this is the second bit of the address. In **SA** mode, a low input will CLeaR the Serial Address Counter, the Data Memory and the display.
A2/DISP FULL	26	In **RA** mode this is the MSB of the Address. In **SA** mode, the output goes high after 8 entries, indicating DISPlay FULL.
OSC/$\overline{OFF}$	25	OSCillator input pin. Adding capacitance to V_{DD} will lower the internal oscillator frequency. An external oscillator can be applied to this pin. A low at this input sets the device into a (shutdown) mode, shutting OFF the display and oscillator but retaining data stored in memory.
SEG d1, SEG a1, SEG a2; SEG j, SEG h, DP, SEG d2, SEG f, SEG i, SEG b, SEG g2, SEG l; SEG m, SEG e, SEG g1, SEG k, SEG c	1 thru 3, 30 thru 38, 40 thru 44	SEGment driver outputs.
CHAR8 thru CHAR5, CHAR4 thru CHAR2, CHAR1	14 thru 17, 19 thru 21, 24	CHARacter driver outputs.
V_{SS}	18	Supply Ground.
V_{DD}	39	Positive Power Supply +3.0V to +3.6V.
NC	11, 12, 22, 23	No connection.

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage V_{DD} - V_{SS} . . . . . +5.5V
Input Voltage (Any Terminal) . . . . . V_{DD} + 0.3V to V_{SS} - 0.3V
CHARacter Output Current 300mA
SEGment Output Current 30mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
44 Ld MQFP Package (Notes 4, 5)	70	21

Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -25°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{DD} = 3.3V, V_{SS} = 0V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage (V_{DD} - V_{SS})	V_{SUPP}		3	3.3	3.6	V
Operating Supply Current	I_{DD}	V_{SUPP} = 3.6V, 10 Segments ON, All 8 Characters	-	50	-	mA
Quiescent Supply Current	I_{STBY}	V_{SUPP} = 3.6V, OSC/$\overline{OFF}$ Pin < 0.5V, CS = V_{SS}	-	3.2	25	µA
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Voltage	V_{IL}		-	-	0.8	V
Input Current	I_{IN}		-10	-	+10	µA
CHARacter Drive Current	I_{CHAR}	V_{SUPP} = 3.3V, V_{OUT} = 1V	70	135	-	mA
		V_{SUPP} = 3.0V, V_{OUT} = 2V	120	175	235	mA
CHARacter Leakage Current	I_{CHLK}		-	-	100	µA
SEGment Drive Current	I_{SEG}	V_{SUPP} = 3.3V, V_{OUT} = 2V	3.7	5.1	6.7	mA
SEGment Leakage Current	I_{SLK}		-	0.02	10	µA
DISPlay FULL Output Low	V_{OL}	I_{OL} = 1.6mA	-	-	0.4	V
DISPlay FULL Output High	V_{OH}	I_{IH} = 100µA	2.4	-	-	V
Display Scan Rate	f_{DS}		-	300	-	Hz

Electrical Specifications

Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V. V_{DD} = 3.3V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS						
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width Low	t_{WPI}		500	250	-	ns
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width High (Note 6)	t_{WPH}		-	250	-	ns
Data Hold Time	t_{DH}		0	-100	-	ns
Data Setup Time	t_{DS}		250	150	-	ns
Address Hold Time	t_{AH}		125	-	-	ns
Address Setup Time	t_{AS}		100	-	-	ns
CS Setup Time	t_{CS}		0	-	-	ns
Pulse Transition Time	t_T		-	-	100	ns
SEN Setup Time	t_{SEN}		0	-25	-	ns
Display Full Delay	t_{WDF}		760	540	-	ns

Capacitance

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}	(Note 7)	-	5	-	pF
Output Capacitance	C_O	(Note 7)	-	5	-	pF

NOTES:

6. In Sequential mode $\overline{WR}$ high must be $\geq T_{SEN} + T_{WDF}$.
7. For design reference only, not tested.

Timing Waveforms

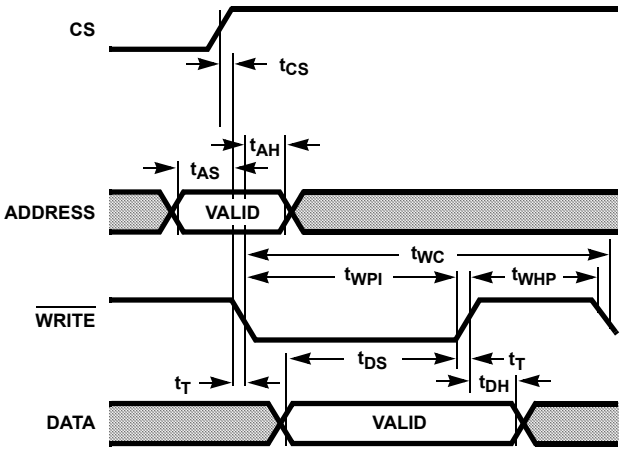


FIGURE 1. RANDOM ACCESS TIMING

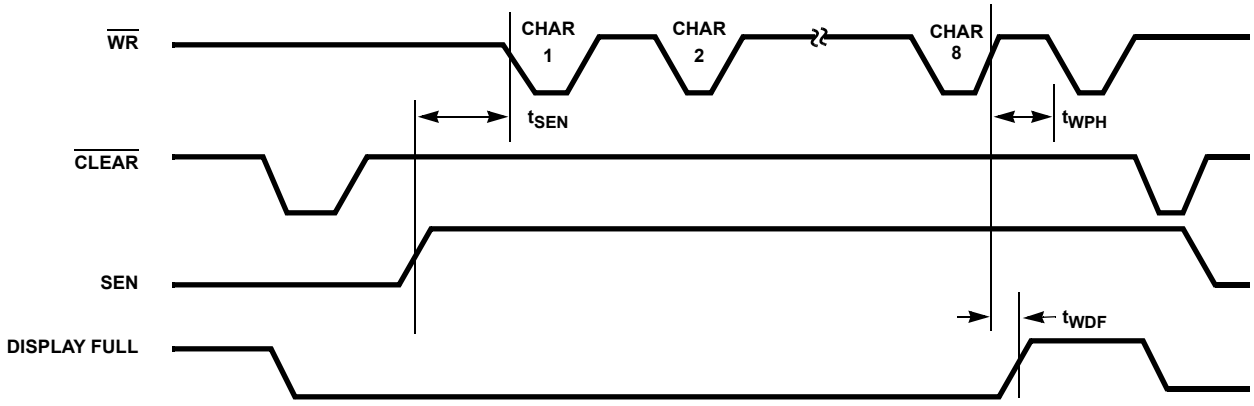


FIGURE 2. SEQUENTIAL ACCESS MODE TIMING (MODE = 1)

Timing Waveforms (Continued)

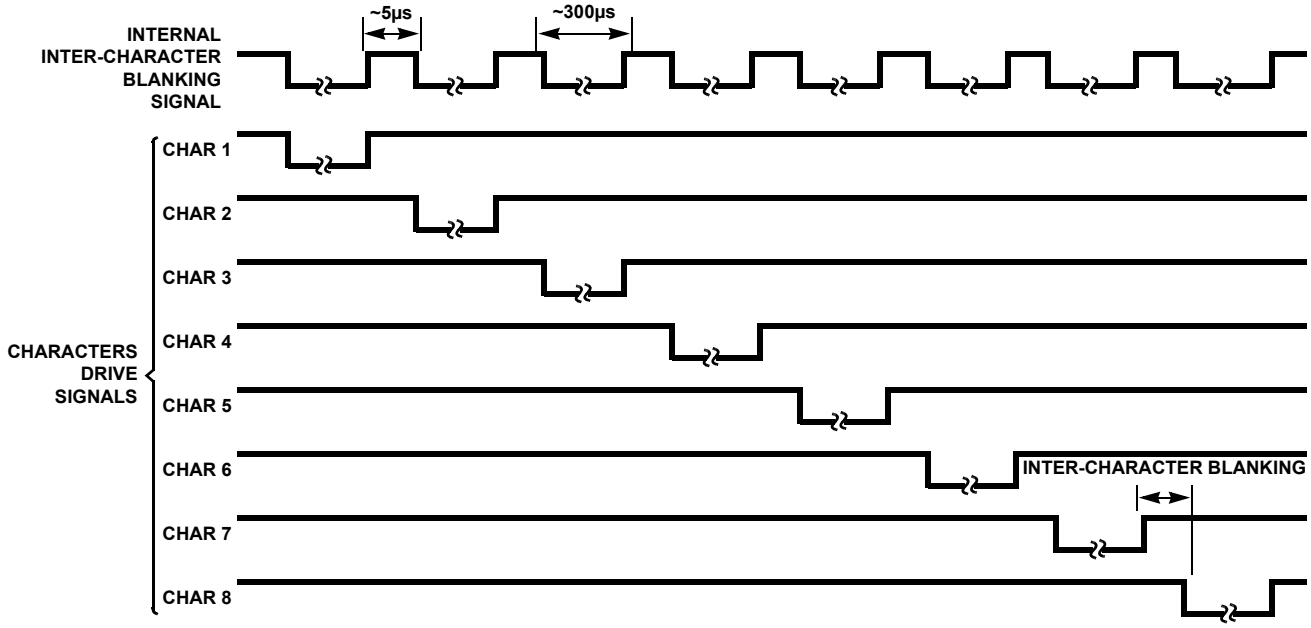


FIGURE 3. DISPLAY CHARACTERS MULTIPLEX TIMING DIAGRAM

Test Circuit

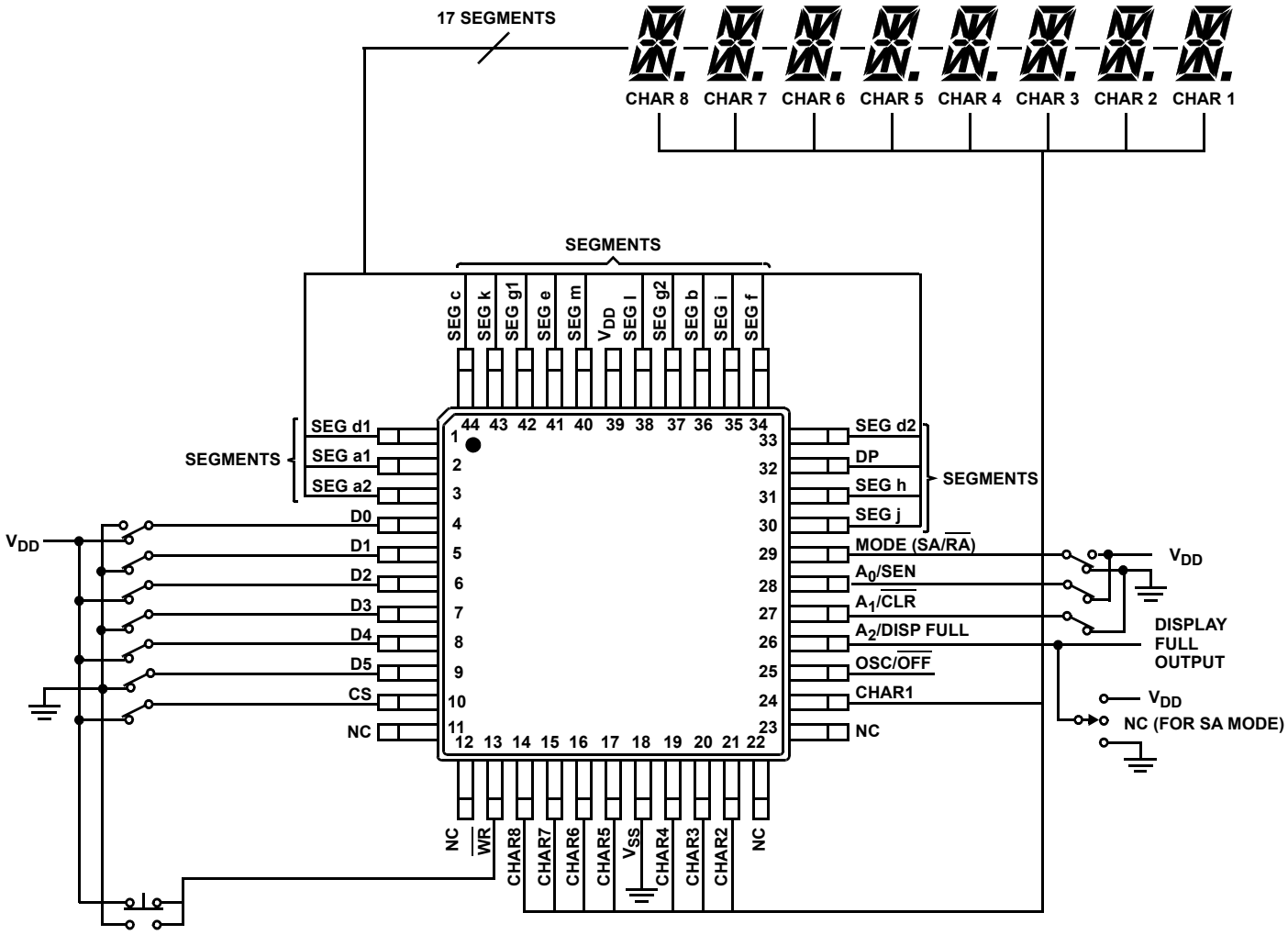


FIGURE 4.

Typical Applications

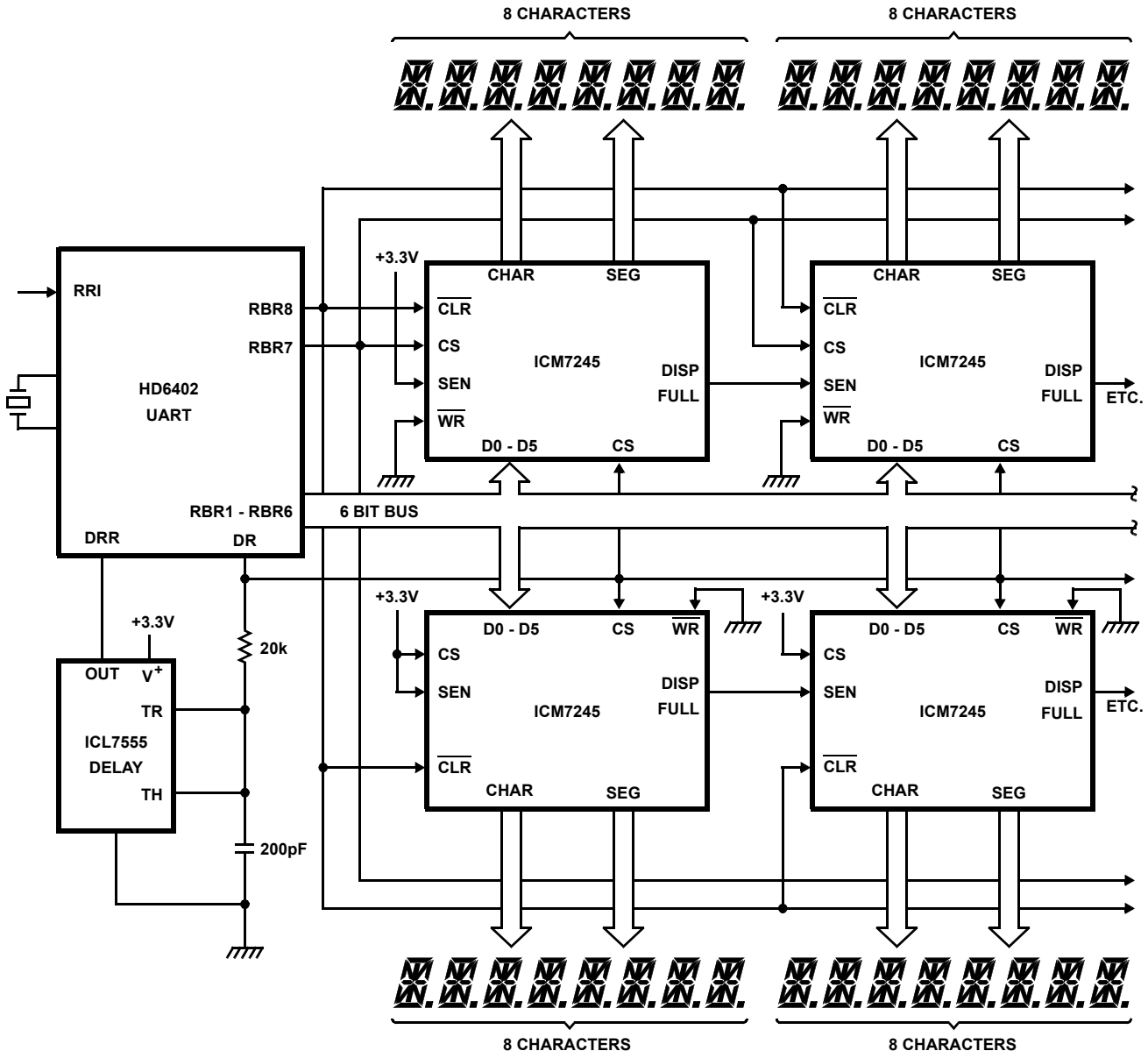


FIGURE 5. DRIVING TWO ROWS OF CHARACTERS FROM A SERIAL INPUT

Typical Applications (Continued)

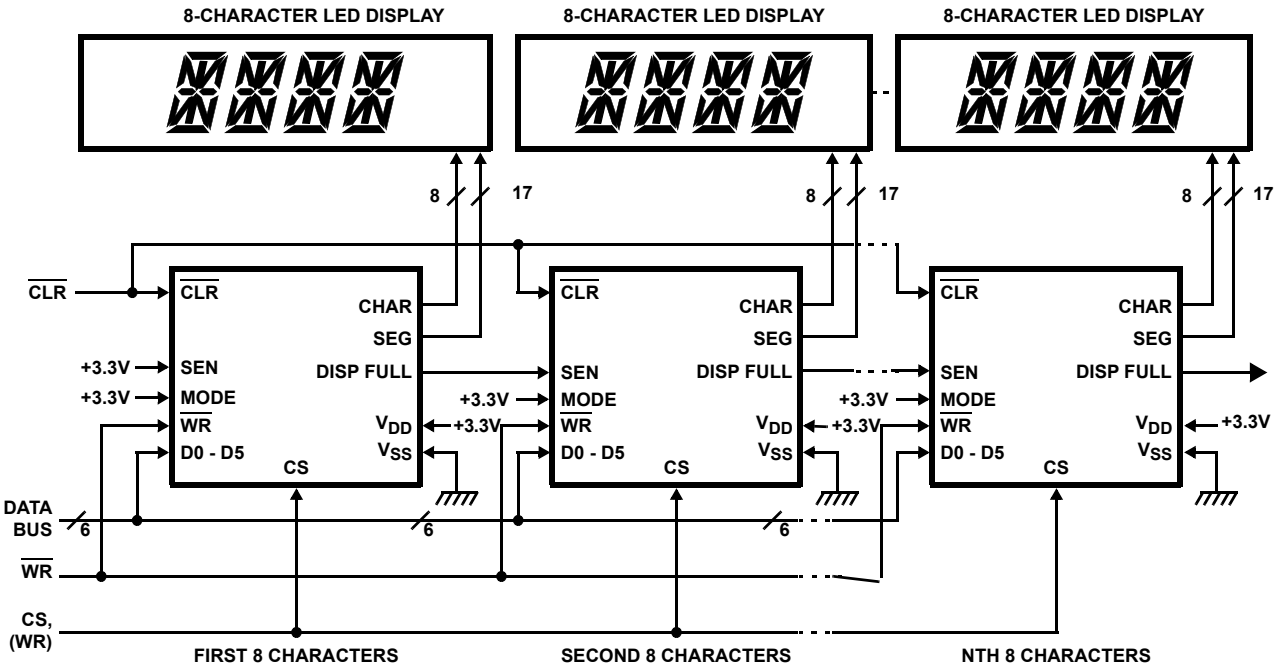


FIGURE 6. MULTICHARACTER DISPLAY USING SEQUENTIAL ACCESS MODE

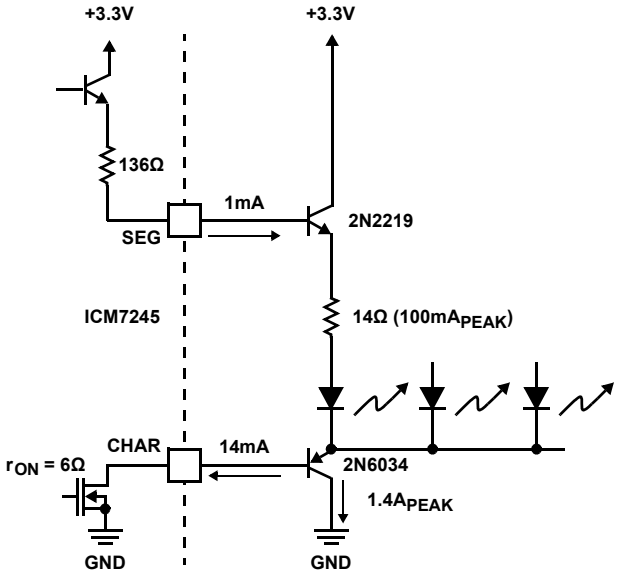


FIGURE 7A. COMMON CATHODE DISPLAY

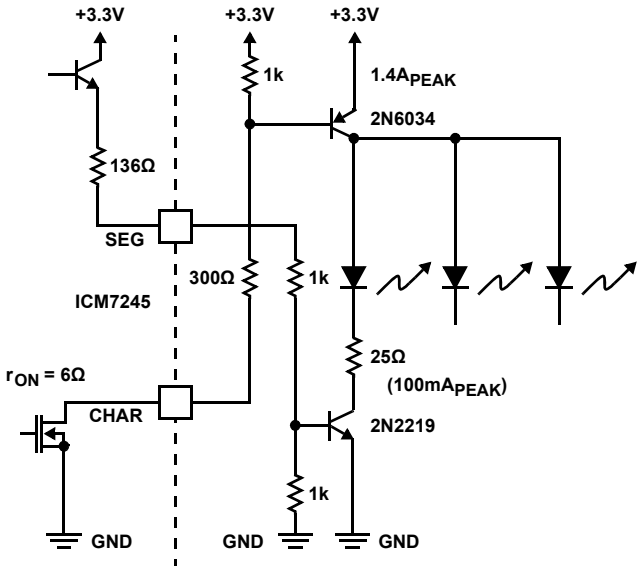


FIGURE 7B. COMMON ANODE DISPLAY

FIGURE 7. DRIVING LARGE DISPLAYS

Typical Applications (Continued)

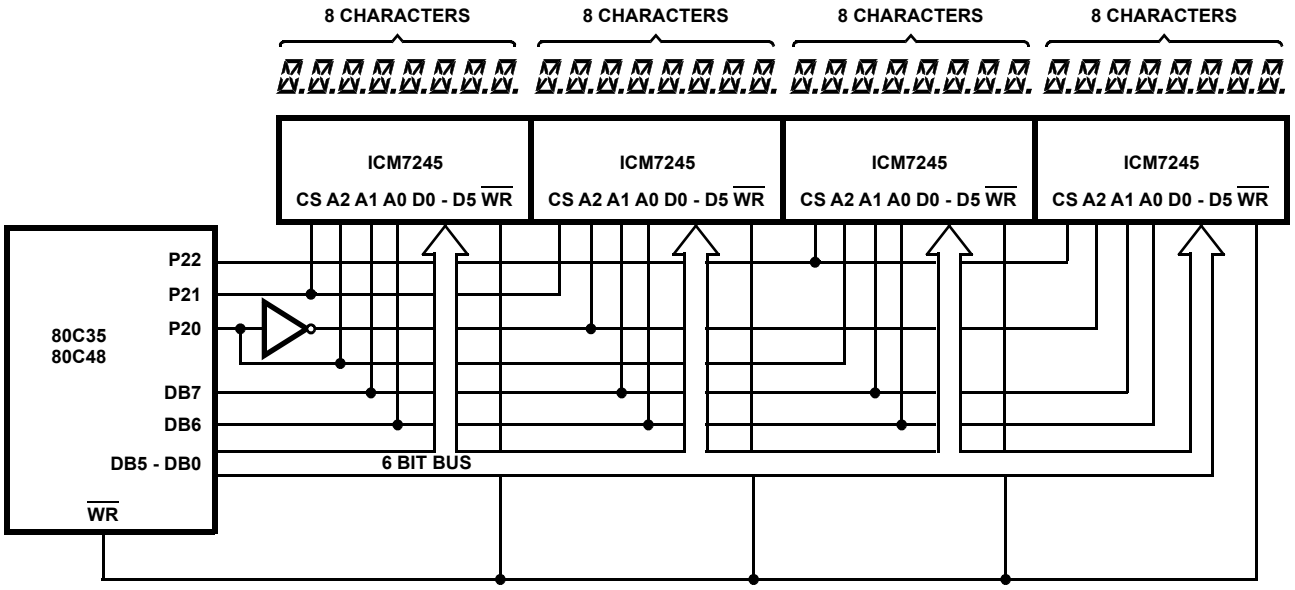
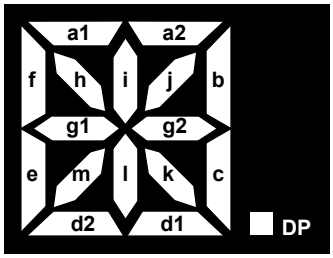
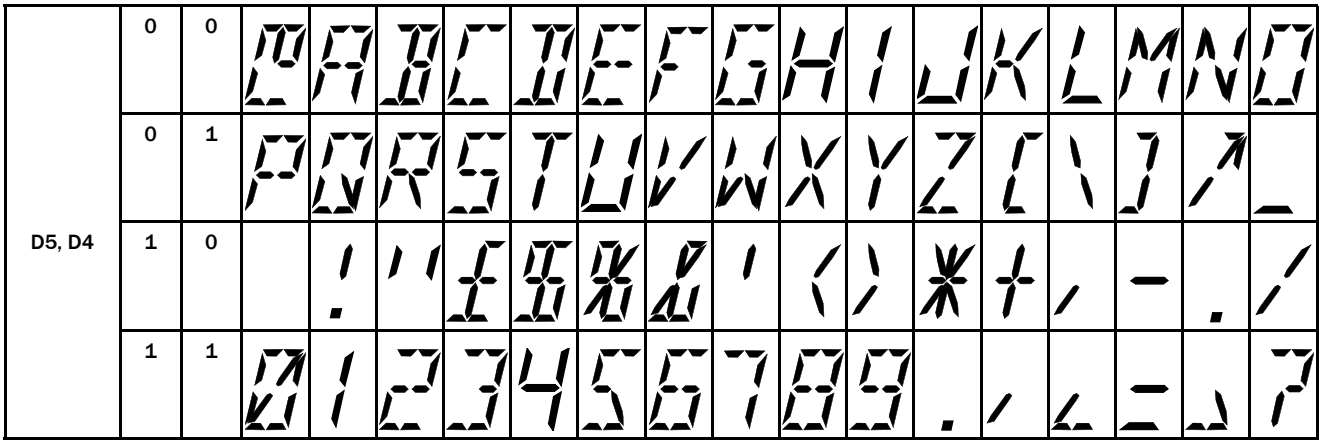


FIGURE 8. RANDOM ACCESS 32-CHARACTER DISPLAY IN A 80C48 SYSTEM

Display Font and Segment Assignments





D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

FIGURE 9. 16-SEGMENT CHARACTER FONT WITH DECIMAL POINT

Display Font and Segment Assignments (Continued)

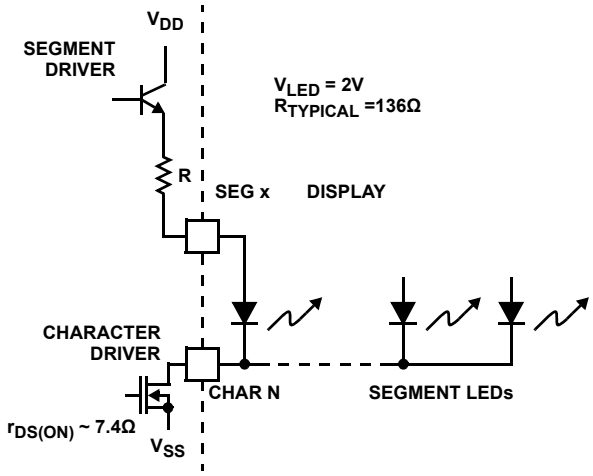


FIGURE 10. SEGMENT AND CHARACTER DRIVERS OUTPUT CIRCUIT

Detailed Description

$\overline{WR}$, CS

These pins are immediately functionally ANDed, so all actions described as occurring on an edge of $\overline{WR}$, with CS enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (about 5ns) greater than from $\overline{WR}$ due to the additional inverter required on the former.

MODE

The MODE pin input is latched on the falling edge of $\overline{WR}$ (or its equivalent, see $\overline{WR}$ description). The location (in Data Memory) where incoming data will be placed is determined either from the Address pins or the Sequential Address Counter. This is controlled by MODE input. MODE also controls the function of A0/SEN, A1/$\overline{CLR}$, and A2/DISPlay FULL lines.

Random Access Mode

When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on A0, A1 and A2 will be latched by the falling edge of $\overline{WR}$ (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by $\overline{WR}$.

Sequential Access Mode

If the internal latch is set for **Sequential Access (SA)**, (MODE latched high), the Serial ENable input or SEN will be latched on the falling edge of $\overline{WR}$ (or its equivalent). The $\overline{CLR}$ input is asynchronous, and will force-clear the Sequential Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output will be active in **SA** mode to indicate the overflow status of the Sequential Address Counter. If this output is low, and SEN is (latched) high, the contents of the Counter will be used to establish the Data Memory location for the Data input. The Counter is then incremented on the rising edge of $\overline{WR}$. If SEN is low, or DISPlay FULL is high, no action will occur. This allows easy “daisy-chaining” of display drivers for multiple character displays in a **Sequential Access** mode.

Changing Modes

Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of WR (or its equivalent). When changing mode from **Sequential Access** to **Random Access**, note that A2/DISPlay FULL will be an output until WR has fallen low, and an Address drive here could cause a conflict. When changing from **Random Access** to **Sequential Access**, A1/CLR should be high to avoid inadvertent clearing of the Data Memory and Sequential Address Counter. DISPlay FULL will become active immediately after the rising edge of WR.

Data Entry

The input Data is latched on the rising edge of $\overline{WR}$ (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in **Random Access** mode. Timing is controlled by the $\overline{WR}$ input.

OSC/$\overline{OFF}$

The device includes a relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V_{DD} at the OSC/$\overline{OFF}$ pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARacter drive lines (Figure 3). An inter-character blanking signal is derived from the pre-divider. An additional comparator on the OSC/$\overline{OFF}$ input detects a level lower than the relaxation oscillator's range, and blanks the display, disables the DISPlay FULL output (if active), and clears the pre-divider and Multiplex Counter. This puts the circuit in a low-power-dissipation mode

in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7245) without driver conflicts.

Display Output

The output of the Multiplex Counter is decoded and multiplexed into the address input of the Data Memory, except during $\overline{WR}$ operations (in Sequential Access mode, with SEN high and DISPlay FULL low), when it scans through the display data. The address decoder also drives the CHARacter outputs, except during the inter-character blanking interval (nominally about 5µs). Each CHARacter output lasts nominally about 300µs, and is repeated nominally every 2.5ms, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 segment signals, which drive the SEGment outputs. Both CHARacter and SEGment outputs are disabled during $\overline{WR}$ operations (with SEN high and DISPlay FULL Low for **Sequential Access** mode). The outputs may also be disabled by pulling OSC/$\overline{OFF}$ low.

The decode pattern from 6 bits to 17 segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by contacting **Intersil sales support**.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

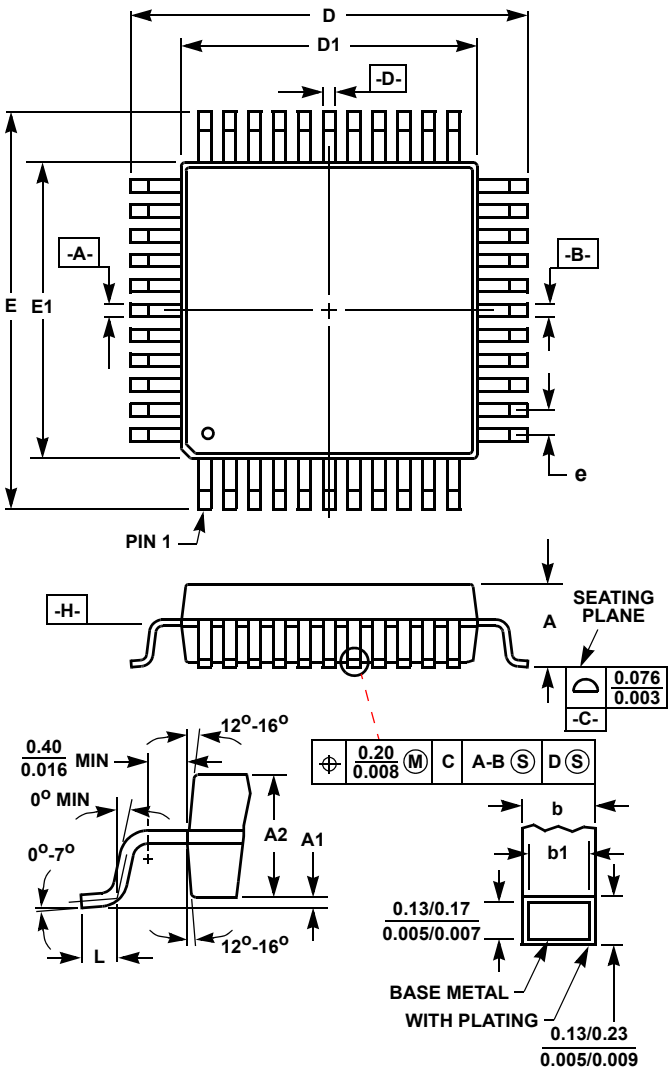
DATE	REVISION	CHANGE
October 29, 2013	FN8587.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Metric Plastic Quad Flatpack Packages (MQFP)



Q44.10x10 (JEDEC MS-022AB ISSUE B)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.096	-	2.45	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.515	0.524	13.08	13.32	3
D1	0.389	0.399	9.88	10.12	4, 5
E	0.516	0.523	13.10	13.30	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 2 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.