HIP6503

Multiple Linear Power Controller with ACPI Control Interface

FN4882
Rev 5.00
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The HIP6503 complements either an HIP6020 or an HIP6021 in ACPI-compliant designs for microprocessor and computer applications. The IC integrates four linear controllers/regulators, switching, monitoring and control functions into a 20 pin SOIC package. One linear controller generates the $3.3V_{DUAL}/3.3V_{SB}$ voltage plane from the ATX supply's 5VSB output, powering the south bridge and the PCI slots through an external pass transistor during sleep states (S3, S4/S5). A second transistor is used to switch in the ATX 3.3V output for operation during S0 and S1/S2 (active) operating states. A linear controllers/regulator supplies at choice either of 2.5V or 3.3V memory power through external pass transistors (switch for 3.3V setting) in active states. During sleep states, integrated pass transistors supply the sleep power. Another controller powers up the $5V_{DUAL}$ plane by switching in the ATX 5V output in active states, and the ATX 5VSB in sleep states. Two internal regulators output both a dedicated, noise-free 2.5V clock chip supply, as well as a 1.8V ICH2 resume well voltage. The HIP6503's operating mode (active outputs or sleep outputs) is selectable through two digital control pins, $\overline{S3}$ and $\overline{S5}$. Enabling sleep state support on the $5V_{DUAL}$ output is offered through the EN5VDL pin. In active state, the $3.3V_{DUAL}/3.3V_{SB}$ and $2.5V_{MEM}/3.3V_{MEM}$ linear regulators use external N-channel pass MOSFETs to connect the outputs directly to the 3.3V input supplied by an ATX power supply, for minimal losses. In sleep state, power delivery on both outputs is transferred to NPN transistors. Active state regulation on the $2.5V_{MEM}$ output is performed through an external NPN transistor. The $5V_{DUAL}$ output is powered through two external MOS transistors. In sleep states, a PMOS (or PNP) transistor conducts the current from the ATX 5VSB output; while in active state, current flow is transferred to an NMOS transistor connected to the ATX 5V output. The operation of the $5V_{DUAL}$ output is dictated not only by the status of the $\overline{S3}$ and $\overline{S5}$ pins, but that of the EN5VDL pin as well. The $3.3V_{DUAL}/3.3V_{SB}$ and $1.8V_{SB}$ outputs are active for as long as the ATX 5VSB voltage is applied to the chip. The $2.5V_{CLK}$ output is only active during S0 and S1/S2, and uses the 3V3 pin as input source for its internal pass element.

Features

- Provides 5 ACPI-Controlled Voltages
  - $5V_{DUAL}$ USB/Keyboard/Mouse
  - $3.3V_{DUAL}/3.3V_{SB}$ PCI/Auxiliary/LAN
  - $2.5V_{MEM}$ RDRAM or $3.3V_{MEM}$ SDRAM
  - $2.5V_{CLK}$ Clock/Processor Terminations
  - $1.8V_{SB}$ ICH2 Resume Well
- Excellent Output Voltage Regulation
  - All Outputs: ±2.0% Over Temperature (as applicable)
- Small Size; Very Low External Component Count
- RDRAM/SDRAM/DDRAM Memory Support
- Undervoltage Monitoring of All Outputs with Centralized FAULT Reporting and Temperature Shutdown
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- ACPI-Compliant Power Regulation for Motherboards

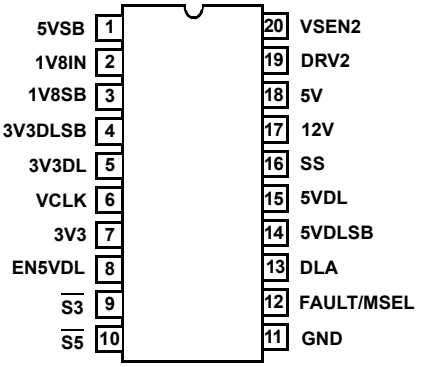
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP6503CB	0 to 70	20 Ld SOIC	M20.3
HIP6503CBZ (Note)	0 to 70	20 Ld SOIC (Pb-free)	M20.3
HIP6503CBZ-T (Note)	20 Ld SOIC Tape and Reel (Pb-free)		M20.3
HIP6503EVAL1	Evaluation Board		

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

HIP6503
(SOIC)
TOP VIEW



Block Diagram

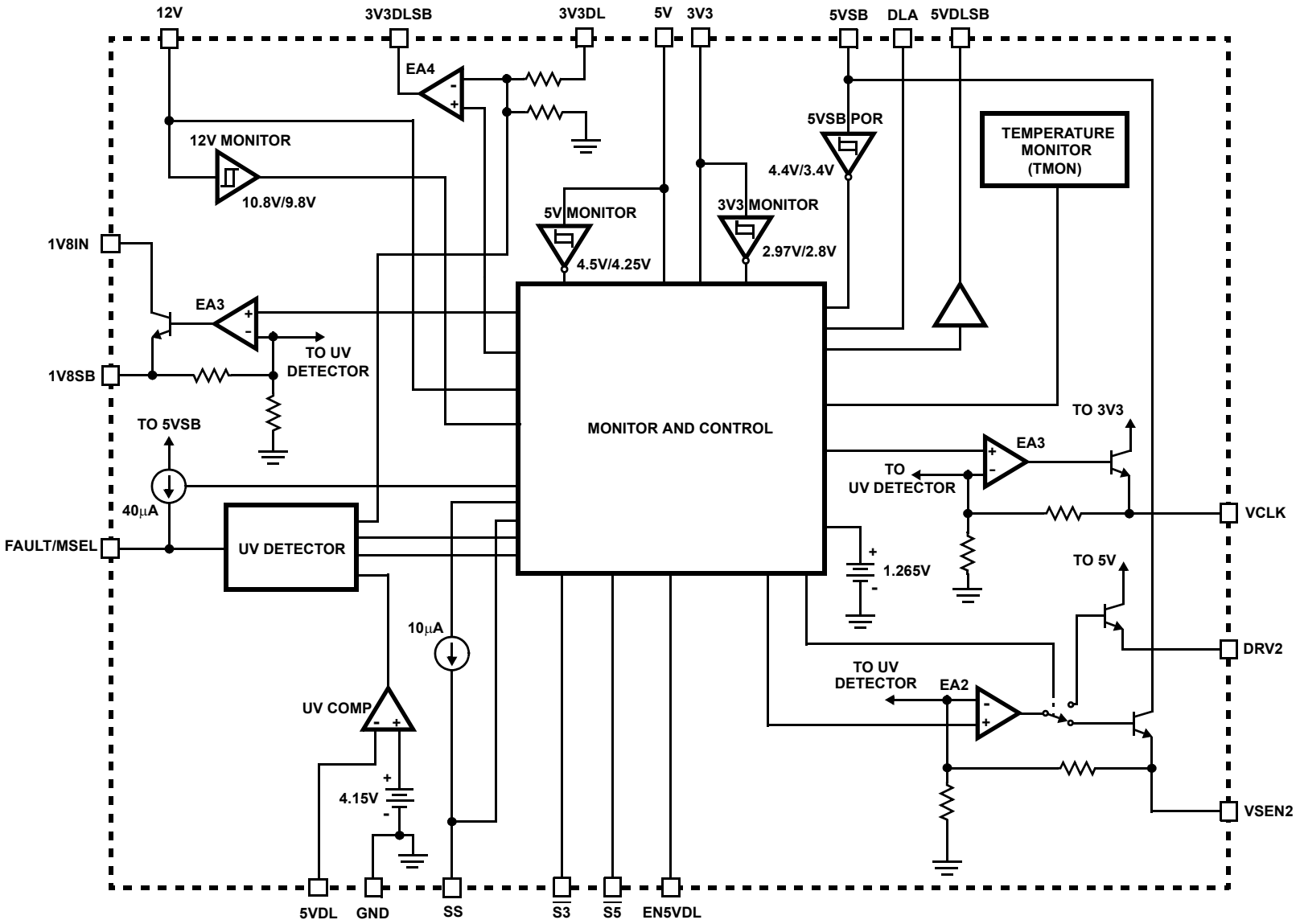


FIGURE 1.

Simplified Power System Diagram

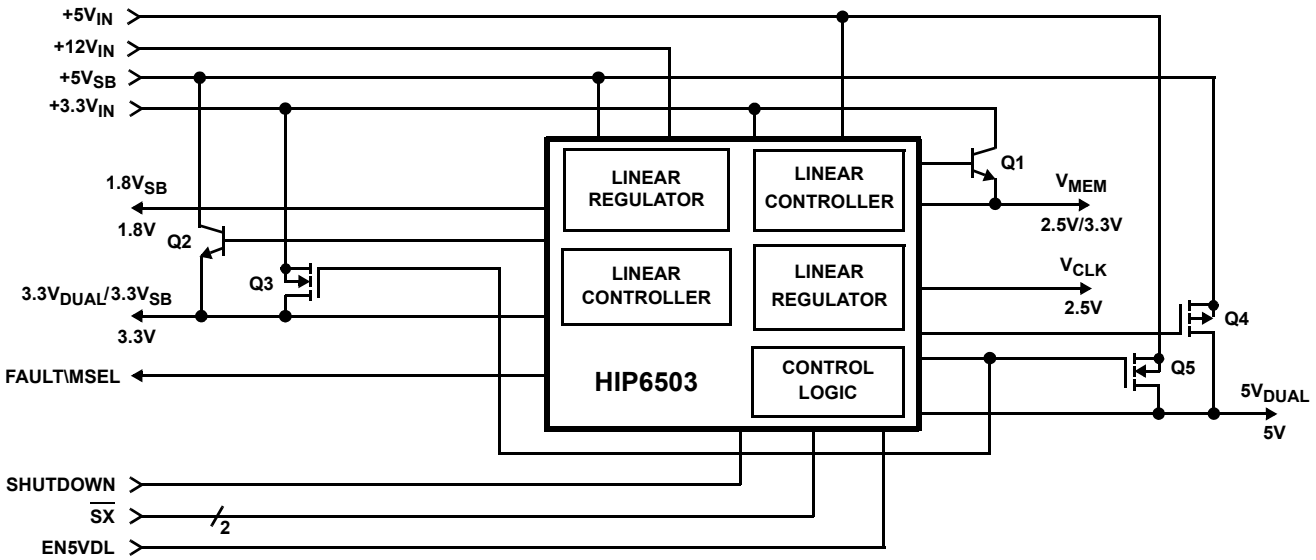


FIGURE 2.

Typical Application

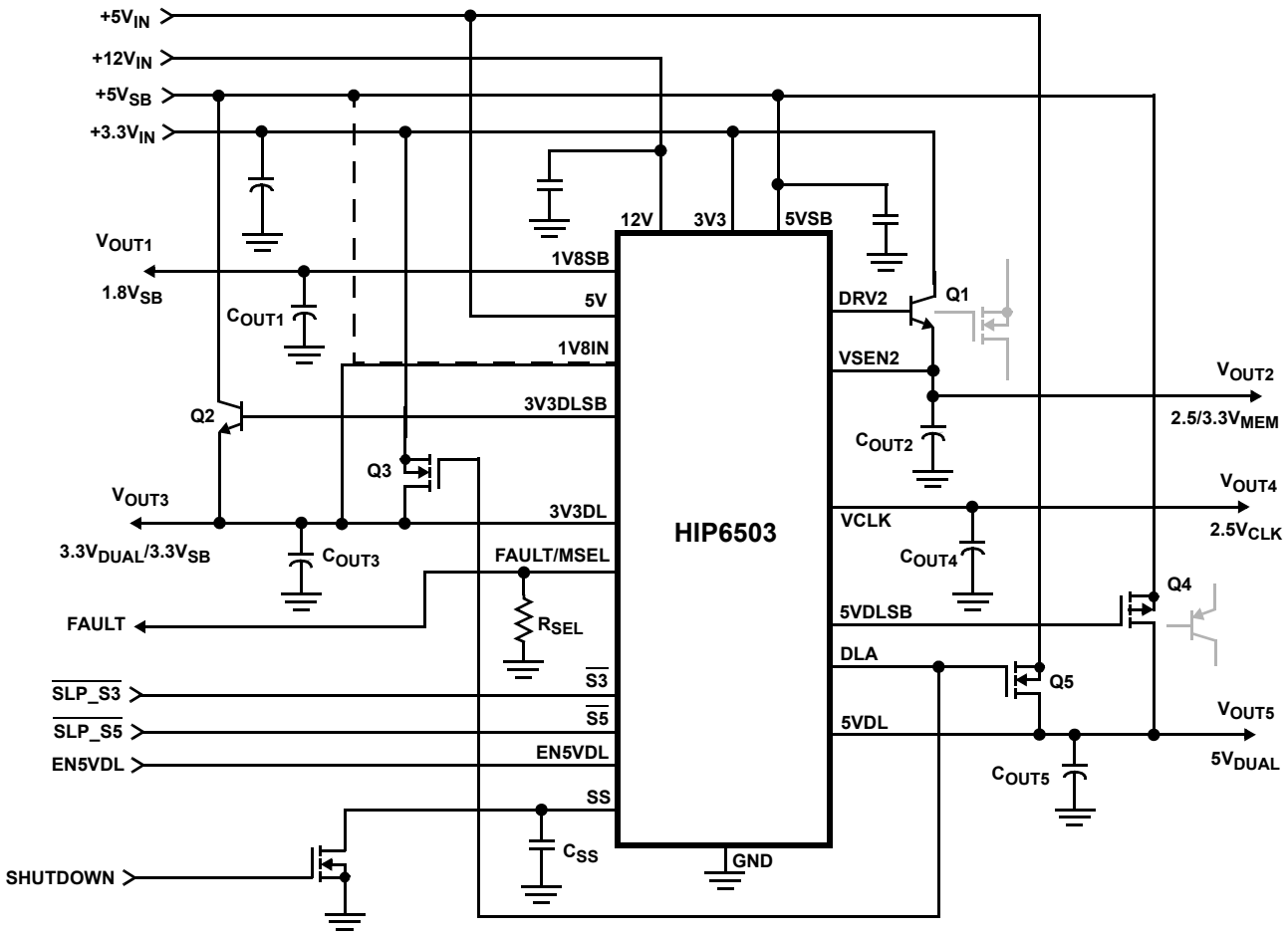


FIGURE 3.

Absolute Maximum Ratings

Supply Voltage, V_{5VSB} . . . . . +7.0V
12V. . . . . GND - 0.3V to +14.5V
DLA, DRV2 . . . . . GND - 0.3V to V_{12V} +0.3V
All Other Pins. . . . . GND - 0.3V to 5VSB + 0.3V
ESD Classification . . . . . Class 3

Recommended Operating Conditions

Supply Voltage, V_{5VSB} . . . . . +5V ±5%
Lowest 5VSB Supply Voltage Guaranteeing Parameters . . . . +4.5V
Digital Inputs, $V_{\overline{SX}}$, V_{EN5VDL}. . . . . .0 to +5.5V
Ambient Temperature Range. . . . . 0°C to 70°C
Junction Temperature Range. . . . . 0°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package (Note 1)	60

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{5VSB}		-	30	-	mA
Shutdown Supply Current	$I_{5VSB(OFF)}$	V_{SS} = 0.8V	-	14	-	mA
POWER-ON RESET, SOFT-START, AND VOLTAGE MONITORS						
Rising 5VSB POR Threshold			-	-	4.5	V
5VSB POR Hysteresis			-	1.0	-	V
Rising 12V Threshold			-	-	10.8	V
12V Hysteresis			-	1.0	-	V
Rising 3V3 and 5V Thresholds			-	90	-	%
3V3 and 5V Hysteresis			-	5	-	%
Falling Threshold Timeout (All Monitors)			-	10	-	µs
Soft-Start Current	I_{SS}		-	10	-	µA
Shutdown Voltage Threshold	V_{SD}		-	-	0.8	V
1.8V_{SB} LINEAR REGULATOR (V_{OUT1})						
Regulation			-	-	2.0	%
1V8SB Nominal Voltage Level	V_{1V8SB}		-	1.8	-	V
1V8SB Undervoltage Rising Threshold			-	1.494	-	V
1V8SB Undervoltage Hysteresis			-	54	-	mV
1V8SB Output Current	I_{1V8SB}	1V8IN = 3.3V	250	300	-	mA
2.5/3.3V_{MEM} LINEAR REGULATOR (V_{OUT2})						
Regulation (Note 2)			-	-	2.0	%
VSEN2 Nominal Voltage Level	V_{VSEN2}	R_{SEL} = 1kΩ	-	2.5	-	V
VSEN2 Nominal Voltage Level	V_{VSEN2}	R_{SEL} = 10kΩ	-	3.3	-	V
VSEN2 Undervoltage Rising Threshold			-	83	-	%
VSEN2 Undervoltage Hysteresis (Note 3)			-	3	-	%
VSEN2 Output Current	I_{VSEN2}	5VSB = 5V	250	300	-	mA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted Refer to Figures 1, 2 and 3 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DRV2 Output Drive Current	I_{DRV2}	5VSB = 5V, R_{SEL} = 1kΩ	220	-	-	mA
DRV2 Output Impedance		R_{SEL} = 10kΩ	-	200	-	Ω
$3.3V_{DUAL}$/$3.3V_{SB}$ LINEAR REGULATOR (V_{OUT3})						
Sleep State Regulation			-	-	2.0	%
3V3DL Nominal Voltage Level	V_{3V3DL}		-	3.3	-	V
3V3DL Undervoltage Rising Threshold			-	2.739	-	V
3V3DL Undervoltage Hysteresis			-	99	-	mV
3V3DLSB Output Drive Current	$I_{3V3DLSB}$	5VSB = 5V	5	10	-	mA
DLA Output Impedance			-	90	-	Ω
$2.5V_{CLK}$ LINEAR REGULATOR (V_{OUT4})						
Regulation			-	-	2.0	%
VCLK Nominal Voltage Level	V_{VCLK}		-	2.5	-	V
VCLK Undervoltage Rising Threshold			-	2.075	-	V
VCLK Undervoltage Hysteresis			-	75	-	mV
VCLK Output Current (Note 4)	I_{VCLK}	V_{3V3} = 3.3V	500	800	-	mA
$5V_{DUAL}$ SWITCH CONTROLLER (V_{OUT5})						
5VDL Undervoltage Rising Threshold			-	4.150	-	V
5VDL Undervoltage Hysteresis			-	150	-	mV
5VDLSB Output Drive Current	I_{5VDLSB}	5VDLSB = 4V, 5VSB = 5V	-20	-	-40	mA
5VDLSB Pull-Up Impedance to 5VSB			-	350	-	Ω
TIMING INTERVALS						
Active State Assessment Past Input UV Thresholds (Note 5)			20	25	30	ms
Active-to-Sleep Control Input Delay			-	200	-	µs
CONTROL I/O ($\overline{S3}$, $\overline{S5}$, EN5VDL, FAULT/MSEL)						
High Level Input Threshold			-	-	2.2	V
Low Level Input Threshold			0.8	-	-	V
$\overline{S3}$, $\overline{S5}$ Internal Pull-up Impedance to 5VSB			-	50	-	kΩ
FAULT Output Impedance		FAULT = high	-	100	-	Ω
TEMPERATURE MONITOR						
Fault-Level Threshold (Note 6)			125	-	-	°C
Shutdown-Level Threshold (Note 6)			-	155	-	°C

NOTES:

2. Sleep-State Only for 3.3V Setting
3. Parameters not guaranteed for 5VSB < 4.0V.
4. At Ambient Temperatures Less Than 50°C.
5. Guaranteed by Correlation.
6. Guaranteed by Design.

Functional Pin Description

3V3 (Pin 7)

Connect this pin to the ATX 3.3V output. This pin provides the output current for the 2V5CLK pin, and is monitored for power quality.

5VSB (Pin 1)

Provide a very well de-coupled 5V bias supply for the IC to this pin by connecting it to the ATX 5VSB output. This pin provides the output current for the VSEN1 and VSEN2 pins, as well as the base current for Q2. The voltage at this pin is monitored for power-on reset (POR) purposes.

5V (Pin 18)

Connect this pin to the ATX 5V output. This pin provides the base bias current for Q1, and is monitored for power quality.

12V (Pin 17)

Connect this pin to the ATX 12V output. This pin provides the gate bias voltage for Q3, Q5 and Q6, and is monitored for power quality.

GND (Pin 11)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

$\overline{S3}$ and $\overline{S5}$ (Pins 9 and 10)

These pins switch the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states. These are digital inputs featuring internal 50kΩ (typical) resistor pull-ups to 5VSB. Internal circuitry de-glitches these pins for disturbances lasting as long as 2μs (typically). Additional circuitry blocks any illegal state transitions (such as $\overline{S3}$ to $\overline{S4/S5}$ or vice versa). Respectively, connect $\overline{S3}$ and $\overline{S5}$ to the computer system's $\overline{SLP\_S3}$ and $\overline{SLP\_S5}$ signals.

EN5VDL (Pin 8)

This pin enables or disables sleep state support on the $5V_{DUAL}$ output in response to S3 and S4/S5 requests. This is a digital input pin whose status can only be changed during active state operation or during chip shutdown (SS pin grounded by external open-drain device or chip bias below POR level). The input information is latched-in when entering a sleep state, as well as following 5VSB POR release or exit from shutdown. EN5VDL is internally pulled high through a 40μA current source.

FAULT/MSEL (Pin 12)

This is a multiplexed function pin allowing the setting of the memory output voltage to either 2.5V or 3.3V (for RDRAM or SDRAM memory systems). An internal 40μA current source creates a voltage across an external resistor - this voltage level is compared to an internal 200mV reference and the memory regulator output voltage is set.

In case of an undervoltage on any of the controlled outputs, on any of the monitored ATX supplies, or in case of an overtemperature event, this pin is used to report the fault condition by being pulled to 5VSB.

SS (Pin 16)

Connect this pin to a small ceramic capacitor (no less than 5nF; 0.1μF recommended). The internal soft-start (SS) current source along with the external capacitor creates a voltage ramp used to control the ramp-up of the output voltages. Pulling this pin low with an open-drain device shuts down all the outputs as well as force the FAULT pin low. The C_{SS} capacitor is also used to provide a controlled voltage slew rate during active-to-sleep transitions on the $3.3V_{DUAL}/3.3V_{SB}$ and $2.5V_{MEM}/3.3V_{MEM}$ outputs.

VSEN2 (Pin 20)

Connect this pin to the memory output (V_{OUT2}). In sleep states, this pin is regulated to 2.5V through an internal pass transistor capable of delivering 300mA (typically). The active-state voltage at this pin is regulated through an external NPN transistor connected at the DRV2 pin. During all operating states, the voltage at this pin is monitored for under-voltage events.

DRV2 (Pin 19)

Connect this pin to the base of a suitable NPN transistor. This pass transistor regulates the 2.5V output from the ATX 3.3V during active states operation.

3V3DL (Pin 5)

Connect this pin to the 3.3V dual/stand-by output (V_{OUT3}). In sleep states, the voltage at this pin is regulated to 3.3V; in active states, ATX 3.3V output is delivered to this node through a fully on N-MOS transistor. During all operating states, this pin is monitored for under-voltage events.

3V3DLSB (Pin 4)

Connect this pin to the base of a suitable NPN transistor. In sleep state, this transistor is used to regulate the voltage at the 3V3DL pin to 3.3V.

DLA (Pin 13)

Connect this pin to the gates of suitable N-MOSFETs, which in active state, switch in the ATX 3.3V and 5V outputs into the $3.3V_{MEM}$, $3.3V_{DUAL}/3.3V_{SB}$ and $5V_{DUAL}$ outputs, respectively.

5VDL (Pin 15)

Connect this pin to the $5V_{DUAL}$ output (V_{OUT5}). In either operating state, the voltage at this pin is provided through a fully on MOS transistor. This pin is also monitored for under-voltage events.

5VDLSB (Pin 14)

Connect this pin to the gate of a suitable P-MOSFET or bipolar PNP. In sleep state, this transistor is switched on, connecting the ATX 5VSB output to the $5V_{DUAL}$ regulator output.

1V8SB (Pin 3)

This pin is the output of the internal 1.8V regulator (V_{OUT1}). This internal regulator operates for as long as 5VSB is applied to the HIP6503. This pin is monitored for under-voltage events.

1V8IN (Pin 2)

This pin is the input supply for the 1.8V internal regulator's pass element. Connect this pin to the $3.3V_{DUAL}/3.3V_{SB}$ output.

VCLK (Pin 6)

This pin is the output of the internal 2.5V clock chip regulator (V_{OUT4}). This internal regulator operates only in active states (S0, S1/S2) and is shut off during any sleep state, regardless of the configuration of the chip. This pin is monitored for under-voltage events.

Description

Operation

The HIP6503 controls 5 output voltages (Refer to Figures 1, 2, and 3). It is designed for microprocessor computer applications with 3.3V, 5V, 5VSB, and 12V bias input from an ATX power supply. The IC is composed of three linear controllers/regulators supplying the computer system's $1.8V_{SB}$ (V_{OUT1}), $3.3V_{SB}$ and PCI slots' $3.3V_{AUX}$ power (V_{OUT3}), the 2.5V RDRAM and 3.3V SDRAM memory power (V_{OUT2}), an integrated regulator dedicated to 2.5V clock chip (V_{OUT4}), a dual switch controller supplying the $5V_{DUAL}$ voltage (V_{OUT5}), as well as all the control and monitoring functions necessary for complete ACPI implementation.

Initialization

The HIP6503 automatically initializes upon receipt of input power. The Power-On Reset (POR) function continually monitors the 5VSB input supply voltage, initiating $3.3V_{DUAL}/3.3V_{SB}$ and $1.8V_{SB}$ soft-start operation shortly after exceeding POR threshold. At 3ms (typically) after these two outputs finish their ramp-up, the EN5VDL and MSEL status is latched in and the chip proceeds to ramp up the remainder of the voltages, as required.

Operational Truth Table

The EN5VDL pin offers the choice of supporting or disabling 5VDUAL output in S3 and S4/S5 sleep states. Table 1 describes the truth combinations pertaining to this output.

TABLE 1. $5V_{DUAL}$ OUTPUT (V_{OUT5}) TRUTH TABLE

EN5VDL	$\overline{S5}$	$\overline{S3}$	5VDL	COMMENTS
0	1	1	5V	S0, S1 States (Active)
0	1	0	0V	S3
0	0	1	Note	Maintains Previous State
0	0	0	0V	S4/S5
1	1	1	5V	S0, S1 States (Active)
1	1	0	5V	S3
1	0	1	Note	Maintains Previous State
1	0	0	5V	S4/S5

NOTE: Combination Not Allowed.

The internal circuitry does not allow the transition from an S3 (suspend to RAM) state to an S4/S5 (suspend to disk/soft off) state or vice versa. The only 'legal' transitions are from an active state (S0, S1) to a sleep state (S3, S5) and vice versa.

Functional Timing Diagrams

Figures 4 through 6 are timing diagrams, detailing the power up/down sequences of all three outputs in response to the status of the enable (EN5VDL) and sleep-state pins ($\overline{S3}$, $\overline{S5}$), as well as the status of the ATX supply.

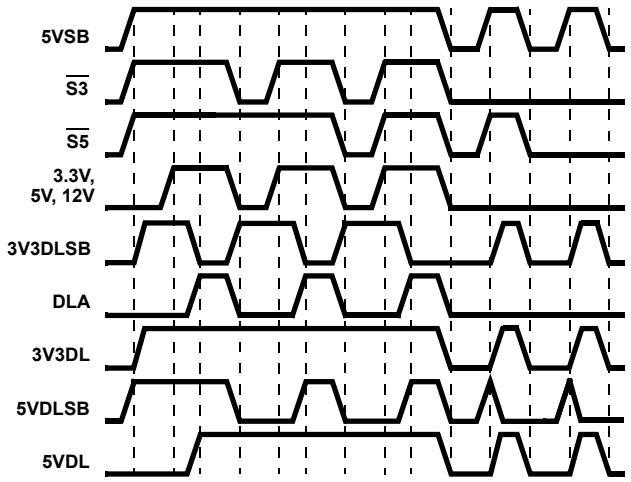


FIGURE 4. $5V_{DUAL}$ TIMING DIAGRAM FOR EN5VDL = 1; $3.3V_{DUAL}/3.3V_{SB}$

The status of the EN5VDL pin can only be changed while in active (S0, S1) states, when the bias supply (5VSB pin) is below POR level, or during chip shutdown (SS pin shorted to GND or within 3ms of 5VSB POR); a status change of this pin while in a sleep state is ignored.

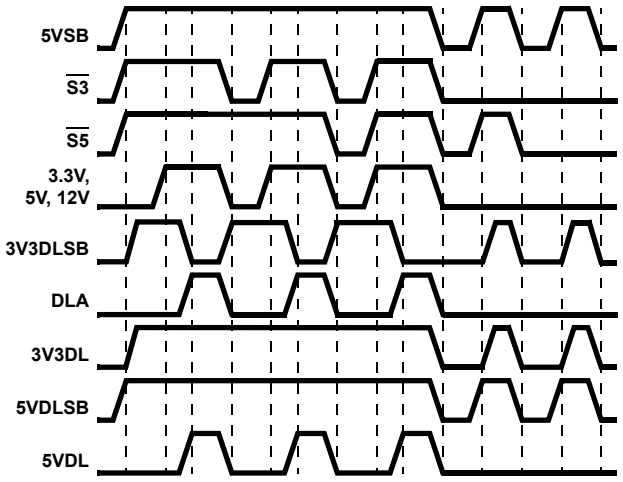


FIGURE 5. $5V_{DUAL}$ TIMING DIAGRAM FOR EN5VDL = 0; $3V_{DUAL}/3V_{SB}$

Not shown in these diagrams is the deglitching feature used to protect against false sleep state tripping. Both $\overline{S3}$ and $\overline{S5}$ pins are protected against noise by a 2µs filter (typically 1 - 4µs). This feature is useful in noisy computer environments if the control signals have to travel over significant distances. Additionally, the $\overline{S3}$ pin features a 200µs delay in transitioning to sleep states. Once the $\overline{S3}$ pin goes low, an internal timer is activated. At the end of the 200µs interval, if the $\overline{S5}$ pin is low, the HIP6503 switches into S5 sleep state; if the $\overline{S5}$ pin is high, the HIP6503 goes into S3 sleep state.

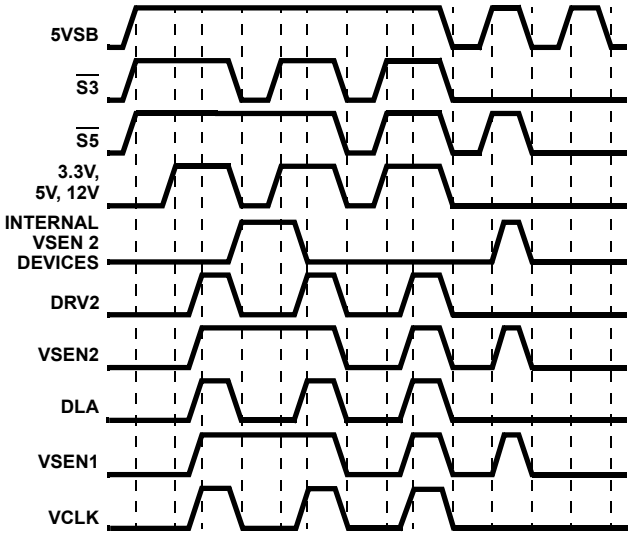


FIGURE 6. $2.5V_{MEM}$, $3.3V_{MEM}$, AND $2.5V_{CLK}$ TIMING DIAGRAM

Soft-Start Circuit

SOFT-START INTO SLEEP STATES (S3, S4/S5)

The 5VSB POR function initiates the soft-start sequence. An internal 10µA current source charges an external capacitor. The error amplifiers reference inputs are clamped to a level proportional to the SS (soft-start) pin voltage. As the SS pin voltage slews from about 1.25V to 2.5V, the input clamp allows a rapid and controlled output voltage rise.

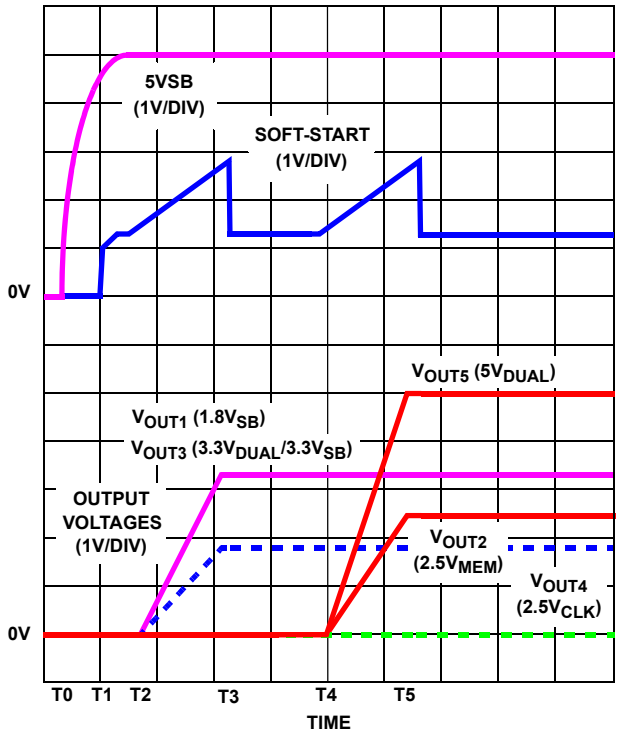


FIGURE 7. SOFT-START INTERVAL IN A SLEEP STATE (ALL OUTPUTS ENABLED)

Figure 7 shows the soft-start sequence for the typical application start-up in sleep state with all output voltages enabled. At time T0 5VSB (bias) is applied to the circuit. At time T1 the 5VSB surpasses POR level. An internal fast charge circuit quickly raises the SS capacitor voltage to approximately 1V, then the 10µA current source continues the charging. The soft-start capacitor voltage reaches approximately 1.25V at time T2, at which point the $3.3V_{DUAL}/3.3V_{SB}$ and $1.8V_{SB}$ error amplifiers' reference inputs start their transition, resulting in the output voltages ramping up proportionally. The ramp-up continues until time T3 when the two voltages reach the set value. As the soft-start capacitor voltage reaches approximately 2.75V, the under-voltage monitoring circuit of this output is activated and the soft-start capacitor is quickly discharged to approximately 1.25V. Following the 3ms (typical) time-out between T3 and T4, the MSEL and EN5VDL selections are latched in, and the soft-start capacitor commences a second ramp-up designed to smoothly bring up the remainder of the voltages required by the system. At time T5 all voltages are within regulation limits, and as the SS voltage reaches 2.75V, all the remaining UV monitors are activated and the SS capacitor is quickly discharged to 1.25V, where it remains until the next transition. As the $2.5V_{CLK}$ output is only active while in an active state, it does not come up, but

rather awaits until the main ATX outputs are well within regulation limits.

SOFT-START INTO ACTIVE STATES (S0, S1)

If both $\overline{S3}$ and $\overline{S5}$ are logic high at the time the 5VSB is applied, the HIP6503 will assume active state wake-up and keep off the required outputs until some time (typically 25ms) after the ATX's main outputs used by the application (3.3V, 5V, and 12V) exceed the set thresholds. This time-out feature is necessary in order to insure the main ATX outputs are stabilized. The time-out also assures smooth transitions from sleep into active when sleep states are being supported. $3.3V_{DUAL}/3.3V_{SB}$ and $1.8V_{SB}$ outputs, whose operation is only dependent on $5V_{SB}$ presence, will come up right after bias voltage surpasses POR level.

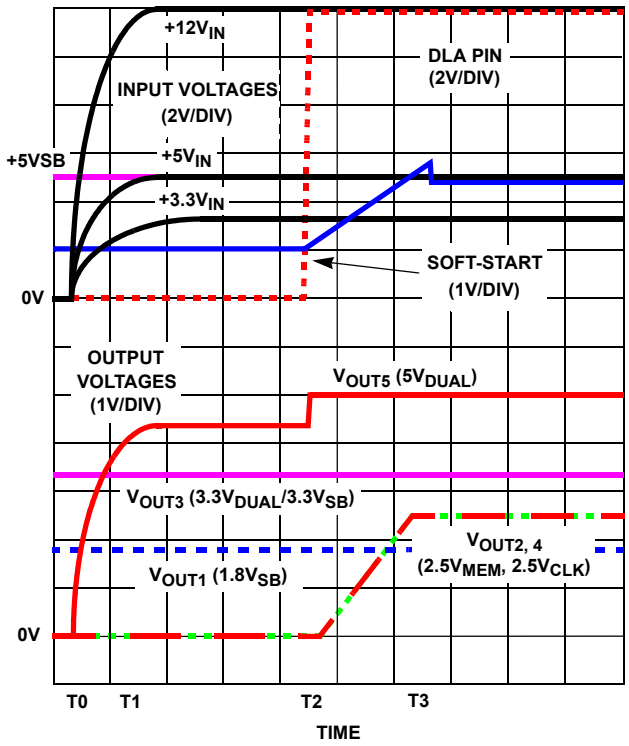


FIGURE 8. SOFT-START INTERVAL IN ACTIVE STATE ($2.5/3.3V_{MEM}$ OUTPUT SHOWN IN 2.5V SETTING)

During sleep to active state transitions from conditions where the outputs are initially 0V (such as S5 to S0 transition on the $5V_{DUAL}$ output with EN5VDL = 0, or simple power-up sequence directly into active state), the memory (in 3.3V setting) and $5V_{DUAL}$ outputs go through a quasi soft-start by being pulled high through the body diodes of the N-Channel MOSFETs connected between these outputs and the 3.3V and 5V ATX outputs. Figure 8 shows this start-up case, exemplifying the $5V_{DUAL}$ output.

5VSB is already present when the main ATX outputs are turned on, at time T0. As a result of $+5V_{IN}$ ramping up, the $5V_{DUAL}$ output capacitors charge up through the body diode of Q5 (see Figure 3). At time T1, all main ATX outputs exceed the HIP6503's undervoltage thresholds, and the internal 25ms (typical) timer is initiated. At T2 the time-out initiates a soft-start, and the 2.5V memory and clock outputs are ramped-up, reaching regulation limits at time T3. Simultaneous with the beginning of the memory and clock voltage ramp-up, at time T2, the DLA pin is pulled high, turning on Q3 and Q5 in the process, and bringing the $5V_{DUAL}$ output in regulation. Shortly after time T3, as the SS voltage reaches 2.75V, the soft-start capacitor is quickly discharged down to approximately 2.45V, where it remains until a valid sleep state request is received from the system.

Fault Protection

All the outputs are monitored against undervoltage events. A severe overcurrent caused by a failed load on any of the outputs, would, in turn, cause that specific output to suddenly drop. If any of the output voltages drops below 80% (typical) of their set value, such event is reported by having the FAULT/MSEL pin pulled to 5V. Additionally, exceeding the maximum current rating of an integrated regulator (output with pass regulator on chip) can lead to output voltage drooping; if excessive, this droop can ultimately trip the under-voltage detector and send a FAULT signal to the computer system.

A FAULT condition occurring on an output when controlled through an external pass transistor will only set off the FAULT flag, and it will not shut off or latch off any part of the circuit. A FAULT condition occurring on an output when controlled through an internal pass transistor, will set off the FAULT flag, and it will shut off the respective faulting regulator only. If shutdown or latch off of the entire circuit is desired in case of a fault, regardless of the cause, this can be achieved by externally pulling or latching the SS pin low. Pulling the SS pin low will also force the FAULT pin to go low and reset any internally latched-off output.

Special consideration is given to the initial start-up sequence. If, following a 5VSB POR event, any of the $1.8V_{SB}$ or $3.3V_{DUAL}/3.3V_{SB}$ outputs is ramped up and is subject to an undervoltage event before the remainder of the controlled voltages have been brought up, then the FAULT output goes high and the entire IC latches off. Latch-off condition can be reset by cycling the bias power ($5V_{SB}$). Undervoltage events on the $1.8V_{SB}$ and the $3.3V_{DUAL}/3.3V_{SB}$ outputs at any other times are handled according to the description found in the second paragraph under the current heading.

Another condition that could set off the FAULT flag is chip over-temperature. If the HIP6503 reaches an internal temperature of 140°C (typical), the FAULT flag is set off, but the chip continues to operate until the temperature reaches 155°C (typical), when unconditional shutdown of all outputs takes place. Operation resumes at 140°C and the temperature cycling occurs until the fault-causing condition is removed.

In HIP6503 applications, loss of any one active ATX output ($3.3V_{IN}$, $5V_{IN}$, or $12V_{IN}$; as detected by the on-board voltage monitors) during active state operation causes the chip to switch to S5 sleep state, in addition to reporting the input UV condition on the FAULT/MSEL pin. Exiting from this forced-S5 state can only be achieved by returning the faulting input voltage above its UV threshold, by resetting the chip through removal of $5V_{SB}$ bias voltage, or by bringing the SS pin at a potential lower than 0.8V.

Output Voltages

The output voltages are internally set and do not require any external components. Selection of the V_{MEM} memory voltage is done by means of an external resistor connected between the FAULT/MSEL pin and ground. An internal 40µA (typical) current source creates a voltage drop across this resistor. Following every $3.3V_{SB}$ ramp-up or chip reset (see Soft-Start Circuit), this voltage is compared with an internal reference and the setting is latched in. Based on this comparison, the output voltage is set at either 2.5V (R_{SEL} = 1kΩ), or 3.3V (R_{SEL} = 10kΩ). It is very important that no capacitor is connected to the FAULT/MSEL pin; the presence of a capacitive element at this pin can lead to false memory voltage selection. See Figure 9 for details.

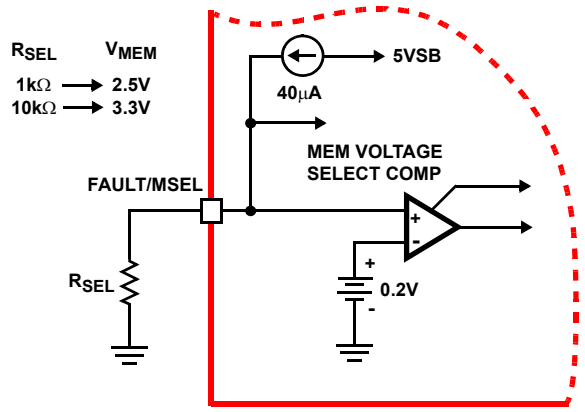


FIGURE 9. 2.5/3.3V_{MEM} OUTPUT VOLTAGE SELECTION CIRCUITRY DETAILS

Application Guidelines

Soft-Start Interval

The 5VSB output of a typical ATX supply is capable of 725mA. During power-up in a sleep state, it needs to provide sufficient current to charge up all the output capacitors and simultaneously provide some amount of current to the output loads. Drawing excessive amounts of current from the 5VSB output of the ATX can lead to voltage collapse and induce a pattern of consecutive restarts with unknown effects on the system's behavior or health.

The built-in soft-start circuitry allows tight control of the slew-up speed of the output voltages controlled by the HIP6503, thus enabling power-ups free of supply drop-off events. Since the outputs are ramped up in a linear fashion, the current dedicated to charging the output capacitors can be calculated with the following formula:

$$I_{COUT} = \frac{I_{SS}}{C_{SS} \times V_{BG}} \times \Sigma(C_{OUT} \times V_{OUT}), \text{ where}$$

I_{SS} - soft-start current (typically 10µA)

C_{SS} - soft-start capacitor

V_{BG} - bandgap voltage (typically 1.26V)

$\Sigma(C_{OUT} \times V_{OUT})$ - sum of the products between the capacitance and the voltage of an output (total charge delivered to all outputs)

Due to the various system timing events, it is recommended that the soft-start interval not be set to exceed 30ms.

Shutdown

In case of a FAULT condition that might endanger the computer system, or at any other time, all the HIP6503 outputs can be shut down by pulling the SS pin below the specified shutdown level (typically 0.8V) with an open drain or open collector device capable of sinking a minimum of 2mA. Pulling the SS pin low effectively shuts down all the pass elements. Upon release of the SS pin, the HIP6503 undergoes a new soft-start cycle and resumes normal operation in accordance to the ATX supply and control pins status.

Layout Considerations

The typical application employing a HIP6503 is a fairly straight forward implementation. Like with any other linear regulator, attention has to be paid to the few potentially sensitive small signal components, such as those connected to sensitive nodes or those supplying critical by-pass current.

The power components (pass transistors) and the controller IC should be placed first. The controller should be placed in a central position on the motherboard, closer to the memory load if possible, but not excessively far from the clock chip or the processor. Insure the 1V8SB, DRV2 and VSEN2 connections are properly sized to carry 250mA without significant resistive losses; similar guideline applies to the VCLK output, which can deliver as much as 800mA (typical). As the current for the VCLK output is provided from the ATX 3.3V, the connection from the 3V3 pin to the 3.3V plane should be sized to carry the maximum clock output current while exhibiting negligible voltage losses. Similarly, the 5VSB and the 5V pins are carrying significant levels of current - for best results, insure they are connected to their respective sources through adequately sized traces. The pass transistors should be placed on pads capable of heatsinking matching the device's power dissipation. Where applicable, multiple via connections to a large internal plane can significantly lower localized device temperature rise.

Placement of the decoupling and bulk capacitors should follow a placement reflecting their purpose. As such, the

high-frequency decoupling capacitors should be placed as close as possible to the load they are decoupling; the ones decoupling the controller close to the controller pins, the ones decoupling the load close to the load connector or the load itself (if embedded). Even though bulk capacitance (aluminum electrolytics or tantalum capacitors) placement is not as critical as the high-frequency capacitor placement, having these capacitors close to the load they serve is preferable.

The critical small signal components include the soft-start capacitor, C_{SS}, as well as the memory selection resistor, R_{SEL}. Locate these components close to the respective pins of the control IC, and connect them to ground through a via placed close to the ground pad. Minimize any leakage current paths from these nodes, since the internal current sources are only 10s of microamperes (10µA to 40µA).

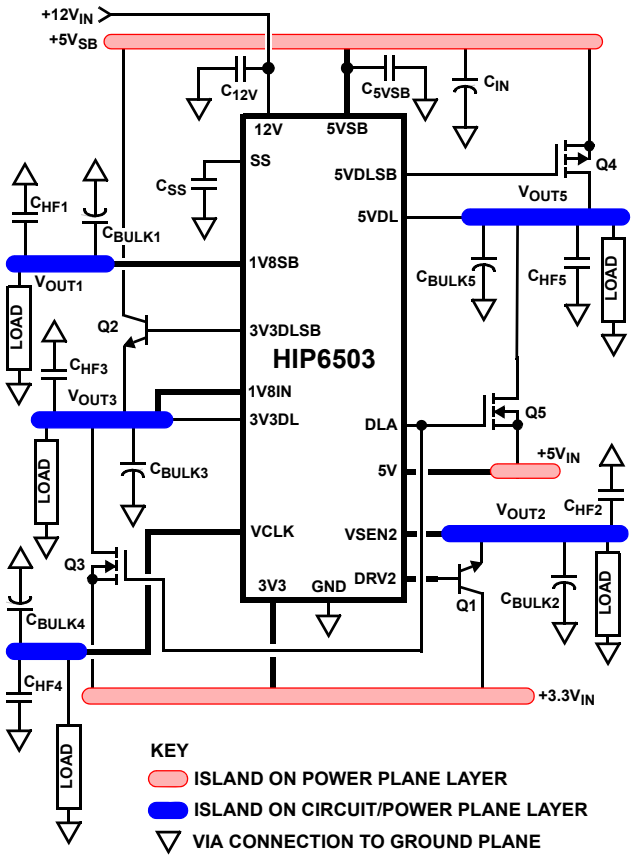


FIGURE 10. PRINTED CIRCUIT BOARD ISLANDS

A multi-layer printed circuit board is recommended. Figure 10 shows the connections of most of the components in the converter. Note that the individual capacitors shown each could represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections through vias placed as close to the component terminal as possible. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Ideally, the power plane should support both the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers to create power islands connecting the filtering components (output capacitors) and the loads. Use the remaining printed circuit layers for small signal wiring.

Component Selection Guidelines

Output Capacitors Selection

The output capacitors for all outputs should be selected to allow the output voltage to meet the dynamic regulation requirements of active state operation (S0, S1). The load transient for the various microprocessor system's components may require high quality capacitors to supply the high slew rate (di/dt) current demands. Thus, it is recommended that the output capacitors be selected for transient load regulation, paying attention to their parasitic components (ESR, ESL).

Also, during the transition between active and sleep states, there is a short interval of time during which none of the power pass elements are conducting - during this time the output capacitors have to supply all the output current. The output voltage drop during this brief period of time can be easily approximated with the following formula:

$$\Delta V_{OUT} = I_{OUT} \times \left(ESR_{OUT} + \frac{t_t}{C_{OUT}} \right), \text{ where}$$

ΔV_{OUT} - output voltage drop

ESR_{OUT} - output capacitor bank ESR

I_{OUT} - output current during transition

C_{OUT} - output capacitor bank capacitance

t_t - active-to-sleep or sleep-to-active transition time (10µs typ.)

The output voltage drop is heavily dependent on the ESR (equivalent series resistance) of the output capacitor bank, the choice of capacitors should be such as to maintain the output voltage above the lowest allowable regulation level.

V_{CLK} (V_{OUT4}) Output Capacitors Selection

The output capacitor for the V_{CLK} linear regulator provides loop stability. Figure 11 outlines a capacitance vs. equivalent series resistance envelope. For stable operation and optimized performance, select a C_{OUT4} capacitor or combination of capacitors with characteristics within the shown envelope.

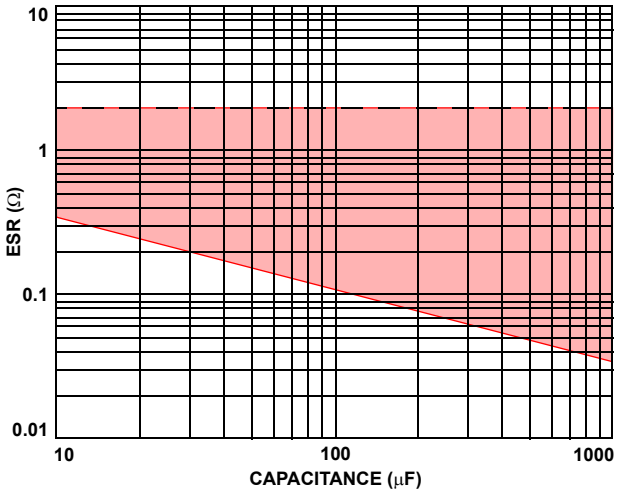


FIGURE 11. C_{OUT4} OUTPUT CAPACITOR

Input Capacitors Selection

The input capacitors for an HIP6503 application have to have a sufficiently low ESR as to not allow the input voltage to dip excessively when energy is transferred to the output capacitors. If the ATX supply does not meet the specifications, certain imbalances between the ATX's outputs and the HIP6503's regulation levels could have as a result a brisk transfer of energy from the input capacitors to the supplied outputs. At the transition between active and sleep states, this phenomena could result in the 5VSB voltage drooping excessively and affecting the output regulation. The solution to a potential problem such as this is using larger input capacitors with a lower total combined ESR.

Transistor Selection/Considerations

The HIP6503 usually requires one P-Channel (or bipolar PNP), two N-Channel MOSFETs and two bipolar NPN transistors.

One important criteria for selection of transistors for all the linear regulators/switching elements is package selection for efficient removal of heat. The power dissipated in a linear regulator/switching element is

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the rating with the maximum expected ambient temperature.

Q1

The active element on the $2.5V_{MEM}$ output has to be a bipolar NPN capable of conducting the maximum active memory current and exhibit a current gain (h_{fe}) of minimum 40 at this current and 0.7V V_{CE}.

Q2

The NPN transistor used as sleep state pass element (Q2) on the $3.3V_{DUAL}$ output has to have a minimum current gain of 100 at 1.5V V_{CE} and 500mA I_{CE} throughout the in-circuit operating temperature range.

Q3, 4, Q2 in $3.3V_{MEM}$ configuration

These N-Channel MOSFETs are used to switch the 3.3V and 5V inputs provided by the ATX supply into the $3.3V_{MEM}$, $3.3V_{DUAL}$/$3.3V_{SB}$, and $5V_{DUAL}$ outputs, while in active (S0, S1) state. The main criteria for the selection of these transistors is output voltage budgeting. The maximum $r_{DS(ON)}$ allowed at highest junction temperature can be expressed with the following equation:

$$r_{DS(ON)max} = \frac{V_{INmin} - V_{OUTmin}}{I_{OUTmax}}, \text{ where}$$

V_{INmin} - minimum input voltage

V_{OUTmin} - minimum output voltage allowed

I_{OUTmax} - maximum output current

The gate bias available for these MOSFETs is of the order of 8V.

Q5

If a P-Channel MOSFET is used to switch the 5VSB output of the ATX supply into the $5V_{DUAL}$ output during S3 and S5 states (as dictated by EN5VDL status), then the selection criteria of this device is proper voltage budgeting. The maximum $r_{DS(ON)}$, however, has to be achieved with only 4.5V of V_{GS}, so a logic level MOSFET needs to be selected. If a PNP device is chosen to perform this function, it has to have a low saturation voltage while providing the maximum sleep current and have a current gain sufficiently high to be saturated using the minimum drive current (typically 20mA).

HIP6503 Application Circuit

Figure 12 shows an application circuit of an ACPI-sanctioned power management system for a microprocessor computer system. The power supply provides the $3.3V_{DUAL}/3.3V_{SB}$ voltage (V_{OUT3}), the ICH2 resume well $1.8V_{SB}$ voltage (V_{OUT1}), the RDRAM $2.5V_{MEM}$ memory voltage (V_{OUT2}), the $2.5V_{CLK}$ clock voltage (V_{OUT4}), and the $5V_{DUAL}$ voltage (V_{OUT5}) from +3.3V, +5VSB, +5V, and +12VDC ATX supply outputs. Q4 can also be a PNP, such as an MMBT2907AL. For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note AN9901.

Also see Intersil Corporation's web page (www.intersil.com) or call 1 888-INTERSIL for the latest information.

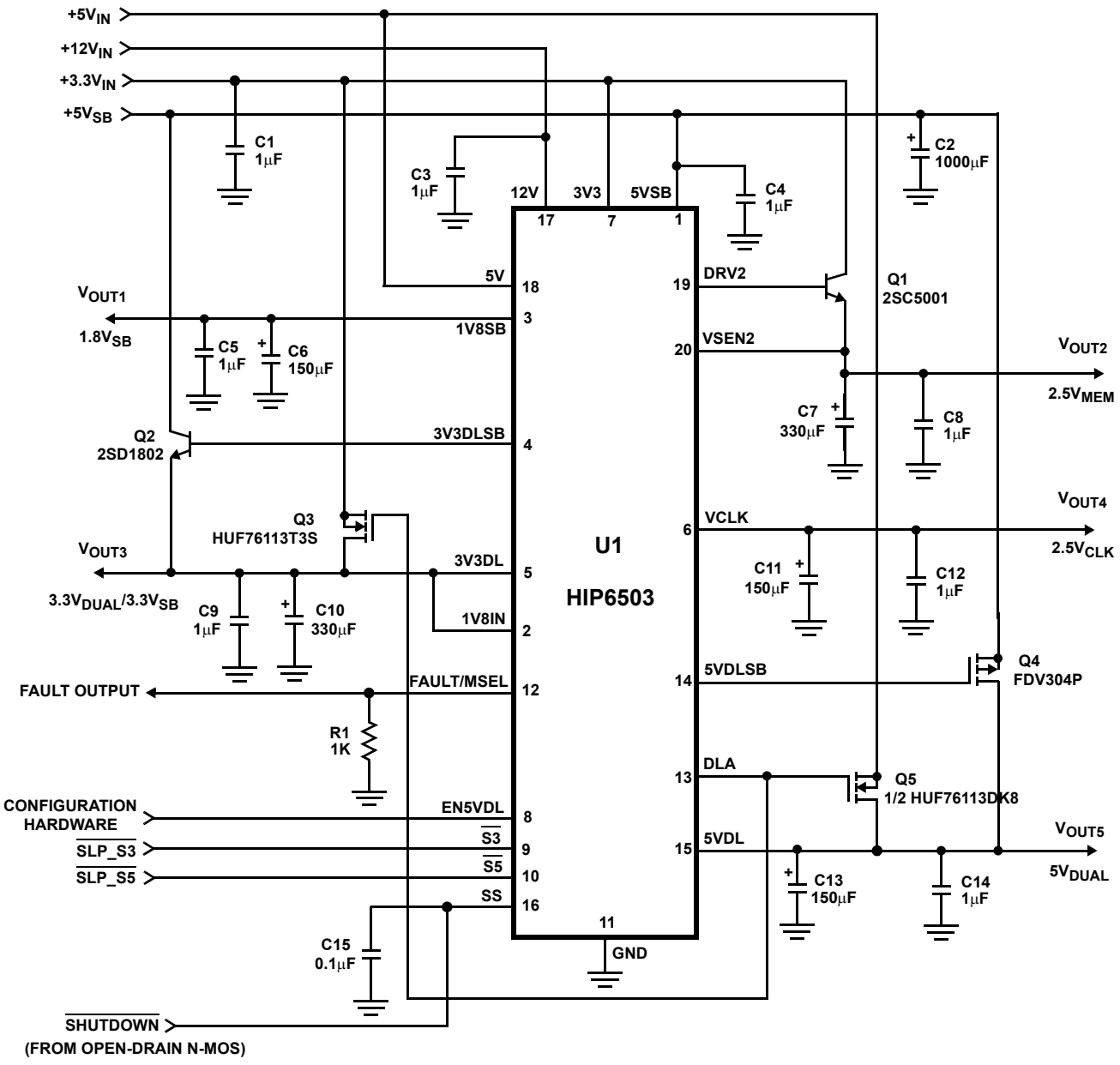
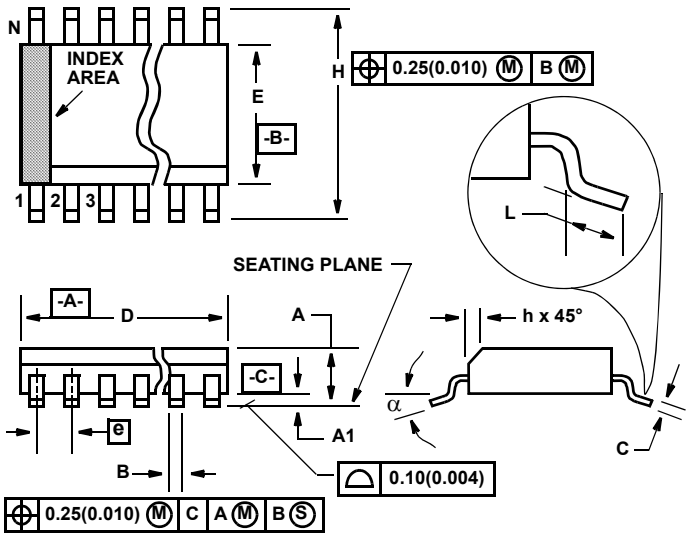


FIGURE 12. TYPICAL HIP6503 APPLICATION DIAGRAM

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.