

**FEATURES:**

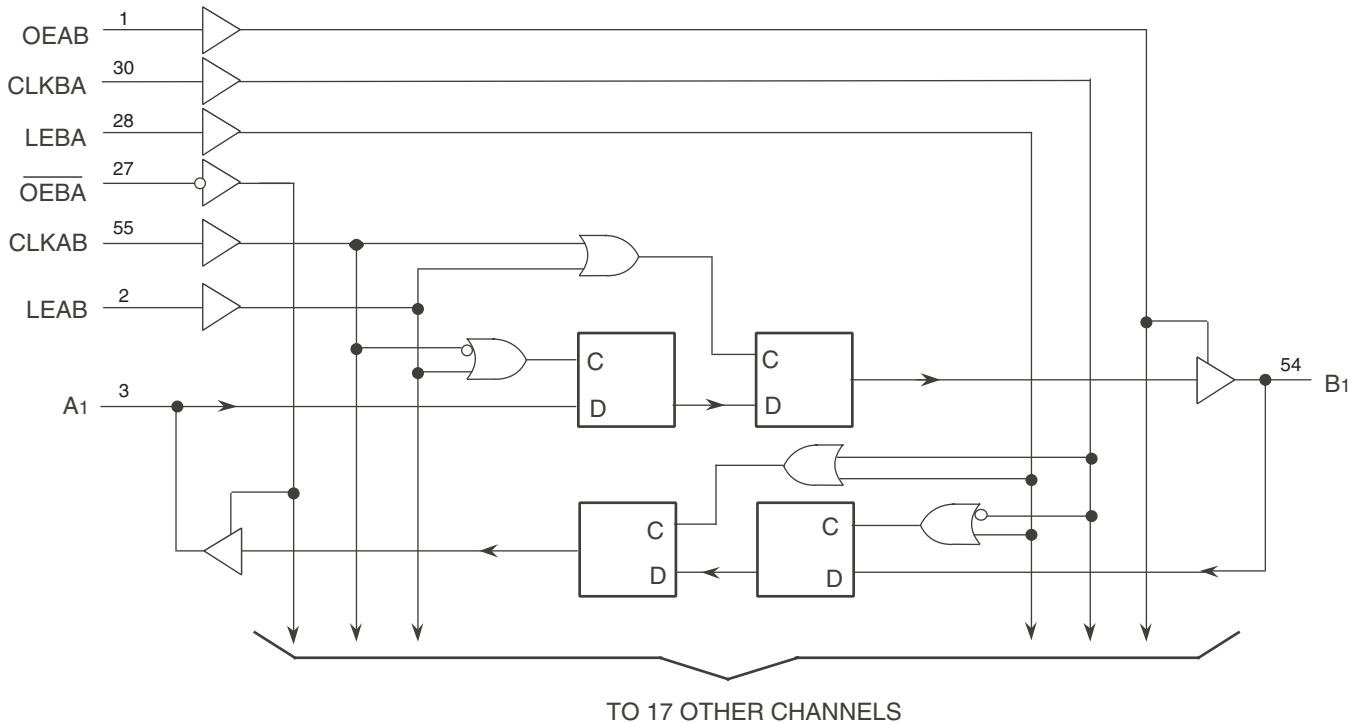
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Balanced Output Drivers ( $\pm 24mA$ )
- Reduced system switching noise
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.6V at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- Available in SSOP and TSSOP packages

**DESCRIPTION:**

The FCT162501T 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. OEAB is the output enable for the B port. Data flow from the B port to the A port is similar but requires using  $\overline{OEBA}$ , LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

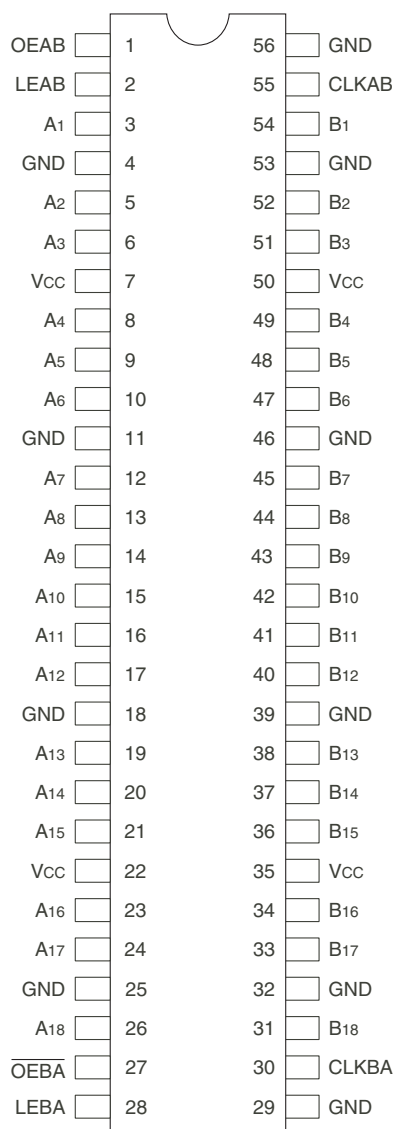
The FCT162501T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162501T is a plug-in replacement for the FCT16501T and ABT16501 for on-board bus interface applications.

**FUNCTIONAL BLOCK DIAGRAM**



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

## PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

## PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

## CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COU	Output Capacitance	VOU = 0V	3.5	8	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## FUNCTION TABLE<sup>(1, 4)</sup>

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B <sup>(2)</sup>
H	L	H	X	B <sup>(3)</sup>

### NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-impedance  
↑ = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>		$V_I = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	5	500	$\mu\text{A}$

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$		60	115	200	mA
$I_{ODH}$	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -24\text{mA}$	2.4	3.3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 24\text{mA}$	—	0.3	0.55	V

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $OEAB = \overline{OEBA} = V_{CC} \text{ or GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A/$ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz (CLKAB)}$ 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ LEAB = GND One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz (CLKAB)}$ 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ LEAB = GND Eighteen Bit Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.5	20.8 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

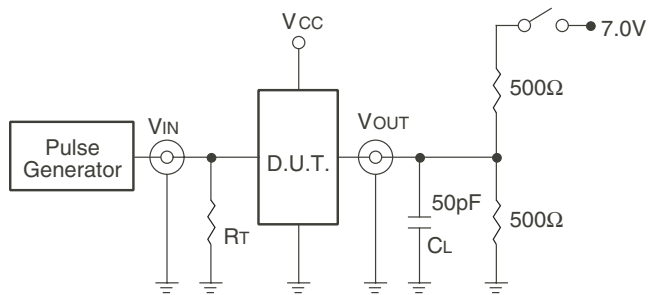
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	74FCT162501AT		74FCT162501CT		Unit	
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.		
f <sub>MAX</sub>	CLKAB or CLKBA frequency <sup>(4)</sup>	CL = 50pF RL = 500Ω	—	150	—	150	MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ax to Bx or Bx to Ax		1.5	5.1	1.5	4.3	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	4.4	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	4.4	ns	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx		1.5	6	1.5	4.8	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx		1.5	5.6	1.5	5.2	ns	
t <sub>SU</sub>	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		3	—	2.4	—	ns	
t <sub>H</sub>	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	ns	
t <sub>SU</sub>	Set-up Time, HIGH or LOW Ax to LEAB, Bx to LEBA		Clock LOW	3	—	2	—	ns
			Clock HIGH	1.5	—	1.5	—	ns
t <sub>H</sub>	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	0.5	—	ns	
t <sub>w</sub>	LEAB or LEBA Pulse Width HIGH <sup>(4)</sup>		3	—	3	—	ns	
t <sub>w</sub>	CLKAB or CLKBA Pulse Width HIGH or LOW <sup>(4)</sup>		3	—	3	—	ns	
t <sub>SK(o)</sub>	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	ns	

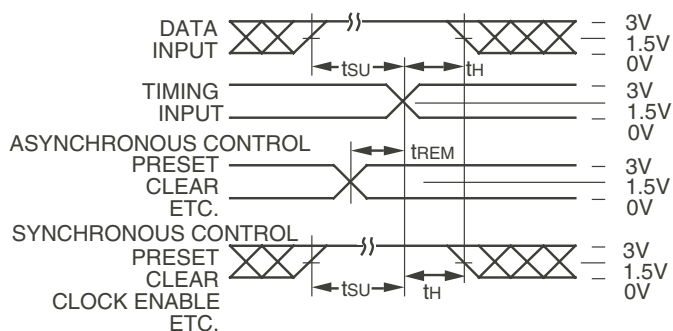
**NOTES:**

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

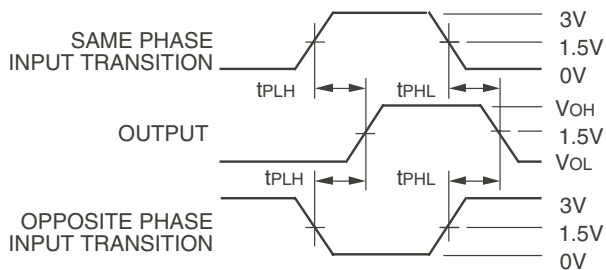
## TEST CIRCUITS AND WAVEFORMS



Test Circuits For all Outputs



Set-up, Hold, and Release Times



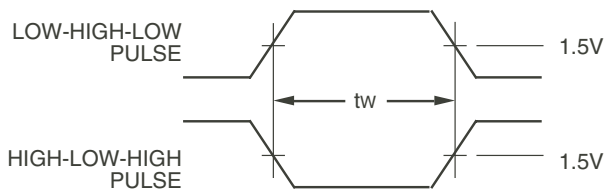
Propagation Delay

## SWITCH POSITION

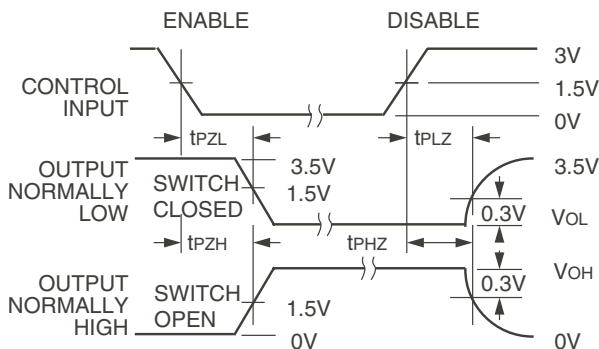
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
Rt = Termination resistance: should be equal to Zout of the Pulse Generator.



Pulse Width

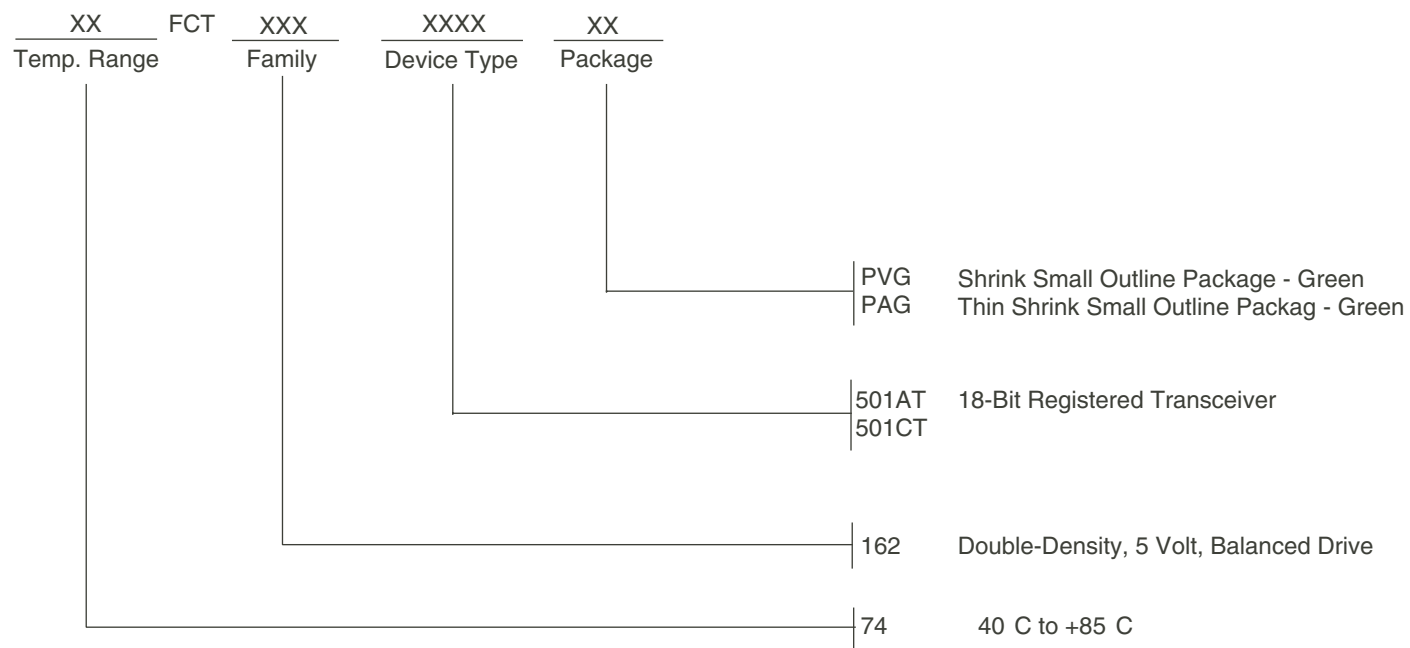


Enable and Disable Times

### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $t_f \leq$  2.5ns;  $t_r \leq$  2.5ns.

## ORDERING INFORMATION



## Datasheet Document History

09/06/09 Pg.6 Updated the ordering information by removing the "IDT" notation and non RoHS part.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.