ISL95338

Bidirectional Buck-Boost Voltage Regulator

The ISL95338 is a bidirectional, buck-boost voltage regulator that provides buck-boost voltage regulation and protection features. The Renesas advanced R3™ Technology provides high light-load efficiency, fast transient response, and seamless DCM/CCM transitions.

The ISL95338 takes input power from a wide range of DC power sources (such as conventional AC/DC ADPs, USB PD ports, and travel ADPs) and safely converts it to a regulated voltage up to 20V. The ISL95338 can also convert a wide range DC power source connected at its output (system side) to a regulated voltage to its input (ADP side). This bidirectional buck-boost regulation feature makes its application very flexible.

The ISL95338 includes various system operation functions such as Forward mode enable, Reverse mode enable, programmable soft-start time, and adjustable V_{OUT} in both the forward direction and reverse direction. The protection functionalities include OCP, OVP, UVP, and OTP.

The ISL95338 has serial communication through SMBus/I^2C that allows programming of many critical parameters to deliver a customized solution. These programming parameters include, but are not limited to: output current limit, input current limit, and output voltage setting.

Related Literature

For a full list of related documents, visit our website:

- ISL95338 device page

Features

- Bidirectional buck, boost, and buck-boost operation
- Input voltage range: 3.8V to 24V (no dead zone)
- Output voltage: up to 20V
- Up to 1MHz switching frequency
- Programmable soft-start time
- LDO output for VDD and VDDP
- System status alert function
- Bidirectional internal discharge function
- Active switching for negative voltage transitions
- Bypass mode in both directions
- Forward mode enable, Reverse mode enable
- OCP, OVP, UVP, and OTP protection
- SMBus and auto-increment I^2C compatible
- Pb-free (RoHS compliant)
- 32 Ld 4x4 TQFN Package

Applications

- Tablets, Ultrabooks, power banks, mobile devices, and USB-C

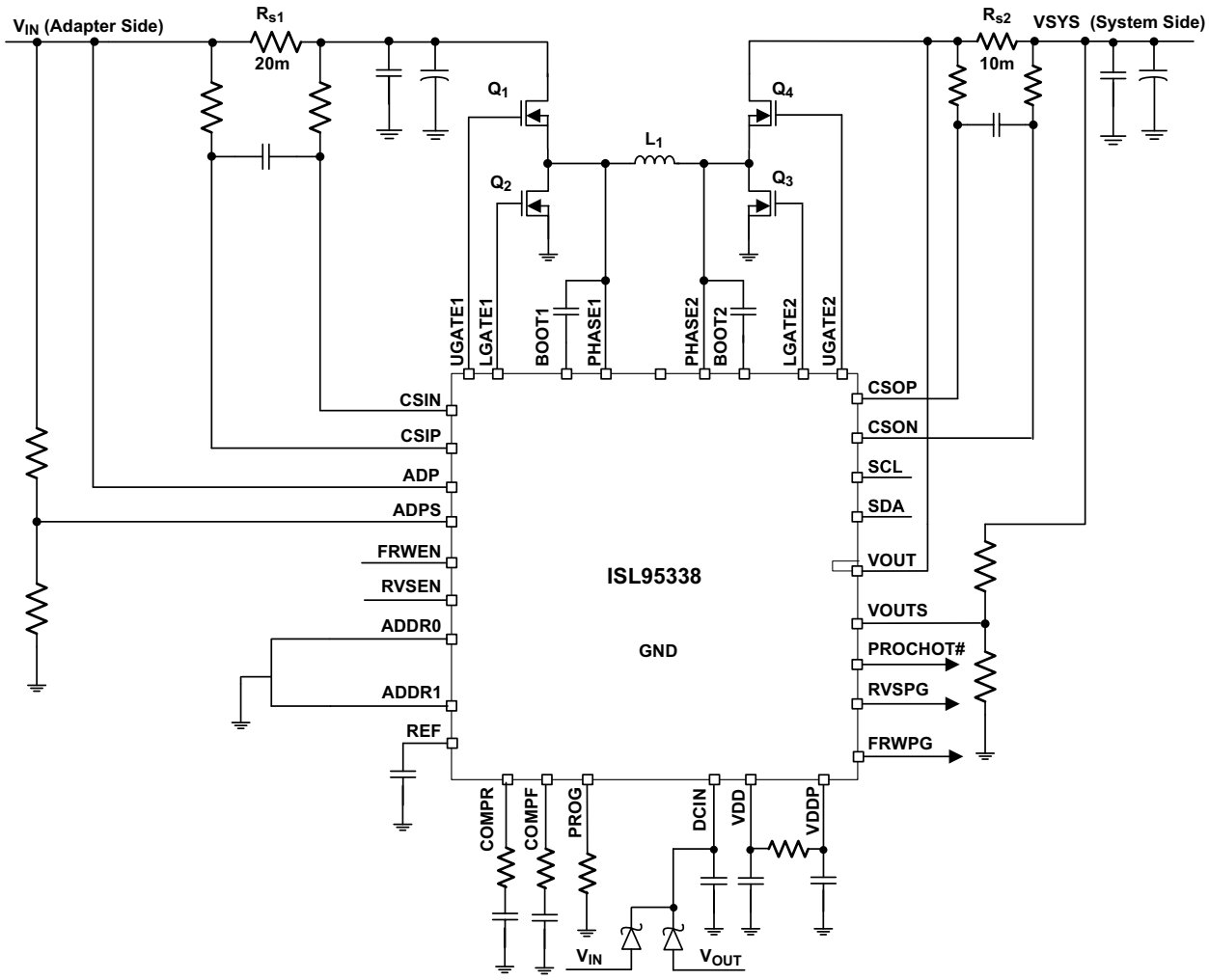


Figure 1. Typical Application Circuit

Contents

1. Overview

1.1 Block Diagram

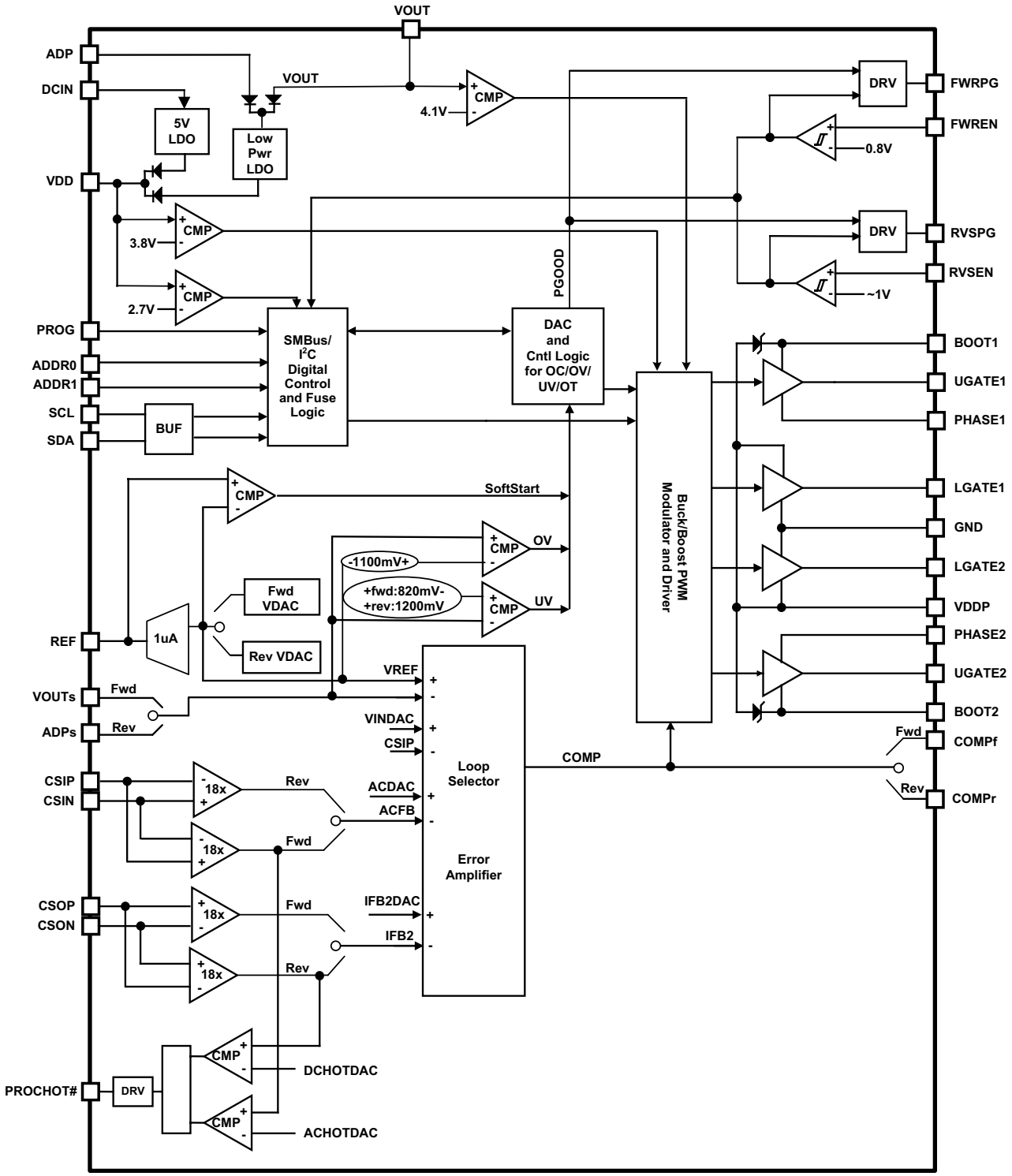


Figure 2. Block Diagram

1.2 Simplified Application Circuit

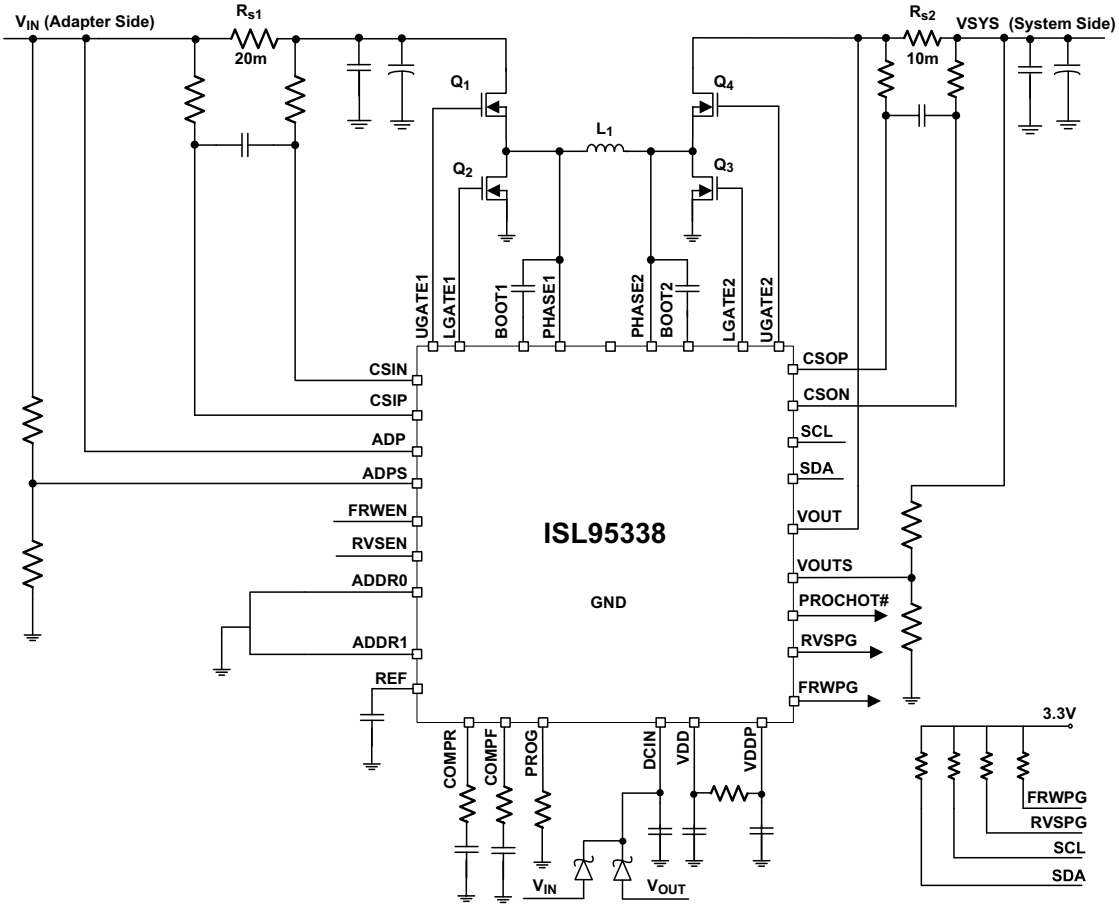


Figure 3. Simplified Application Diagram

1.3 Ordering Information

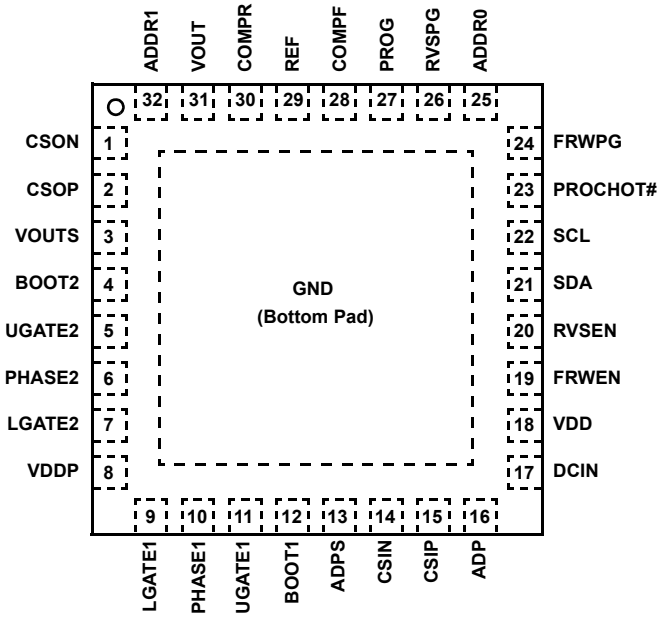
Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL95338HRTZ	95338H	-10 to +100	-	32 Ld 4x4 TQFN	L32.4x4D
ISL95338HRTZ-T	95338H	-10 to +100	6k	32 Ld 4x4 TQFN	L32.4x4D
ISL95338HRTZ-TK	95338H	-10 to +100	1k	32 Ld 4x4 TQFN	L32.4x4D
ISL95338HRTZ-T7A	95338H	-10 to +100	250	32 Ld 4x4 TQFN	L32.4x4D
ISL95338IRTZ	95338I	-40 to +100	-	32 Ld 4x4 TQFN	L32.4x4D
ISL95338IRTZ-T	95338I	-40 to +100	6k	32 Ld 4x4 TQFN	L32.4x4D
ISL95338IRTZ-TK	95338I	-40 to +100	1k	32 Ld 4x4 TQFN	L32.4x4D
ISL95338EVAL1Z	Evaluation board				

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL95338 device page. For more information about MSL, see TB363.

1.4 Pin Configuration

32 Ld 4x4 TQFN
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Description
BOTTOM PAD	GND	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin. GND should also be used as the thermal pad for heat dissipation.
1	CSON	Forward V_{OUT} current sense “-” input. Connect to the VOUT current resistor negative input. Place a 0.1µF ceramic capacitor between CSOP and CSON to provide differential mode filtering.
2	CSOP	Forward V_{OUT} current sense “+” input. Connect to the VOUT current resistor positive input. Place a 0.1µF ceramic capacitor between CSOP and CSON to provide differential mode filtering.
3	VOUTS	Forward VSYS feedback voltage. Use a resistor divider externally to configure the forward VSYS voltage.
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 pin and the PHASE2 pin. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT2 pin when the PHASE2 pin drops below VDDP minus the voltage drop across the internal boot diode.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain, and one terminal of the inductor.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply for the gate drivers. Connect to the VDD pin through a 4.7Ω resistor and connect a 2.2µF ceramic capacitor to GND. The effective capacitance at 5V must be at least 0.4µF after derating.
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain, and the input terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 pin and the PHASE1 pin. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT1 pin when the PHASE1 pin drops below VDDP minus the voltage drop across the internal boot diode.
13	ADPS	Reverse output voltage feedback. Use a resistor divider externally to configure the reverse output voltage.
14	CSIN	ADP current sense “-” input.
15	CSIP	ADP current sense “+” input. The modulator also uses this pin to sense the input voltage in Forward mode and output voltage in Reverse mode.

Pin Number	Pin Name	Description
16	ADP	Senses ADP voltage. When the ADP voltage is higher than 4.1V, Forward mode can be enabled. The ADP pin is also one of the two internal low power LDO inputs.
17	DCIN	Internal LDO input that provides power to the IC. Connect a diode OR from ADP and the system outputs. Connect a 4.7µF ceramic capacitor to GND. The effective capacitance at 20V must be at least 0.4µF after derating.
18	VDD	Internal LOD output; provides the bias power for the internal analog and digital circuit Connect a 2.2µF ceramic capacitor to GND. The effective capacitance at 5V must be at least 0.4µF after derating. If VDD is pulled below 2.7V, the ISL95338 resets all the SMBus register values to the default.
19	FRWEN	Forward mode enable, analog signal input. Forward mode is valid if the FRWEN pin voltage is greater than 0.8V.
20	RVSEN	Reverse mode enable, digital signal input. Reverse mode is valid if the signal is “1” (logic high), otherwise, Reverse mode is disabled.
21	SDA	SMBus data I/O. Connect to the data line from the host controller. Connect a 10k pull-up resistor according to the SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller. Connect a 10k pull-up resistor according to the SMBus specification.
23	PROCHOT#	Open-drain output. Pulled low when input current is detected as hot in Forward and Reverse mode. SMBus command to pull low (see Table 8 on page 25 and Table 10 on page 27 for Control 2 Register 0x3DH and Control4 Register 0x4EH).
24	FRWPG	Open-drain output. Indicator output to indicate the forward modulator is enabled.
25	ADDR0	Address setting pin for the IC. The IC address is set by the ADDR0 and ADDR1 logic voltage levels.
26	RVSPG	Open-drain output. Indicator output to indicate the reverse modulator is enabled.
27	PROG	A resistor from the PROG pin to GND sets the default forward system output voltage.
28	COMPF	Forward mode error amplifier output. Connect a compensation network externally from COMPF to GND.
29	REF	Output voltage soft-start reference. A ceramic capacitor from REF to GND is set to the desired soft-start time. In Forward mode, forward output voltage (VOUTS) reference soft-start time is set. In Reverse mode, reverse output voltage (ADPS) reference soft-start time is set.
30	COMPR	Reverse mode error amplifier output. Connect a compensation network externally from COMPR to GND.
31	VOUT	Forward V_{OUT} sense voltage for the modulator and PHASE 2 zero-current comparator.
32	ADDR1	Address setting pin for the IC. The IC address is set by the ADDR0 and ADDR1 logic voltage levels.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
CSIP, CSIN, DCIN, ADPS, ADP	-0.3	+30	V
CSIP	0.3	ADP + 2	V
PHASE1	GND - 0.3	+30	V
PHASE1	GND - 2 (<20ns)	+30	V
UGATE1	PHASE1 - 0.3	BOOT1 + 0.3	V
PHASE2	GND - 0.3	+30	V
PHASE2	GND - 2 (<20ns)	+30	V
UGATE2	PHASE2 - 0.3	BOOT2 + 0.3	V
LGATE1, LGATE2	GND - 0.3	VDDP + 0.3	V
LGATE1, LGATE2	GND - 2 (<20ns)	VDDP + 0.3	V
VOUT, VOUTS, CSOP, CSON	-0.3	+24	V
VDD, VDDP	-0.3V	+6.5	V
BOOT1, BOOT2	- 0.3	VDDP + 25	V
BOOT1	(PHASE1 - 0.3)	PHASE1 + 6.5	V
BOOT2	(PHASE2 - 0.3)	PHASE2 + 6.5	V
BOOT1-PHASE1, BOOT2-PHASE2	-0.3	+6.5	V
COMPR, COMPF, REF, PROG	-0.3	+6.5	V
RVSEN, FRWEN, ADDR0, ADDR1	-0.3	+6.5	V
FRWPG, PROCHOT#, RVSPG	-0.3	+6.5	V
SCL, SDA	-0.3	+6.5	V
CSIP-CSIN, CSOP-CSON	-0.3	+0.3	V
RVSEN, FRWEN, SDA, SCL, FRWPG, RVSPG, PROCHOT#		2	mA
ESD Rating	**Rating**		**Unit**
Human Body Model (Tested per JS-001-2014)	2		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld TQFN Package (Notes 4, 5)	37	2

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
5. For θ_{JC}, the “case temp” location is the center of the ceramic on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature Range (T_J)	-10	+125	°C
Storage Temperature Range (T_S)	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature - HRTZ	-10	+100	°C
Ambient Temperature - IRTZ	-40	+100	°C
ADP Input Voltage	+4	+24	V
V_{OUT} Input Voltage	+4	+20	V

2.4 Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 4V and 23V, VOUTS = VOUT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
UVLO/ACOK						
VADP UVLO Rising	VADP_UVLO_r		**3.9**	4.2	**4.55**	V
VADP UVLO Hysteresis	VADP_UVLO_h			530		mV
V_{OUT} UVLO Rising	VOUT_UVLO_r		**3.9**	4.2	**4.55**	V
V_{OUT} UVLO Hysteresis	VOUT_UVLO_h			300		mV
VDDA 2P7 Rising, SMBus Active (Note 7)	VDD_2P7_r		**2.5**	2.7	**2.9**	V
VDDA 2P7 POR Hysteresis (Note 7)	VDD_2P7_h			150		mV
VDDA 3P8 POR Rising, Modulator, and Gate Driver Active	VDD_3P8_r		**3.6**	3.8	**3.9**	V
VDD 3P8 Hysteresis	VDD_3P8_h			150		mV
FRWEN Rising	FRWEN_r		**0.775**	0.8	**0.825**	V
FRWEN Hysteresis	FRWEN_h			50		mV
Bias Current						
Forward Supply Current, Disable State		ADP, ADPS CSIN, CSIP, VDDP, DCIN = 5V, FWREN = Low		130	**200**	µA
Reverse Supply Current, Disable State		V_{OUT}, VOUTS CSON, CSOP, VDDP, DCIN = 5V, RVSEN = Low		70	**150**	µA
Forward Supply Current, Enable State		ADP, ADPS CSIN, CSIP, DCIN = 20V, FWREN = High		3000	**3300**	µA
Reverse Supply Current, Enable State		VOUT, VOUTS CSON, CSOP, DCIN = 20V, RVSEN = High		3000	**3300**	µA
Forward Supply Current, Enable State		DCIN only (does not include gate driver current)		1600	**2000**	µA
Reverse Supply Current, Enable State		DCIN only (does not include gate driver current)		1600	**2000**	µA
Linear Regulator						
VDDA Output Voltage	VDD	6V < V_{ADP} < 23V, no load	**4.5**	5.1	**5.5**	V
VDDA Dropout Voltage	VDD_dp	30mA, V_{DCIN} = 4V		100		mV
VDD Overcurrent Threshold	VDD_OC		**90**	135	**165**	mA
ADP Current Regulation, R_{ADP} = 20mΩ						
Input Current Accuracy		|CSIP - CSIN| = 80mV		4		A
			-3		**+3**	%
		|CSIP - CSIN| = 40mV		2		A
			-4		**+4**	%
		|CSIP - CSIN| = 10mV		0.5		A
			-10		**+10**	%

Operating conditions: ADP = CSIP = CSIN = 4V and 23V, VOUTS = VOUT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
ADP Current PROCHOT# Threshold R_{s1} = 20mΩ	$I_{ADP\_HOT\_TH10}$	ACProchot = 0x0A80H (2688mA)		2688		mA
			-3.0		**+3.0**	%
		ACProchot = 0x0400H (1024mA)		1024		mA
			-6.0		**+6.0**	%
Voltage Regulation						
Output Voltage Accuracy Forward (HRTZ)		Measured at VOUTS, 8V and up	**-1**		**+1**	%
		Measured at VOUTS, 4V to 8V	**-1.5**		**+1.5**	%
Output Voltage Accuracy Reverse (HRTZ)		Measured at ADPS, 8V and up	**-1**		**+1**	%
		Measured at ADPS, 4V to 8V	**-1.5**		**+1.5**	%
Output Voltage Accuracy Forward (IRTZ)		Measured at VOUTS, 8V and up	**-2**		**+2**	%
		Measured at VOUTS, 4V to 8V	**-1.5**		**+1.5**	%
Output Voltage Accuracy Reverse (IRTZ)		Measured at ADPS, 8V and up	**-2**		**+2**	%
		Measured at ADPS, 4V to 8V	**-3**		**+3**	%
Minimum Input Voltage Accuracy		Measured at ADPS	**-3**		**+3**	V
V_{OUT} Current Regulation, R_{s2} = 10mΩ						
V_{OUT} Current Accuracy		|CSOP - CSON| = 60mV		6		A
			-3		**+3**	%
		|CSOP - CSON| = 20mV		2		A
			-5		**+5**	%
		|CSOP - CSON| = 10mV		1		A
			-10		**+10**	%
		|CSOP - CSON| = 5mV		0.5		A
			-20		**+20**	%
ADP Current-Sense Amplifier, R_{ADP} = 20mΩ						
CSIP/CSIN Input Voltage Range	$V_{CSIP/N}$		**0**		**27**	V
V_{OUT} Current-Sense Amplifier, R_{BAT} = 10mΩ						
System Side Current PROCHOT# Threshold, R_{s2} = 10mΩ	I_{SYS_HOT}	SystemSideProchot = 0x1000H (4096mA)		4096		mA
			-5		**+5**	%
RVSEN						
High-Level Input Voltage			**0.9**			V
Low-Level Input Voltage					**0.35**	V
Input Leakage Current		V_{RVSEN} = 3.3V, 5V			**1**	µA
PROCHOT#, RVSPG, FWRPG						
Output Sinking Current		Pin at 0.4V		37		mA
Leakage Current					**1**	µA
PROCHOT#						
PROCHOT# Debounce Time (Note 7)		PROCHOT# Debounce register	**-15**		**15**	%
PROCHOT# Duration Time (Note 7)		PROCHOT# Duration register	**-15**		**15**	%
Protection						
ADP Overvoltage Rising Hysteresis		Forward mode	**25.5**	26.4	**27**	V
ADP Overvoltage Hysteresis				0.35		V
VOUTS Overvoltage Rising Threshold		Forward mode VOUTS-12xREF	**0.85**	1.1	**1.45**	V
VOUTS Overvoltage Hysteresis				0.55		V
ADPS Overvoltage Rising Threshold		Reverse mode ADPS-12xREF	**0.9**	1.2	**1.5**	V
ADPS Overvoltage Hysteresis				0.6		V

Operating conditions: ADP = CSIP = CSIN = 4V and 23V, VOUTS = VOUT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
VOUTS Undervoltage Falling Threshold		Forward mode VOUTS-12xREF	**-1.15**	-0.85	**-0.55**	V
VOUTS Undervoltage Hysteresis				0.6		V
ADPS Undervoltage Falling Threshold		Reverse mode ADPS-12xREF	**-1.55**	-1.2	**-0.85**	V
ADPS Undervoltage Hysteresis				0.4		V
Over-Temperature Threshold (Note 7)			**140**	150	**160**	°C
Oscillator						
Oscillator Frequency, Digital Core Only			**0.85**	1	**1.15**	MHz
Digital Debounce Time Accuracy		PV Debounce and UV Debounce for FWRPG and RVSPG delay	**-15**		**15**	%
Miscellaneous						
Switching Frequency Accuracy		All programmed f_{SW} settings, CCM, and no period stretching	**-15**		**15**	%
ADP Discharge Current		ADP = 5V		6.5		mA
V_{OUT} Discharge Current		V_{OUT} = 5V		8.5		mA
REF Pin Sink/Source Current		Control1 <3> = 0		0.7		µA
REF Pin Fast Sink Current		Control1 <3> = 1		0.7		µA
REF Pin Fast Source Current		Control1 <3> = 1		14		µA
SMBus						
SDA/SCL Input Low Voltage		3.3V			**0.8**	V
SDA/SCL Input High Voltage		3.3V	**2**			V
SDA/SCL Input Bias Current		3.3V			**1**	µA
SDA, Output Sink Current (Note 7)		SDA = 0.4V	**4**			mA
SMBus Frequency	f_{SMB}		**10**		**400**	kHz
Gate Driver						
UGATE1 Pull-Up Resistance	$UG1_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE1 Source Current	$UG1_{SRC}$	UGATE1 - PHASE1 = 2.5V	**1.3**	2		A
UGATE1 Pull-Down Resistance	$UG1_{RPD}$	100mA sink current		350	**475**	mΩ
UGATE1 Sink Current	$UG1_{SNK}$	UGATE1 - PHASE1 = 2.5V	**1.9**	2.8		A
LGATE1 Pull-Up Resistance	$LG1_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE1 Source Current	$LG1_{SRC}$	LGATE1 - GND = 2.5V	**1.3**	2		A
LGATE1 Pull-Down Resistance	$LG1_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE1 Sink Current	$LG1_{SNK}$	LGATE1 - GND = 2.5V	**2.3**	3.5		A
LGATE2 Pull-Up Resistance	$LG2_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE2 Source Current	$LG2_{SRC}$	LGATE2 - GND = 2.5V	**1.3**	2		A
LGATE2 Pull-Down Resistance	$LG2_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE2 Sink Current	$LG2_{SNK}$	LGATE2 - GND = 2.5V	**2.3**	3.5		A
UGATE2 Pull-Up Resistance	$UG2_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE2 Source Current	$UG2_{SRC}$	UGATE2 - PHASE2 = 2.5V	**1.3**	2		A
UGATE2 Pull-Down Resistance	$UG2_{RPD}$	100mA sink current		300	**450**	mΩ
UGATE2 Sink Current	$UG2_{SNK}$	UGATE2 - PHASE2 = 2.5V	**2.3**	3.5		A
UGATE1 to LGATE1 Dead Time	$t_{UG1LG1DEAD}$		**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	$t_{LG1UG1DEAD}$		**10**	20	**40**	ns
LGATE2 to UGATE2 Dead Time	$t_{LG2UG2DEAD}$		**10**	20	**40**	ns
UGATE2 to LGATE2 Dead Time	$t_{UG2LG2DEAD}$		**10**	20	**40**	ns

2.5 SMBus Timing Specification

Parameters	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
SMBus Frequency	F_{SMB}		10		400	kHz
Bus-Free Time	t_{BUF}		4.7			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
Start Condition Set-Up Time from SCL	$t_{SU:STA}$		4.7			µs
Stop Condition Set-Up Time from SCL	$t_{SU:STO}$		4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Set-Up Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Period	t_{LOW}		4.7			µs
SCL High Period	t_{HIGH}		4			µs
SMBus Inactivity Timeout		Maximum charging period without an SMBus Write to MaxSystemVoltage or ADPCurrent register		175		s

Notes:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

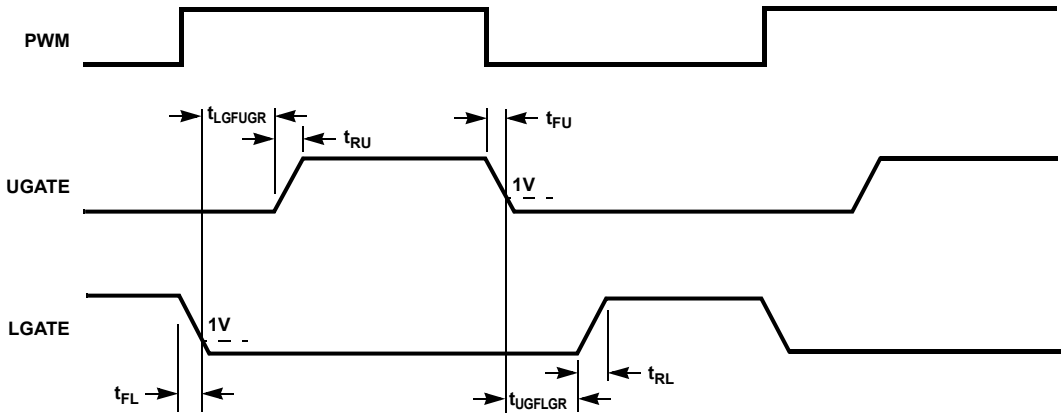


Figure 4. Gate Driver Timing Diagram

3. Typical Performance Curves

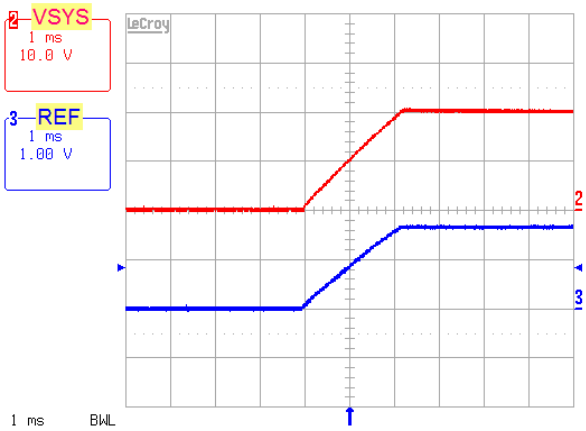


Figure 5. Forward Mode Soft-Start, $12V_{ADP}$, $20V_{SYS}$

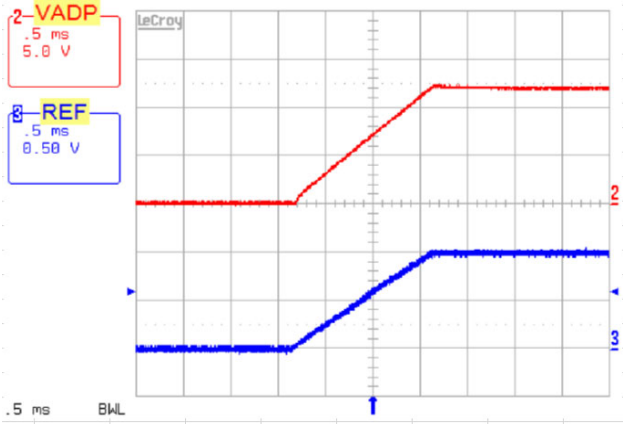


Figure 6. Reverse Mode, Soft-Start, $12V_{ADP}$, $5V_{SYS}$

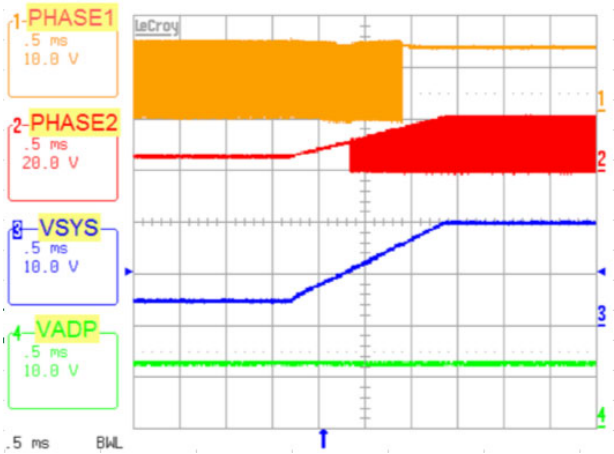


Figure 7. V_{SYS} Voltage Ramps Up in Forward Mode, Buck -> Buck-Boost -> Boost Operation Mode Transition

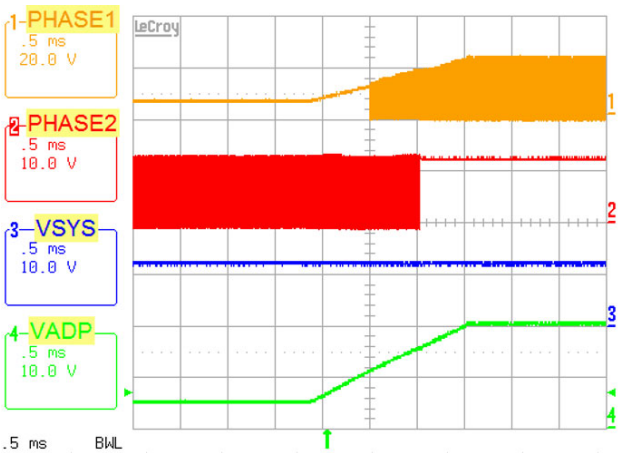


Figure 8. ADP Voltage Ramps Up in Reverse Mode, Buck -> Buck-Boost -> Boost Operation Mode Transition

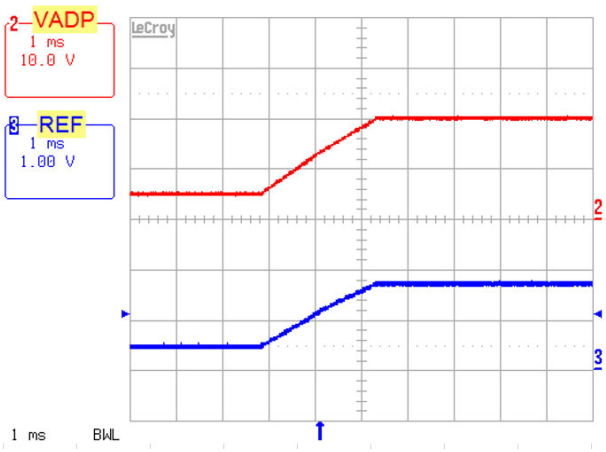


Figure 9. Reverse Mode, $5V_{ADP}$ to $20V_{ADP}$

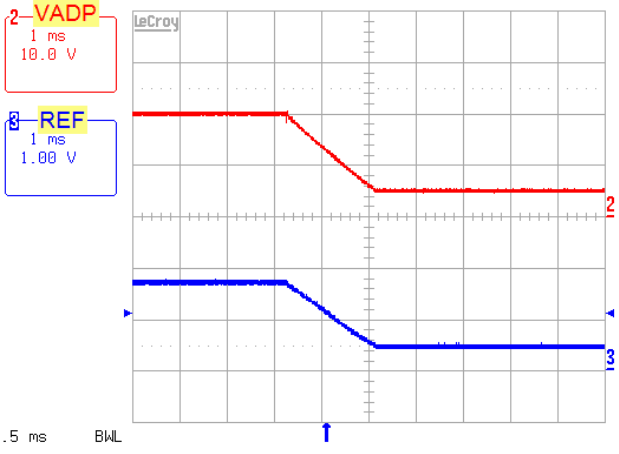


Figure 10. Reverse Mode, $20V_{ADP}$ to $5V_{ADP}$

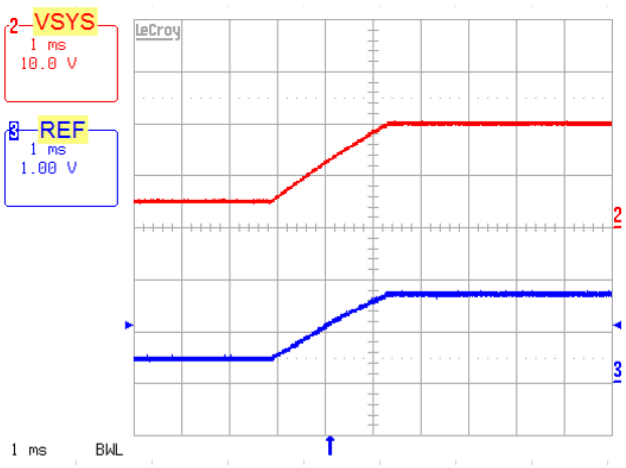


Figure 11. Forward Mode, $5V_{SYS}$ to $20V_{SYS}$

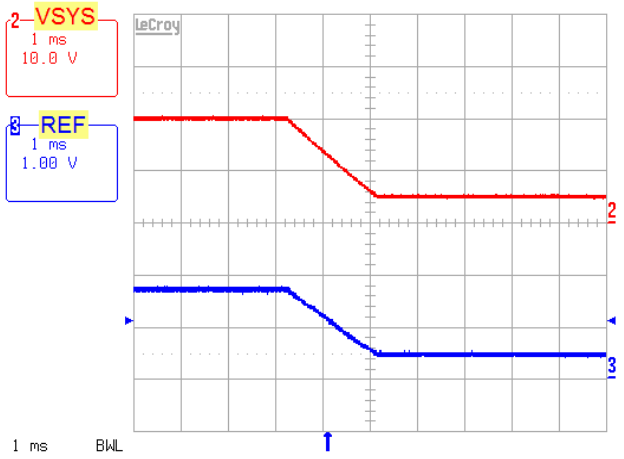


Figure 12. Forward Mode, $20V_{SYS}$ to $5V_{SYS}$

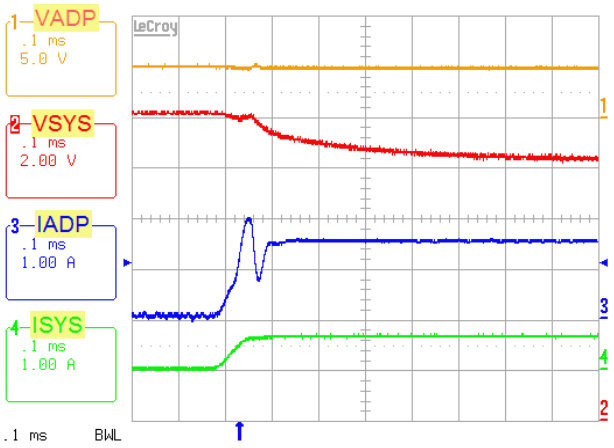


Figure 13. Forward Mode, Output Voltage Loop to ADP Current Loop Transition. $5V_{ADP}$, $12V_{SYS}$, System Load 0A to 0.65A Step, ADP Current Limit = 1.5A

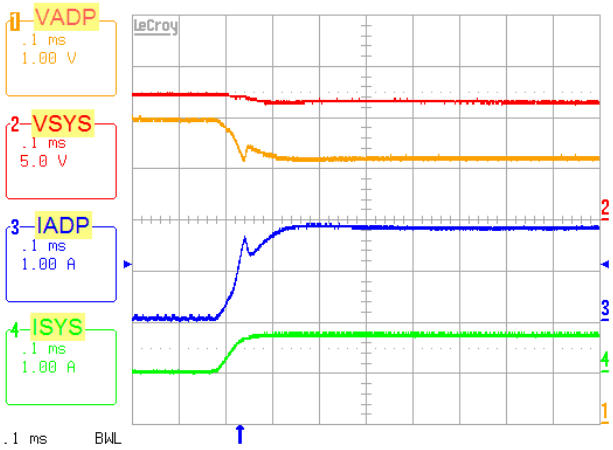


Figure 14. Forward Mode, Output Voltage Loop to Adapter Voltage Loop Transition. $6V_{ADP}$, Input Voltage Limit = 5.12V, $12V_{SYS}$, System Load 0A to 0.78A Step, System Current Limit = 5A, Input Current Limit = 5A

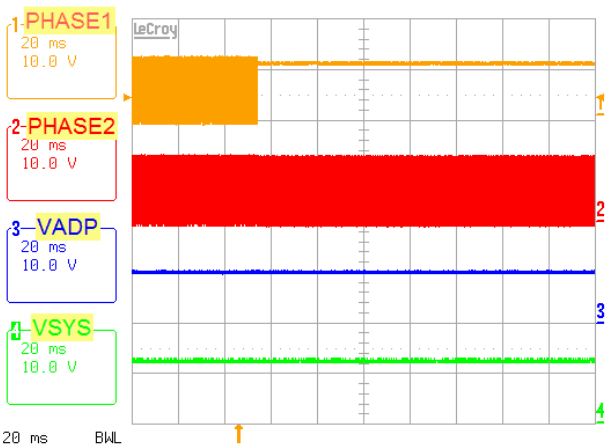


Figure 15. Forward Mode, Force Buck-Boost Mode to Boost Mode. $10V_{ADP}$, $12V_{SYS}$

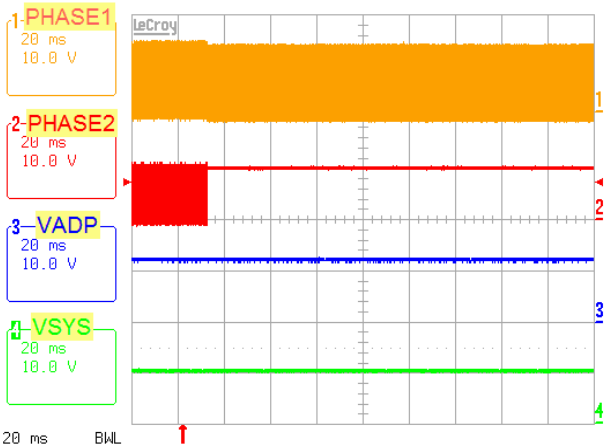


Figure 16. Reverse Mode, Force Buck-Boost Mode to Boost Mode. $12V_{ADP}$, $10V_{SYS}$

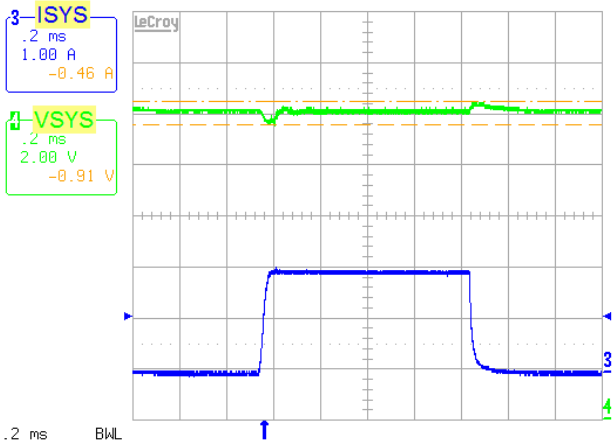


Figure 17. Forward Mode, $5V_{ADP}$, $12V_{SYS}$, 0A-2A Transient Load

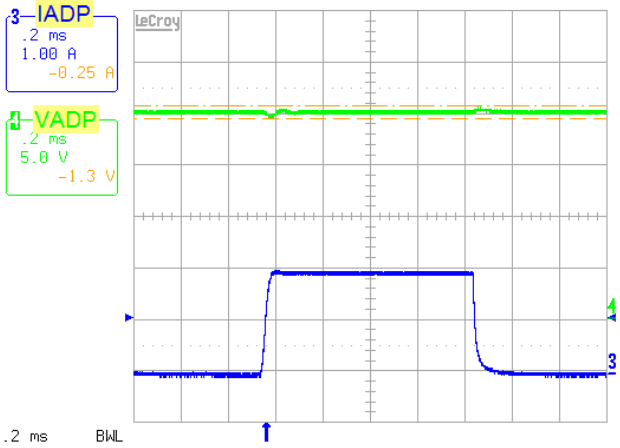


Figure 18. Reverse Mode, $20V_{ADP}$, $12V_{SYS}$, 0A-2A Transient Load

4. General SMBus Architecture

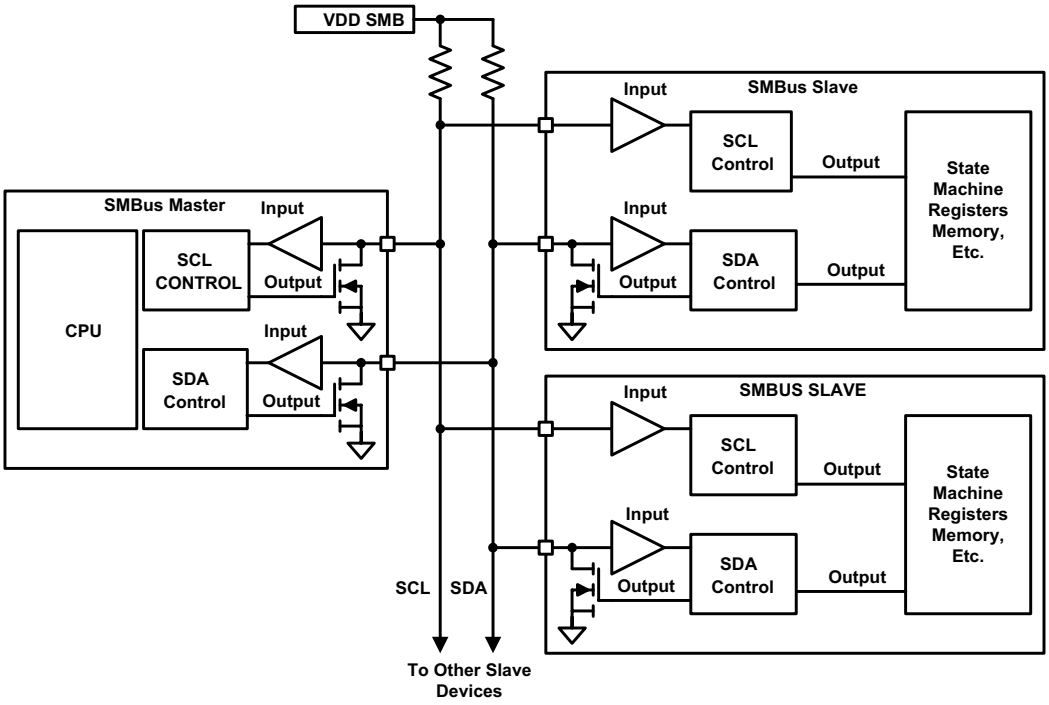


Figure 19. General SMBus Architecture

4.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 20.

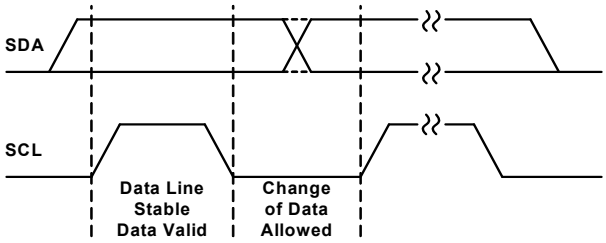


Figure 20. Data Validity

4.2 START and STOP Conditions

As Figure 21 shows, the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

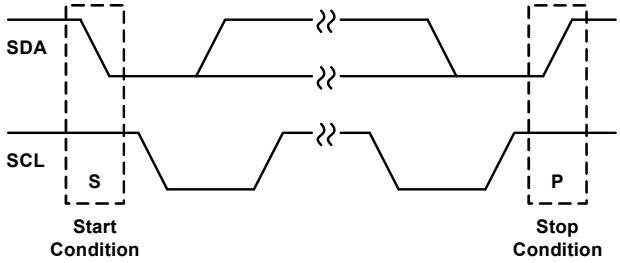


Figure 21. Start and Stop Waveforms

4.3 Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends seven slave address bits and an R/W bit during the next eight clock pulses. During the nine clock pulse, the device that recognizes its own address holds the data line low to acknowledge (see Figure 22). Both the master and slave use the ACK bit to acknowledge receipt of register addresses and data.

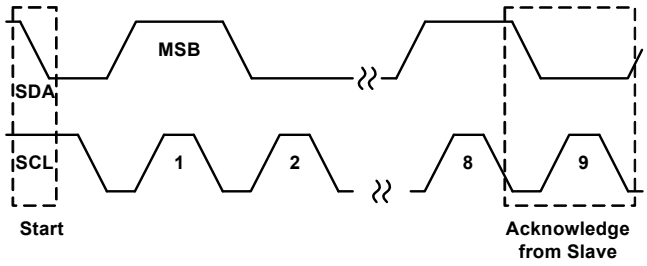


Figure 22. Acknowledge on the SMBus

4.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a START condition, followed by seven bits of slave address (see Table 1 on page 20), and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is “0” for a WRITE or “1” for a READ. If any slave device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is “1”, which indicates a Not Acknowledge condition.

After the control byte is sent and the ISL95338 acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the SystemCurrentLimit register. The register address byte tells the ISL95338 which register the master writes or reads. See Table 2 on page 20 for details of the registers. After the ISL95338 receives a register address byte, it responds with an acknowledge.

4.5 Byte Format

Every byte put on the SDA line must be eight bits long and must be followed by an acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

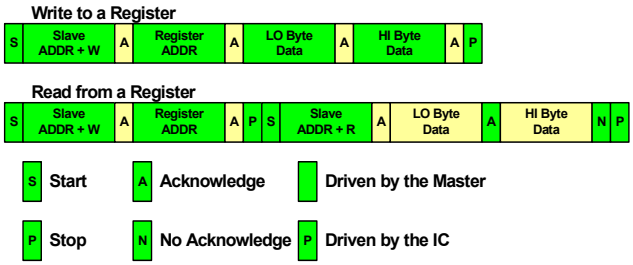


Figure 23. SMBus Read and Write Protocol

4.6 SMBus and I²C Compatibility

The ISL95338 SMBus minimum input logic high voltage is 2V, so it is compatible with I²C with higher than 2V pull-up power supply.

The ISL95338 SMBus registers are 16 bits, so it is compatible with 16 bits I²C or 8 bits I²C with auto-increment capability. The chip does not acknowledge SMBus communication unless either ADP or VOUT is higher than 4.1V.

5. ISL95338 SMBus Commands

The ISL95338 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL95338 uses the SMBus Read-word and Write-word protocols (see Figure 23 on page 19) to communicate with the host system. The ISL95338 is an SMBus slave device and does not initiate communication on the bus. The ISL95338 address is programmable through ADDR0 and ADDR1 voltage levels (see Table 1) to support multiple ISL95338s sharing a common SMBus. Connect the ADDR0 and ADDR1 pins to either ground or VDD.

Bits 1 and 2 are for ADDR0 and ADDR1 pins, respectively. The “1” means the pin voltage is high, while the “0” means the pin voltage is low. From Bits 3 to 7, the value is fixed as 10010. The address is latched at rising VDD 2P7 POR threshold.

Table 1. Address Table

ADDR0	ADDR1	Read/Write	Binary Address	Hex Address
0	0	1	1001,0001	0X91H
0	0	0	1001,0000	0X90H
0	1	1	1001,0101	0X95H
0	1	0	1001,0100	0X94H
1	0	1	1001,0011	0X93H
1	0	0	1001,0010	0X92H
1	1	1	1001,0111	0X97H
1	1	0	1001,0110	0X96H

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The illustration in this datasheet is based on current sensing-resistors R_{s1} = 20mΩ and R_{s2} = 10mΩ, unless otherwise specified.

Table 2. Register Summary

Register Names	Register Address	Read/ Write	Number of Bits	Description	Default
SystemCurrentLimit	0X14	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA, with 10mΩ R_{S1}	1.5A
ForwardRegulatingVoltage	0X15	R/W	12	[14:3]12-bit, LSB size 12mV, see PROG Table 21 on page 37	5.004V
					9.000V
					12.000V
					16.008V
					20.004V
Control0	0X39	R/W	16	Configure various options	0x0000h
Information1	0X3A	R	16	Indicate various status	0x0000h
Control1	0X3C	R/W	16	Configure various options	0x0000h
Control2	0X3D	R/W	16	Configure various options	0x0000h
ForwardInputCurrent	0X3F	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA, with 20mΩ R_{S1}	1.5A
ADPInputCurrentProchot#	0X47	R/W	6	[12:7] ADP input current PROCHOT# threshold. Default 3.072A,128mA resolution for 20mΩ R_{s1}, for Forward mode only.	3.072A
SystemInputCurrentProchot#	0X48	R/W	6	[13:8] System current towards switcher PROCHOT# threshold. Default 4.096A, 256mA resolution for 10mΩ R_{s2}.	4.096A
ReverseRegulatingVoltage	0X49	R/W	12	[14:3] 12-bit, LSB size 12mV Reverse mode regulating voltage reference	5.004V
ReverseOutputCurrent	0X4A	R/W	6	[12:7] 6-bit, LSB size 128mA, total range 4.096A Reverse mode maximum current limit	0.512A

Table 2. Register Summary (Continued)

Register Names	Register Address	Read/ Write	Number of Bits	Description	Default
InputVoltageLimit	0X4B	R/W	6	[13:8] 6-bit, LSB size 512mV Forward low V_{IN} loop voltage reference	4.096V
Control3	0X4C	R/W	16	Configure various options	0x0000h
Information2	0X4D	R	16	Indicate various status	0x0000h
Control4	0X4E	R/W	8	[7:0] 8-bit, configure various options	0x00h
ManufacturerID	0XFE	R	8	Manufacturers ID register	0x49h
DeviceID	0XFF	R	8	Device ID register - 0x0D	0x0Dh

5.1 Setting System Side Current Limit

To set the system side current limit, which is the output current in Forward mode or the input current in Reverse mode, write a 16-bit SystemCurrentLimit command (0X14H or 0b00010100) using the Write-word protocol shown in Figure 23 on page 19 and the data format shown in Table 3 for a 10mΩ R_{s2} or Table 4 for a 5mΩ R_{s2}.

The ISL95338 limits the system current by limiting the CSOP-CSON voltage. By using the recommended current-sense resistor value R_{s2} = 10mΩ, the register's LSB always translates to 4mA of output current. The SystemCurrentLimit register accepts any output current command but only the valid register bits are written to the register and the maximum value is clamped at 6080mA for R_{s2} = 10mΩ.

After POR, the SystemCurrentLimit register is reset to 0x05DCH (1.5A). The SystemCurrentLimit register can be read back to verify its content.

Table 3. SystemCurrentLimit Register 0x14H (11-Bit, 4mA Step, 10mΩ Sense Resistor, x36)

Bit	Description
<1:0>	Not used
<2>	0 = Add 0mA of system current limit. 1 = Add 4mA of system current limit.
<3>	0 = Add 0mA of system current limit. 1 = Add 8mA of system current limit.
<4>	0 = Add 0mA of system current limit. 1 = Add 16mA of system current limit.
<5>	0 = Add 0mA of system current limit. 1 = Add 32mA of system current limit.
<6>	0 = Add 0mA of system current limit. 1 = Add 64mA of system current limit.
<7>	0 = Add 0mA of system current limit. 1 = Add 128mA of system current limit.
<8>	0 = Add 0mA of system current limit. 1 = Add 256mA of system current limit.
<9>	0 = Add 0mA of system current limit. 1 = Add 512mA of system current limit.
<10>	0 = Add 0mA of system current limit. 1 = Add 1024mA of system current limit.
<11>	0 = Add 0mA of system current limit. 1 = Add 2048mA of system current limit.
<12>	0 = Add 0mA of system current limit. 1 = Add 4096mA of system current limit.
<13:15>	Not used
Maximum	<12:2> = 10111110000 6080mA

Note: The gain for the system side current-sensing amplifiers is different for Forward mode and Reverse mode. The gain in Reverse mode is half of that in Forward mode. Therefore, in Reverse mode, the sensing current value needs to be doubled compared to the value set in the SystemCurrentLimit register.

Table 4. ForwardOutputCurrentLimit Register 0x14H (11-Bit, 8mA Step, 5mΩ Sense Resistor, x36)

Bit	Description
<1:0>	Not used
<2>	0 = Add 0mA of system current limit. 1 = Add 8mA of system current limit.
<3>	0 = Add 0mA of system current limit. 1 = Add 16mA of system current limit.
<4>	0 = Add 0mA of system current limit. 1 = Add 32mA of system current limit.
<5>	0 = Add 0mA of system current limit. 1 = Add 64mA of system current limit.
<6>	0 = Add 0mA of system current limit. 1 = Add 128mA of system current limit.
<7>	0 = Add 0mA of system current limit. 1 = Add 256mA of system current limit.
<8>	0 = Add 0mA of system current limit. 1 = Add 512mA of system current limit.
<9>	0 = Add 0mA of system current limit. 1 = Add 1024mA of system current limit.
<10>	0 = Add 0mA of system current limit. 1 = Add 2048mA of system current limit.
<11>	0 = Add 0mA of system current limit. 1 = Add 4096mA of system current limit.
<12>	0 = Add 0mA of system current limit. 1 = Add 8192mA of system current limit.
<13:15>	Not used
Maximum	<12:2> = 10111110000 12160mA

5.2 Setting Input Current Limit in Forward Mode

To set the input current limit in Forward mode, write a 16-bit ForwardInputCurrent command (0x3FH or 0b00111111) using the Write-word protocol shown in Figure 23 on page 19 and the data format shown in Table 5 for a 20mΩ R_{s1} or Table 6 for a 10mΩ R_{s1}.

The ISL95338 limits the input current in Forward mode by limiting the CSIP-CSIN voltage. By using the recommended current-sense resistor values, the register's LSB always translates to 4mA of input current. Any input current limit command is accepted, but only the valid register bits are written to the ForwardInputCurrent register and the maximum values are clamped at 6080mA for R_{s1} = 20mΩ.

Table 5. ForwardInputCurrent Register 0x3FH (11-Bit, 4mA Step, 20mΩ Sense Resistor, x18)

Bit	Description
<1:0>	Not used
<2>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 4mA of input current limit in Forward mode.
<3>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 8mA of input current limit in Forward mode.
<4>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 16mA of input current limit in Forward mode.
<5>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 32mA of input current limit in Forward mode.
<6>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 64mA of input current limit in Forward mode.
<7>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 128mA of input current limit in Forward mode.

Table 5. ForwardInputCurrent Register 0x3FH (11-Bit, 4mA Step, 20mΩ Sense Resistor, x18)

Bit	Description
<8>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 256mA of input current limit in Forward mode.
<9>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 512mA of input current limit in Forward mode.
<10>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 1024mA of input current limit in Forward mode.
<11>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 2048mA of input current limit in Forward mode.
<12>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 4096mA of input current limit in Forward mode.
<13:15>	Not used
Maximum	<12:2> = 10111110000 6080mA.

Table 6. ForwardInputCurrent Register 0x3FH (11-Bit, 8mA Step, 10mΩ Sense Resistor, x18)

Bit	Description
<1:0>	Not used
<2>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 8mA of input current limit in Forward mode.
<3>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 16mA of input current limit in Forward mode.
<4>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 32mA of input current limit in Forward mode.
<5>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 64mA of input current limit in Forward mode.
<6>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 128mA of input current limit in Forward mode.
<7>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 256mA of input current limit in Forward mode.
<8>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 512mA of input current limit in Forward mode.
<9>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 1024mA of input current limit in Forward mode.
<10>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 2048mA of input current limit in Forward mode.
<11>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 4096mA of input current limit in Forward mode.
<12>	0 = Add 0mA of input current limit in Forward mode. 1 = Add 8192mA of input current limit in Forward mode.
<13:15>	Not used
Maximum	<12:2> = 10111110000 12160mA

5.3 Setting System Regulating Voltage in Forward Mode

To set the regulating voltage in Forward mode, write a 16-bit ForwardRegulatingVoltage command (0x15H or 0b00010101) using the Write-word protocol shown in Figure 23 on page 19 and the data format as shown in Table 7.

The output regulating voltage range in Forward mode is 2V to 24V. The ForwardRegulatingVoltage register accepts any voltage command, but only the valid register bits are written to the register. The maximum value is clamped at 24.576V. The ISL95338 accepts a 0V command, but the register value does not change. The VOUTS pin is the output voltage regulation sense point in Forward mode.

In Forward mode, you can also configure the regulating output voltage by setting the external voltage divider on the VOUTS pin without changing the ForwardRegulatingVoltage register value.

Table 7. ForwardRegulatingVoltage Register 0x15H (12mV Step)

Bit	Description
<2:0>	Not used
<3>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 12mV of regulating voltage in Forward mode.
<4>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 24mV of regulating voltage in Forward mode.
<5>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 48mV of regulating voltage in Forward mode.
<6>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 96mV of regulating voltage in Forward mode.
<7>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 192mV of regulating voltage in Forward mode.
<8>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 384mV of regulating voltage in Forward mode.
<9>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 768mV of regulating voltage in Forward mode.
<10>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 1536mV of regulating voltage in Forward mode.
<11>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 3072mV of regulating voltage in Forward mode.
<12>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 6144mV of regulating voltage in Forward mode.
<13>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 12288mV of regulating voltage in Forward mode.
<14>	0 = Add 0mV of regulating voltage in Forward mode. 1 = Add 24576mV of regulating voltage in Forward mode.
<15>	Not used
Maximum	24576mV

Note: The default reading value of this register is 6.288V when the chip is powering up without writing any values because of the DAC initial value. Thus, write the needed value in this register before enabling forward output voltage.

5.4 Setting PROCHOT# Threshold for ADP Side Overcurrent Condition

To set the PROCHOT# assertion threshold for the ADP side input overcurrent condition in Forward mode, write a 16-bit ADPsideProchot# command (0x47H or 0b01000111) using the Write-word protocol shown in Figure 23 on page 19 and the data format shown in Table 8. By using the recommended current-sense resistor values, the register's LSB always translates to 128mA of input current. The ADPsideProchot# register accepts any current command, but only the valid register bits are written to the register. The maximum values are clamped at 6400mA for R_{s1} = 20mΩ.

After POR, the ADPsideProchot# register is reset to 0x0C00H. The ADPsideProchot# register can be read back to verify its content.

If the input current exceeds the ADPsideProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit<10:9> and latches on for a minimum time programmed by Control2 register Bit<8:6>.

Table 8. ADPsideProchot# Register 0x47H (20mΩ Sensing Resistor, 128mA Step, x18 Gain)

Bit	Description
<6:0>	Not used
<7>	0 = Add 0mA of ADPsideProchot# threshold. 1 = Add 128mA of ADPsideProchot# threshold.
<8>	0 = Add 0mA of ADPsideProchot# threshold. 1 = Add 256mA of ADPsideProchot# threshold.
<9>	0 = Add 0mA of ADPsideProchot# threshold. 1 = Add 512mA of ADPsideProchot# threshold.
<10>	0 = Add 0mA of ADPsideProchot# threshold. 1 = Add 1024mA of ADPsideProchot# threshold.
<11>	0 = Add 0mA of ADPsideProchot# threshold. 1 = Add 2048mA of ADPsideProchot# threshold.
<12>	0 = Add 0mA of ADPsideProchot# threshold. 1 = Add 4096mA of ADPsideProchot# threshold.
<15:13>	Not used
Maximum	<12:7> = 110010, 6400mA

5.5 Setting PROCHOT# Threshold for System Side Overcurrent Condition

To set the PROCHOT# signal assertion threshold for system side input overcurrent condition in Reverse mode, write a 16-bit SystemsideProchot# command (0x48H or 0b01001000) using the Write-word protocol shown in Figure 23 on page 19 and the data format shown in Table 9. By using the recommended current-sense resistor values, the register's LSB always translates to 256mA of system side current. The SystemsideProchot# register accepts any current command, but only the valid register bits are written to the register. The maximum values are clamped at 12.8A for R_{s2} = 10mΩ.

After POR, the SystemsideProchot# register is reset to 0x1000H. The SystemsideProchot# register can be read back to verify its content.

If the system side current exceeds the SystemsideProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit<10:9> and latches on for a minimum time programmed by Control2 register Bit<8:6>.

Table 9. SystemsideProchot# Register 0x48H (10mΩ Sensing Resistor, 256mA Step, x18 Gain)

Bit	Description
<7:0>	Not used
<8>	0 = Add 0mA of SystemsideProchot# threshold. 1 = Add 256mA of SystemsideProchot# threshold.
<9>	0 = Add 0mA of SystemsideProchot# threshold. 1 = Add 512mA of SystemsideProchot# threshold.
<10>	0 = Add 0mA of SystemsideProchot# threshold. 1 = Add 1024mA of SystemsideProchot# threshold.
<11>	0 = Add 0mA of SystemsideProchot# threshold. 1 = Add 2048mA of SystemsideProchot# threshold.
<12>	0 = Add 0mA of SystemsideProchot# threshold. 1 = Add 4096mA of SystemsideProchot# threshold.
<13>	0 = Add 0mA of SystemsideProchot# threshold. 1 = Add 8192mA of SystemsideProchot# threshold.
<15:14>	Not used
Maximum	<13:8> = 110010, 12800mA

5.6 Setting PROCHOT# Debounce Time and Duration Time

Control2 register Bit<10:9> configures the PROCHOT# signal debounce time before its assertion for ADPsideProchot# and SystemsideProchot#.

Control2 register Bit<8:6> configures the minimum duration of the PROCHOT# signal when asserted.

5.7 Control Registers

The Control0, Control1, Control2, Control3, and Control4 registers configure the operation of the ISL95338. To change certain functions or options after POR, write a 16-bit control command to Control0 register (0x39H or 0b00111001), and a 16-bit control command to Control1 register (0x3CH or 0b00111100), Control2 register (0x3DH or 0b00111101), Control3 register (0x4CH or 0b00111100), or Control4 register (0x4EH or 0b00111101) using the Write-word protocol shown in Figure 23 on page 19 and the data format shown in Tables 10, 11, 12, 13, and 14, respectively.

Table 10. Control0 Register 0x39H

Bit	Bit Name	Description
<15:13>	Forward Buck and Buck-Boost Phase Comparator Threshold Offset	Adjusts the phase comparator threshold offset for forward buck and buck-boost. 000 = 0mV 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
<12:10>	Forward and Reverse Boost Phase Comparator Threshold Offset	Adjusts the phase comparator threshold offset for forward and reverse boost. 000 = 0mV 001 = 0.5mV 010 = 1mV 011 = 1.5mV 100 = -2mV 101 = -1.5mV 110 = -1mV 111 = -0.5mV
<9:7>	Reverse Buck and Buck-Boost Phase Comparator Threshold Offset	Adjusts the phase comparator threshold offset for reverse buck and buck-boost. 000 = 0mV 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
<6:5>	High-Side FET Short Detection Threshold	Configures the high-side FET short detection PHASE node voltage threshold during low-side FET turn-on. 00 = 400mV (default) 01 = 500mV 10 = 600mV 11 = 800mV
<4:3>		Not used
<2>	Disable Input Voltage Regulation Loop	Disables or enables the input voltage regulation loop. 0 = Enable input voltage regulation loop (default) 1 = Disable input voltage regulation loop
<1>	ADP Side Discharge	Enables or disables the ADP side charger function. 0 = Disable (default) 1 = Enable
<0>	System Side Discharge	Enables or disables the system side charger function. 0 = Disable (default) 1 = Enable

Table 11. Control1 Register 0x3CH

Bit	Bit Name	Description
<15>	Disable Diode-Emulation Comparator	Enables or disables diode-emulation comparator. 0 = Diode-emulation comparator enabled (default) 1 = Diode-emulation comparator disabled
<14>	Allow Sinking Current During Negative DAC Transition	Enables or disables sinking current during negative DAC transition. 0 = Sinking current during negative DAC transition enabled (default) 1 = Sinking current during negative DAC transition disabled
<13>	Skip Trim During Restart	Enables or disables trim read during restart. Program this bit when PGOOD is high. 0 = Read trim during restart 1 = Skip trim during restart
<12>	Skip Autozero During Restart	Enables or disables autozero during restart. Program this bit when PGOOD is high. 0 = Autozero during restart 1 = Skip autozero during restart

Table 11. Control1 Register 0x3CH (Continued)

Bit	Bit Name	Description
<11>	Reverse Mode Function	Enables or disables Force Reverse mode function. 0 = Disable Force Reverse mode function (default) 1 = Enable Force Reverse mode function
<10>	Audio Filter	Enables or disables the audio filter function. No audio filter function in Buck-Boost mode. 0 = Disable (default) 1 = Enable
<9:7>	Switching Frequency	Configures the switching frequency. 000 = 1000kHz 001 = 910kHz 010 = 850kHz 011 = 787kHz 100 = 744kHz 101 = 695kHz 110 = 660kHz 111 = 620kHz
<6>		Not used
<5>	Disable System Side Current-Amp When in FWD Mode without ADP	Enables or disables the system side current amplifier when in FWD mode without ADP. 0 = Enable system side current amplifier (default) 1 = Disable system side current amplifier
<4>	Bypass Mode	Enables or disables the Bypass mode. 0 = Disable (default) 1 = Enable
<3>	Fast REF mode	Enables or disables the fast REF mode. 0 = Disable (default) 1 = Enable
<2>	Stop Switching in FWD Mode	Enables or disables the buck-boost switching V_{OUT} output. When disabled, the ISL95338 stops switching and REF drops to OV. Valid in Forward mode only. 0 = Enable switching (default) 1 = Disable switching
<1>	OV Enable or Disable During Slew-Down	Enables or disables OV fault when the VDAC slew rate is down in Forward and Reverse mode. 0 = Enable OV (default) 1 = Disable OV
<0>	Force 5.04V VDAC	Enables or disables force 5.04V VDAC in Forward and Reverse mode. 0 = Disable force 5.04V VDAC (default) 1 = Enable force 5.04V VDAC

Table 12. Control2 Register 0x3DH

Bit	Bit Name	Description
<15>	OV Control	Enables or disables OV. 0 = Enable OV (default) 1 = Disable OV
<14>	UV Control	Enables or disables UV. 0 = Enable UV (default) 1 = Disable UV
<13>	Fault Restart Debounce for Reverse Enable	Configures fault restart debounce for reverse enable. 0 = Debounce time is 1.3s (default) 1 = Debounce time is 150ms
<12>	Fault Restart Debounce	Configures fast fault restart debounce. 0 = Debounce time is 1.3s or 150ms, depends on Bit<13> setting (default) 1 = Debounce time is 200µs or 10µs, depends on Bit<13> setting
<11>	Forward Restart Debounce for Forward Enable	Configures fault restart debounce for forward enable. 0 = Debounce time is 1.3s (default) 1 = Debounce time is 150ms

Table 12. Control2 Register 0x3DH (Continued)

Bit	Bit Name	Description
<10:9>	PROCHOT# Debounce	Configures the PROCHOT# debounce time before its assertion for ADPsideProchot# and SystemsideProchot#. 00: 7µs (default) 01: 100µs 10: 500µs 11: 1ms
<8:6>	PROCHOT# Duration	Configures the minimum duration of the PROCHOT# signal when asserted. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 500µs 110 = 100µs 111 = 0s
<5>		Not used
<4>	Reverse Fast Swap	Configures reverse fast swap. 0 = Disable reverse fast swap (default) 1 = Enable reverse fast swap
<3>	Forward Fast Swap	Configures forward fast swap. 0 = Disable forward fast swap (default) 1 = Enable forward fast swap
<2>	Not Used	Not used
<1>	Disable WOC Fault	Enables or disables WOC fault. 0 = Enable WOC (default) 1 = Disable WOC
<0>	System Side WOC Threshold	Configures the System Side WOC fault comparator value. 0 = 20mV (default) 1 = 30mV

Table 13. Control3 Register 0x4CH

Bit	Bit Name	Description
<15>	Re-Read PROG Pin Resistor	Specifies whether to re-read the PROG pin resistor before switching. 0 = Re-read PROG pin resistor (default) 1 = Do not re-read PROG pin resistor
<14>		Not used
<13>		Not used
<12>	Reverse Startup Debounce Time	Configures the startup debounce time for reverse mode. 0 = Debounce time is 200µs (default) 1 = Debounce time is 10µs
<11>	Forward Startup Debounce Time	Configures the startup debounce time for forward mode. 0 = Debounce time is 200µs (default) 1 = Debounce time is 10µs
<10:8>	Force Operating Mode	Enables or disables Force Operating mode. 0XX: No effect 100: No switching, do not use 101: Buck mode 110: Boost mode 111: Buck-Boost mode
<7>		Not used
<6>	Current Loop Feedback Gain	Configures the current loop feedback gain for high current. 0 = Gain x 1 (default) 1 = Gain x 0.5
<5>	Input Current Limit Loop	Disables the input current limit loop. 0 = Enable input current limit loop (default) 1 = Disable input current limit loop

Table 13. Control3 Register 0x4CH (Continued)

Bit	Bit Name	Description
<4>	Not Used	Not used
<3>	Disabled REF Amplifier for Use with External Reference	Disables the REF amplifier. 0 = Enable REF amplifier (default) 1 = Disable REF amplifier
<2>	Digital Reset	Resets all SMBus register values to POR default value and restarts switching. 0 = Idle (default) 1 = Reset
<1>	Buck-Boost Switching Period	Configures the switching period in Buck-Boost mode. 0 = Period x 1 (default) 1 = Period x 2 (half switching frequency)
<0>	PGOOD Setting	Configures the PGGOD assert condition. 0 = PGOOD suppressed until VREF equals to VDAC (default) 1 = PGOOD assert when switching starts

Table 14. Control4 Register 0x4EH

Bit	Bit Name	Description
<15:8>		Not used
<7>	Reverse Mode Current PROCHOT#	Enables or disables trigger PROCHOT# with current in Reverse mode. 0 = Enable (default) 1 = Disable
<6>	Forward Sleep Mode	Enables or disables Chip Sleep mode in Forward mode regardless of ADP voltage. RVSEN pin or Control1 bit <11> can override this function. 0 = Disable (default) 1 = Enable
<5:2>		Not used
<1>	PROCHOT# Clear	Clears PROCHOT#. 0 = Idle (default) 1 = Clear PROCHOT#
<0>	PROCHOT# Latch	Manually resets PROCHOT#. 0 = PROCHOT# signal auto-clear 1 = hold PROCHOT# low when tripped

5.8 Regulating Voltage Register in Reverse Mode

The ReverseRegulatingVoltage register contains the SMBus readable and writable Reverse mode output regulation voltage reference. The default value is 5.004V. This register accepts any voltage command but only the valid register bits are written to the register. However, the register should not be programmed higher than the recommended operating voltage.

In Reverse mode, you can also configure the regulating output voltage on the ADP side by setting the external voltage divider on the ADP pin, without changing the ReverseRegulatingVoltage register value.

Table 15. ReverseRegulatingVoltage Register 0x49H

Bit	Description
<2:0>	Not used
<3>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 12mV of regulating voltage in Reverse mode.
<4>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 24mV of regulating voltage in Reverse mode.
<5>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 48mV of regulating voltage in Reverse mode.
<6>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 96mV of regulating voltage in Reverse mode.

Table 15. ReverseRegulatingVoltage Register 0x49H (Continued)

Bit	Description
<7>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 192mV of regulating voltage in Reverse mode.
<8>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 384mV of regulating voltage in Reverse mode.
<9>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 768mV of regulating voltage in Reverse mode.
<10>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 1536mV of regulating voltage in Reverse mode.
<11>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 3072mV of regulating voltage in Reverse mode.
<12>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 6144mV of regulating voltage in Reverse mode.
<13>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 12288mV of regulating voltage in Reverse mode.
<14>	0 = Add 0mV of regulating voltage in Reverse mode. 1 = Add 24576mV of regulating voltage in Reverse mode.
<15>	Not used
Maximum	27456mV

5.9 Output Current Limit Register in Reverse Mode

The ReverseCurrentLimit register contains the SMBus readable and writable reverse current limit. The default is 512mA. This register accepts any current command, but only the valid register bits are written to the register. The maximum values are clamped at 4096mA for R_{s1} = 20mΩ.

Table 16. ReverseCurrentLimit Register 0x4AH

Bit	Description
<6:0>	Not used
<7>	0 = Add 0mA of output current limit in Reverse mode. 1 = Add 128mA of output current limit in Reverse mode.
<8>	0 = Add 0mA of output current limit in Reverse mode. 1 = Add 256mA of output current limit in Reverse mode.
<9>	0 = Add 0mV of output current limit in Reverse mode. 1 = Add 512mA of output current limit in Reverse mode.
<10>	0 = Add 0mV of output current limit in Reverse mode. 1 = Add 1024mA of output current limit in Reverse mode.
<11>	0 = Add 0mV of output current limit in Reverse mode. 1 = Add 2048mA of output current limit in Reverse mode.
<12>	0 = Add 0mV of output current limit in Reverse mode. 1 = Add 4096mA of output current limit in Reverse mode.
<15:13>	Not used
Maximum	4096mA

5.10 Input Voltage Limit Register

The InputVoltageLimit register contains the SMBus readable and writable input voltage limits. The default is 4.096V. This register accepts any command, but only the valid register bits are written to the register. The maximum values are clamped at 18V.

Table 17. InputVoltageLimit Register 0x4BH

Bit	Description
<7:0>	Not used
<8>	0 = Add 0mV of input voltage limit. 1 = Add 512mV of input voltage limit.
<9>	0 = Add 0mA of input voltage limit. 1 = Add 1024mV of input voltage limit.
<10>	0 = Add 0mV of input voltage limit. 1 = Add 2048mV of input voltage limit.
<11>	0 = Add 0mV of input voltage limit. 1 = Add 4096mV of input voltage limit.
<12>	0 = Add 0mV of input voltage limit. 1 = Add 8192mV of input voltage limit.
<13>	0 = Add 0mV of input voltage limit. 1 = Add 16384mV of input voltage limit.
<15:14>	Not used
Maximum	18000mV

5.11 Information Register

The Information Register contains SMBus readable information about manufacture and operating modes. Tables 18 and 19 identify the bit locations of the information available.

Table 18. Information1 Register 0x3AH

Bit	Description
<10:0>	Not used
<11>	Indicates whether SystemSideProchot# is tripped. 0 = SystemSideProchot# is not tripped 1 = SystemSideProchot# is tripped
<12>	Indicates whether ADPsideProchot# is tripped. 0 = ADPSideProchot# is not tripped 1 = ADPSideProchot# is tripped
<14:13>	Indicates the active control loop. 00 = Voltage control loop is active 01 = System current loop is active 10 = ADP current limit loop is active 11 = Input voltage loop is active
<15>	Indicates whether the internal reference circuit is active. Bit<15> = 0 indicates that the ISL95338 is in low power mode. 0 = Reference is not active 1 = Reference is active

Table 19. Information2 Register 0x4DH

Bit	Description
<4:0>	Program resister read out
<7:5>	Indicates the ISL95338 operation mode. 001: Forward Boost 010: Forward Buck 011: Forward Buck-Boost 101: Reverse Boost 110: Reverse Buck 111: Reverse Buck-Boost
<11:8>	Indicates the ISL95338 state machine status. 0000 = OFF 0010 = ADP 0100 = VSYS 0110 = Enable Reverse mode 1000 = Enable LDO5 1110 = WAIT
<12>	Not used
<13>	Not used
<14>	Indicates forward switching enable. 0 = Not enabled 1 = Enabled
<15>	Not used

6. Application Information

6.1 R3 Modulator

The ISL95338 uses the Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM, while eliminating many of their shortcomings. Figure 24 conceptually shows the R3 modulator circuit and Figure 25 shows the operation principles in steady state.

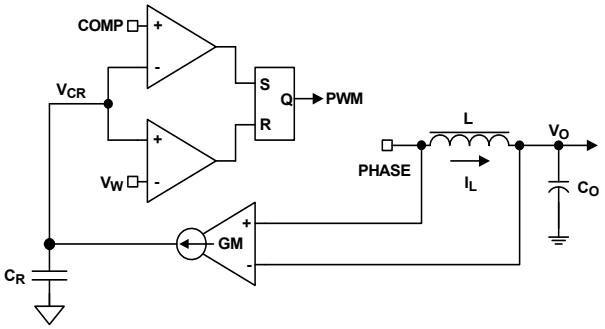


Figure 24. R3 Modulator

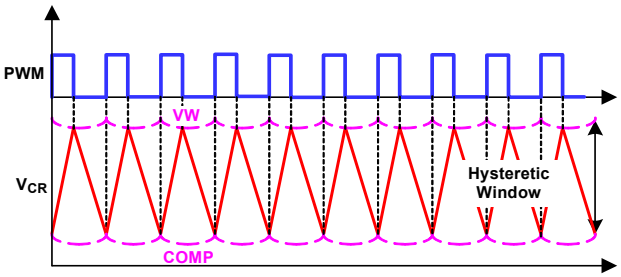


Figure 25. R3 Modulator Operation Principles in Steady State

The fixed voltage window between VW and COMP is called the VW window in the following discussion. The modulator charges the ripple capacitor C_R with a current source equal to $g_m (V_{IN} - V_O)$ during PWM on-time and discharges the ripple capacitor C_R with a current source equal to $g_m V_O$ during PWM off-time, where g_m is a gain factor. The C_r voltage V_{CR}, therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{CR} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{cr}, which is a large amplitude and noise-free synthesized signal, it achieves lower phase jitter than a conventional hysteretic mode modulator.

Figure 26 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response and turns on PWM pulses earlier and more frequently temporarily. This behavior allows for higher control loop bandwidth than a conventional fixed frequency PWM modulator at the same steady-state switching frequency.

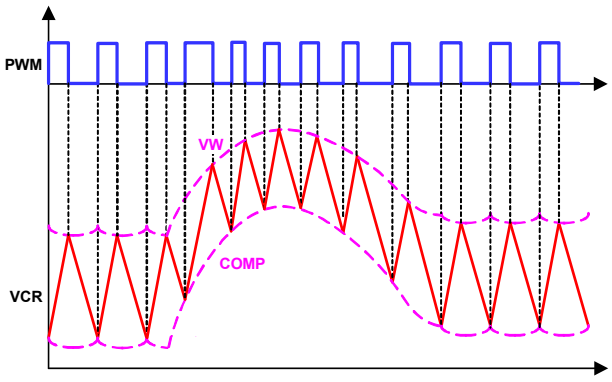


Figure 26. R3 Modulator Operation Principles in Dynamic Response

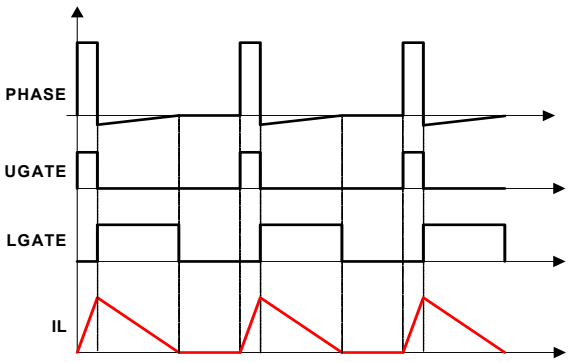


Figure 27. Diode Emulation

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. For example, in Buck DE mode the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, emulating a diode. As shown in Figure 27, when LGATE is on, the low-side MOSFET carries current, which creates negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the

phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss. Similar operations apply for other modes, such as Boost and Buck-boost mode.

If the load current is light enough, as Figure 27 shows, the inductor current reaches and stays at zero before the next phase node pulse. At this stage, the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and the regulator is in CCM, although the controller is in DE mode.

Figure 28 shows the operation principle in Diode Emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, therefore, it is the same, making the inductor current triangle the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{CR} in DE mode to make it mimic the inductor current. The COMP voltage takes longer to reach V_{CR}, which naturally stretches the switching period. The inductor current triangles move farther apart from each other, so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

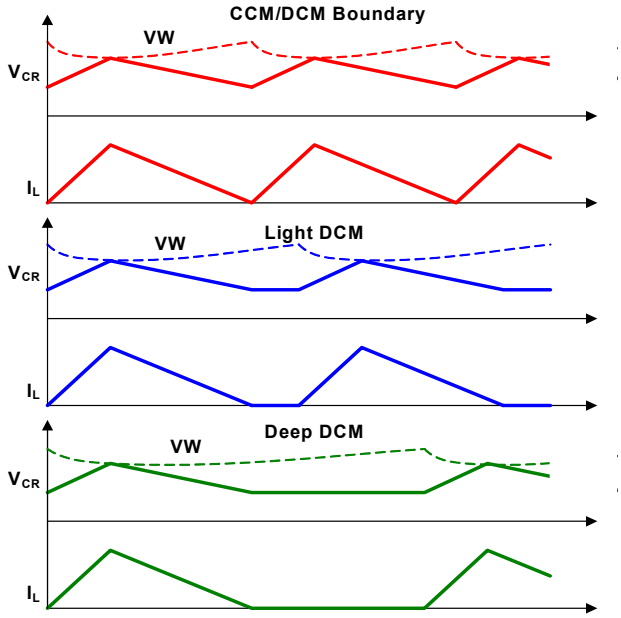


Figure 28. Period Stretching

6.2 ISL95338 Bidirectional Buck-Boost Voltage Regulator

The ISL95338 bidirectional buck-boost voltage regulator drives an external N-channel MOSFET bridge comprised of two transistor pairs as shown in Figure 2 on page 5. The first pair, Q_1 and Q_2, is a buck arrangement with the transistor center tap connected to an inductor “input”, as is the case with a buck converter in Forward mode. The second transistor pair, Q_3 and Q_4, is a boost arrangement with the transistor center tap connected to the same inductor’s “output”, as is the case with a boost converter in Forward mode. This arrangement supports the same operation mode in reverse direction.

- In Forward Buck mode, Q_1 and Q_2 turn on and off alternatively, while Q_3 remains off and Q_4 remains on.
- In Forward Boost mode, Q3 and Q4 turn on and off alternatively, while Q1 remains on and Q2 remains off.
- In Forward Buck-Boost mode, Q_1 and Q_3 turn on at the same time, Q_3 turns off and Q_4 turns on, Q_1 turns off and Q_2 turns on, and after Q_2 and Q_4 turn off at the same time, and Q_1 and Q_3 turn on again.
- In Forward Bypass mode, Q_1 and Q_4 are always on, while Q_2 and Q_3 are always off.
- In Reverse Buck mode, Q_3 and Q_4 turn on and off alternatively, while Q_2 remains off and Q_1 remains on.
- In Reverse Boost mode, Q_1 and Q_2 turn on and off alternatively, while Q_4 remains on and Q_3 remains off.

- In Reverse Buck-Boost mode, Q_4 and Q_2 turn on at the same time, Q_2 turns off and Q_1 turns on, Q_4 turns off and Q_3 turns on, and after Q_3 and Q_1 turn off at the same time and Q_4 and Q_2 turn on again.
- In Reverse Bypass mode, Q_1 and Q_4 are always on, except during the needed refresh time, while Q_2 and Q_3 are always off.
- In Reverse mode, the output sensing point is CSIP pin.

Table 20. Operation Mode

Mode	Q_1	Q_2	Q_3	Q_4
Forward Buck	Control FET	Sync. FET	OFF	ON
Forward Boost	ON	OFF	Control FET	Sync. FET
Forward Buck-Boost	Control FET	Sync. FET	Control FET	Sync. FET
Forward Bypass	ON	OFF	OFF	ON
Reverse Buck	ON	OFF	Sync. FET	Control FET
Reverse Boost	Sync. FET	Control FET	OFF	ON
Reverse Buck-Boost	Sync. FET	Control FET	Sync. FET	Control FET
Reverse Bypass	ON	OFF	OFF	ON

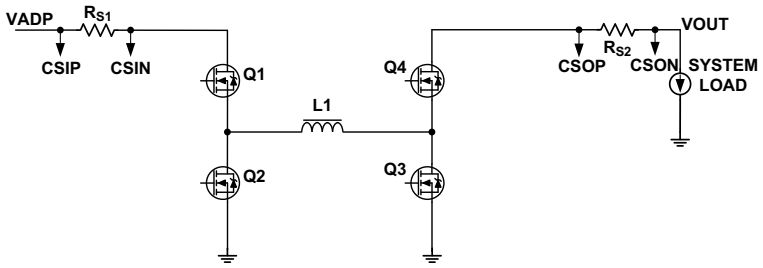


Figure 29. Buck-Boost Regulator Topology

The ISL95338 optimizes the operation mode transition algorithm by considering the input and output voltage ratio and the load condition. The ISL95338 transitions from Boost mode to Buck-Boost mode when ADP voltage V_{ADP} is rising and is higher than 94% of the system bus voltage VSYS, If V_{ADP} is higher than 120% of VSYS, the ISL95338 transitions from Buck-Boost mode to Buck mode under any circumstance. At a heavier load, the mode transition point changes accordingly to accommodate the duty cycle change due to the power loss on the voltage regulator circuit.

When the ADP voltage V_{ADP} is falling and is lower than 106% of the system bus voltage VSYS, the ISL95338 transitions from Buck mode to Buck-Boost mode. If V_{ADP} is lower than 80% of VSYS, the ISL95338 transitions from Buck-Boost mode to Boost mode.

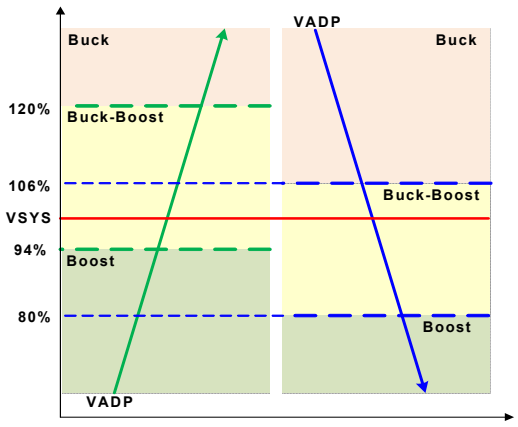


Figure 30. Operation Mode

When the reverse function is enabled with the SMBus command or RVSEN pin, and if reverse voltage VSYS is higher than 4.1V, the ISL95338 operates in Reverse mode.

You can enable Bypass mode with Control1 register Bit 4. When the Bypass mode control bit is enabled, the REF ramps to the input voltage, and the switcher continues switching until the output voltage is in the 300mV window to the input. When the regulating voltage is within the 300mV window to the input voltage, the latch is set to stop the switching, Q_1 and Q_4 are always on while Q_2 and Q_3 are always off, and UV and OV are disabled. To exit Bypass mode, unprogram Control1 register Bit 4; the REF then ramps to DAC and switching resumes.

6.3 Soft-Start

The ISL95338 includes a low power LDO with nominal 5V output with an input that is OR-ed from the VOUT pin and ADP pin. The ISL95338 also includes a high power LDO with nominal 5V output with an input that is from the DCIN pin connected to the ADP and the system bus, through an external OR-ing diode circuit. Both LDO outputs are tied to the VDD pin to provide the bias power and gate drive power for ISL95338. The VDDP pin is the ISL95338 gate drive power supply input. Use an R-C filter to generate the VDDP pin voltage from the VDD pin voltage.

When V_{DD} > 2.7V, the ISL95338 digital block is activated. The soft-start time can be set by the external capacitor on the REF pin. The ISL95338 sources 1µA current out of the REF pin to charge this external capacitor. Its voltage is used as the output voltage reference in the soft-start procedure.

6.4 Programming Options

The resistor from the PROG pin to GND programs the ISL95338's forward output voltage configuration. Table 21 shows the programing options.

Table 21. PROG Pin Programming Options

Prog-GND Resistance (kΩ)		Default Forward Regulating Voltage
Min	Max	
0	28	5.004
35.7	71.5	9.000
82.5	133	12.000
147	215	16.008
237	open	20.004

The switching frequency can be changed through SMBus Control1 register Bit<9:7> after POR. See the SMBus Control1 register programming table (Table 11) for a detailed description.

After POR, the ISL95338 sources 10µA current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. If the ISL95338 is powered up from reverse side, it does not read PROG resistor. When FRWEN is enabled, the ISL95338 resets the forward regulating voltage register to its default values according to the PROG pin setting.

By default, the ADP current-sensing resistor R_{s1} is 20mΩ and VSYS current-sensing resistor R_{s2} is 10mΩ. Using these R_{s1} = 20mΩ and R_{s2} = 10mΩ options results in a 4mA/LSB correlation in the SMBus current commands.

If the R_{s1} and R_{s2} values are different from these R_{s1} = 20mΩ and R_{s2} = 10mΩ options, the SMBus command needs to be scaled accordingly to obtain the correct current. Smaller current-sense resistor values reduce the power loss whereas larger current-sense resistor values give better accuracy.

The illustration in this datasheet is based on current-sensing resistors R_{s1} = 20mΩ and R_{s2} = 10mΩ unless specified otherwise.

6.5 DE Operation

In DE mode, the ISL95338 uses a phase comparator to monitor the PHASE node voltage to the ground or VOUT or ADP voltage during the low-side switching FET on-time to detect the inductor current zero crossing, depending on the operation mode (Buck, Buck-Boost, or Boost) and power delivery direction (Forward or reverse direction). See Table 22. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize the inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the ISL95338 may lose diode emulation ability. To prevent this scenario, the ISL95338 uses a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the ISL95338 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point.

Table 22. Voltage Comparator for DE Operation

Mode	Direction	Voltage Comparator
Buck	Forward	PHASE 1 to GND
Boost	Forward	PHASE 1 to VOUT
Buck-Boost	Forward	PHASE 1 to VOUT
Buck	Reverse	PHASE 2 to GND
Boost	Reverse	PHASE 1 to ADP
Buck-Boost	Reverse	PHASE 1 to ADP

6.6 Forward Mode

When the forward function is enabled with the SMBus command or FRWEN pin (voltage is higher than 0.8V) and DCIN is powered by ADP, and if the ADP is plugged in and its value is higher than 4.1V, the ISL95338 can operate in Forward Buck mode, Forward Boost mode, Forward Buck-Boost mode, or Forward Bypass mode. After the forward output voltage reaches the regulating output voltage range set by register 0X15H Bit<14:3>, forward power-good FWGPG asserts to High.

6.7 Reverse Mode for USB OTG (On-the-Go)

When the reverse function is enabled with the SMBus command (Control1 Bit 11) or RVSEN pin, and if an external voltage is on system side and its value is higher than 4.1V, the ISL95338 can operate in Reverse Buck mode, Reverse Boost mode, Reverse Buck-Boost mode, or Reverse Bypass mode. RVSEN is the digital input pin. The 1.3s or 150ms debounce time can be set by Control2 register Bit<13>. After the reverse output voltage reaches the output voltage set by register 0X49H Bit<14:3>, reverse power-good RVSPG asserts to High.

Before Reverse mode starts switching, the CSIP pin voltage needs to drop below the reverse output overvoltage protection threshold (ReverseRegulatingVoltage + 1177mV) first.

The default reverse output voltage is 5V and programmable up to 20V in Reverse Buck, Reverse Buck-Boost, and Reverse Boost mode. In Reverse Bypass mode, the reverse output voltage's maximum value is programmable up to 20V. The reverse voltage register 0X49H can be used to configure the reverse output voltage.

6.8 Fast REF

To achieve fast REF in some applications, the fast REF function can be programmed by Control1 Bit 3. If this bit is programmed, a 1µA current source for the REF pin is replaced with 5k impedance to get faster transitions for REF voltage.

6.9 Fast Swap

The ISL95338 provides fast swap function in Forward mode and Reverse mode. You can implement the fast swap function in Forward mode in one of two ways (pin reverse or software reverse) by completing the following steps:

- Pin reverse fast swap enable:
  1. Program Control2 Bit 4 (Reverse Fast Swap).
  2. Skip trim during restart by programming Control1 Bit 13.
  3. Skip autozero during restart by programming Control1 Bit 12.
  4. Enable RVSEN pin.
- Software reverse fast swap enable:
  1. Program Control1 Bit 0 (Force 5.04V VDAC).
  2. Program Control1 Bit 3 (Fast REF).
  3. Skip trim during restart with programming Control1 Bit 13.
  4. Skip autozero during restart with programming Control1 Bit 12.
  5. Program Control1 Bit 11 (Force Reverse mode).

Similarly, you can implement the fast swap function in Reverse mode in one of two ways (pin reverse or software reverse) by following the steps below:

- Pin forward fast swap enable:
  1. Program Control2 Bit 3 (Forward Fast Swap).
  2. Skip trim during restart by programming Control1 Bit 13.
  3. Skip autozero during restart by programming Control1 Bit 12.
  4. Disable the RVSEN pin.
  5. Enable the FWREN pin.
- Software forward fast swap enable:
  1. Program Control1 Bit 0 (Force 5.04V VDAC).
  2. Program Control1 Bit 3 (Fast REF).
  3. Skip trim during restart by programming Control1 Bit 13.
  4. Skip autozero during restart by programming Control1 Bit 12.
  5. Un-program Control1 Bit 11 (Force Reverse mode).

6.10 Way Overcurrent Protection (WOCP)

The ISL95338 provides Way Overcurrent Protection (WOCP) against MOSFET shorts, system side and ADP side shorts, and inductor shorts. The ISL95338 monitors the CSIP-CSIN voltage and CSON-CSOP voltage and compares them to the WOCP threshold 12A for ADP current and 20A for system side current in Forward mode.

When the WOC comparator is tripped, the ISL95338 counts one time within each 10µs window. If the ISL95338 counts WOC to 7 times in 50ms, it stops switching immediately. After the 1.3s or 150ms debounce time is set by Control2 register Bit<12>, the ISL95338 goes through the start-up sequence to retry.

The WOCP function can be disabled through Control2 register Bit<1>.

6.11 ADP Input Overvoltage Protection

If the ADP pin input voltage exceeds 26.4V for more than 10µs, the ISL95338 declares an ADP overvoltage condition and stops switching. When the ADP voltage drops below 25.608V for more than 100µs, the ISL95338 starts to switch.

6.12 System Output Overvoltage Protection

The ISL95338 provides system rail output overvoltage protection. If the system voltage VOUTS is 1095mV higher than the ForwardRegulatingVoltage register set value for more than 100µs, it declares the system overvoltage, de-asserts FWRPG, and stops switching. It resumes switching with the 100µs debounce when the VOUTS is less than 542mV plus the setting reference voltage for forward.

6.13 System Output Undervoltage Protection

The ISL95338 provides system rail output undervoltage protection. If the system voltage VOUTS is 818mV lower than the ForwardRegulatingVoltage register set value for more than 1ms, it declares the system undervoltage, de-asserts FWRPG, and restarts.

6.14 ADP Output Overvoltage Protection

The ISL95338 provides ADP rail output overvoltage protection. If the ADP voltage ADPS is 1177mV higher than the ReverseRegulatingVoltage register set value for more than 100µs, it declares the ADP overvoltage, de-asserts RVSPG, and stops switching. The ISL95338 resumes switching with the 100µs debounce when ADPS is less than 583mV plus the setting reference voltage for reverse.

6.15 ADP Output Undervoltage Protection

The ISL95338 provides ADP rail output undervoltage protection. If the ADP voltage VADPS is 1177mV lower than the ReverseRegulatingVoltage register set value for more than 1ms, it declares the ADP undervoltage, de-asserts RVSPG, and stops switching.

6.16 Over-Temperature Protection

The ISL95338 stops switching for self protection when the junction temperature exceeds +140°C. The ISL95338 resumes switching when the temperature falls below +120°C and after a 100µs delay.

6.17 Switching Power MOSFET Gate Capacitance

The ISL95338 includes an internal 5V LDO output at the VDD pin that can provide the switching MOSFET gate driver power through the VDDP pin with an R-C filter. The 5V LDO output overcurrent protection threshold is 115mA nominal. When selecting the switching power MOSFET, the MOSFET gate capacitance should be considered carefully to avoid overloading the 5V LDO, especially in Buck-Boost mode when four MOSFETs are switching at the same time. For one MOSFET, the gate drive current can be estimated by Equation 1:

(EQ. 1) $$I_{driver} = Q_g \bullet f_{SW}$$

where:

Q_g is the total gate ADP which can be found in the MOSFET datasheet

f_{SW} is switching frequency

Renesas recommends connecting a 2.2µF ceramic capacitor from the VDD and VDDP pins to GND. The effective capacitance of the MLCC at 5V must be at least 0.4µF after derating and at least 1.6 times the effective capacitance at the BOOT pin. Use a X7R or X5R ceramic capacitor.

6.18 ADP Side Input Filter

The ADP cable parasitic inductance and capacitance can cause some voltage ringing or an overshoot spike at the ADP connector node when the ADP is hot plugged in. This voltage spike can damage the ISL95338 pins connecting to the ADP connector node. One low cost solution is to add an R-C snubber circuit at the ADP connector node to clamp the voltage spike as shown in Figure 31. A practical value of the R-C snubber is 2.2Ω to 2.2µF; however, the appropriate values and power rating should be carefully characterized based on the actual design. Additionally, it is not recommended to add a pure capacitor at the ADP connector node, which can cause an even bigger voltage spike due to the ADP cable or the ADP current path parasitic inductance.

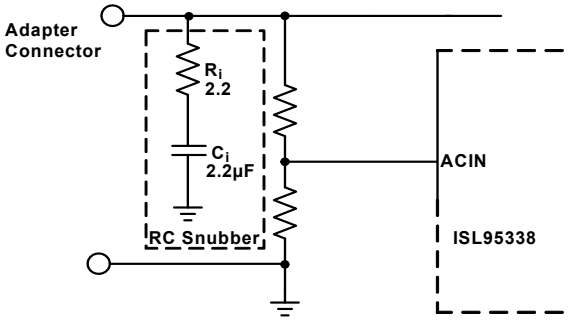


Figure 31. Adapter Input RC Snubber Circuit

7. General Application Information

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following sections. In addition to this guide, complete reference designs that include schematics, bill of materials, and example board layouts are provided.

7.1 Select the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 2:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 2)}$$

The output inductor peak-to-peak ripple current is written by Equation 3:

$$I_{P\text{-}P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L} \quad \text{(EQ. 3)}$$

A typical step-down DC/DC converter has an $I_{P\text{-}P}$ of 20% to 40% of the maximum DC output load current for a practical design. The value of $I_{P\text{-}P}$ is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 4:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \text{(EQ. 4)}$$

where I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O, into which ripple current $I_{P\text{-}P}$ can flow. Current $I_{P\text{-}P}$ develops a corresponding ripple voltage $V_{P\text{-}P}$ across $C_{O,}$ which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from ADP moved in and out of the capacitor. These two voltages are written by Equations 5 and 6:

$$\Delta V_{ESR} = I_{P\text{-}P} \cdot ESR \quad \text{(EQ. 5)}$$

$$\Delta V_{C} = \frac{I_{P\text{-}P}}{8 \cdot C_O \cdot f_{SW}} \quad \text{(EQ. 6)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required $V_{P\text{-}P}$ is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that $I_{P\text{-}P}$ is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

7.2 Select the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. The typical application circuit (Figure 1 on page 2) is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function of duty cycle and is adjusted for converter efficiency. The normalized RMS ripple current calculation is written as Equation 7:

$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1 - D) + \frac{D \cdot k^2}{12}}}{I_{MAX}} \quad \text{(EQ. 7)}$$

where:

I_{MAX} is the maximum continuous I_{LOAD} of the converter

k is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a ratio of I_{MAX} (0 to 1)

D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as Equation 8:

$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF} \quad \text{(EQ. 8)}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

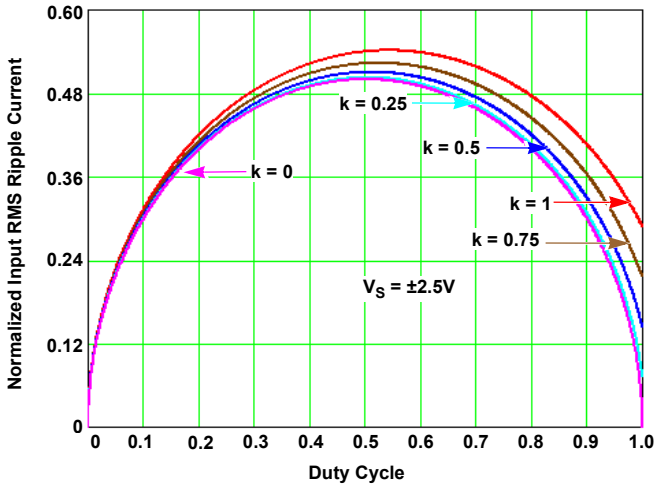


Figure 32. Normalized RMS Input Current at EFF = 1

7.3 Select the Switching Power MOSFET

Typically, a MOSFET cannot tolerate even brief excursions beyond its maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs are readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate ADP so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its

body diode during turn off, the high-side MOSFET turns off with a VDS of approximately V_{IN} - V_{OUT}, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. Note that this is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for high-side and low-side devices may be warranted.

For the low-side (LS) MOSFET, the power loss can be assumed to be conductive only and is written as Equation 9:

(EQ. 9) $$P_{CON\_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)\_LS} \cdot (1 - D)$$

For the high-side (HS) MOSFET, the conduction loss is written as Equation 10:

(EQ. 10) $$P_{CON\_HS} = I_{LOAD}^{2} \cdot r_{DS(ON)\_HS} \cdot D$$

For the high-side MOSFET, the switching loss is written as Equation 11:

(EQ. 11) $$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{SW(ON)} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{SW(OFF)} \cdot f_{SW}}{2}$$

where:

I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current

I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current

$t_{SW(ON)}$ is the time required to drive the device into saturation

$t_{SW(OFF)}$ is the time required to drive the device into cut-off

7.4 Select the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 12:

(EQ. 12) $$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}}$$

where:

Q_g is the total gate required to turn on the high-side MOSFET

ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on

As an example, suppose the high-side MOSFET has a total gate ADP Q_g of 25nC at V_{GS} = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF is enough.

Renesas recommends using a 0.47µF ceramic capacitor at the BOOT pin. The effective capacitance of the MLCC at 5V must be at least 0.25µF after derating and at least 50 times the effective high-side MOSFET gate capacitance. Use a X7R or X5R ceramic capacitor.

7.5 Select the Resistor Divider for VOUTS and ADPS

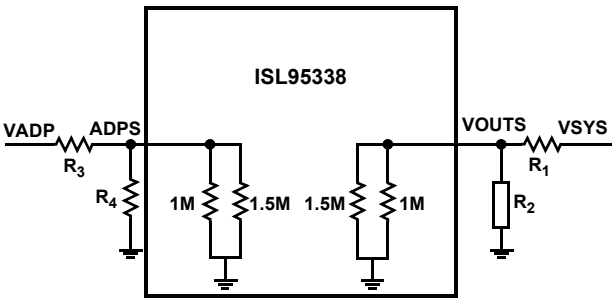


Figure 33. Resistor Divider for VOUTS and ADPS

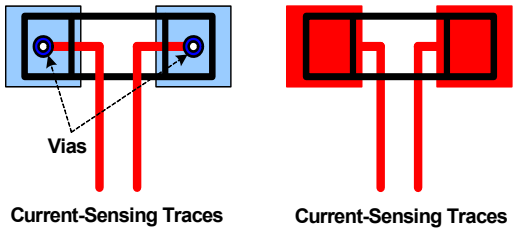
ADPS and VOUTS are output voltage feedback pins, in Reverse mode and Forward mode, respectively, that allow you to change output voltage by the resistor divider (R_1, R_2, and R_3, R_4), as shown in Figure 2. There are two parallel resistors (1M and 1.5M) inside from VOUTS and ADPS to ground. For example, in Forward mode, VSYS voltage magnitude can be revised by tuning R_1 and R_2 values, written by Equation 13. Thus, there is no need to change the Forward Regulating Voltage register (0x15H) through the GUI. The same process can be applied at the ADPS pin.

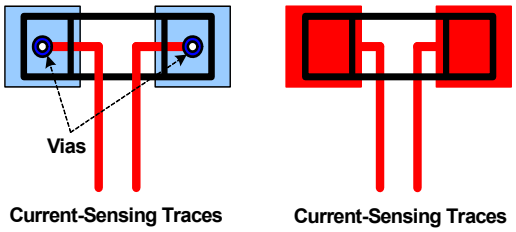
(EQ. 13) $$V_{OUTS} = V_{SYS}\frac{(1.5M\backslash\backslash 1M\backslash\backslash R_2)}{(1.5M\backslash\backslash 1M\backslash\backslash R_2) + R_1}$$

7.6 Selecting the DCIN Filter

When the ADP is plugged in, it can cause some voltage spike at the DCIN node. This voltage spike can damage the associated pins and the ISL95338 internal LDO. Therefore, a simple R-C filter must be connected at the DCIN pin to minimize the effect of the voltage spike. Renesas recommends using a 4.7Ω resistor and a 4.7µF ceramic capacitor as the R-C filter at the DCIN pin. The effective capacitance of the MLCC at 20V must be at least 0.4µF after derating. Use a X7R or X5R ceramic capacitor.

8. Layout

Pin Number	Pin Name	Layout Guidelines
BOTTOM PAD	GND	Connect this ground pad to the ground plane through a low impedance path. Renesas recommends using at least five vias to connect to the ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
1	CSON	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current-sensing resistor to the IC. Place the differential mode and common-mode RC filter components in the general proximity of the controller. Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
2	CSOP	
3	VOUTS	Signal pin that provides feedback for the forward system bus voltage. Run a dedicated trace from the system bus to the pin and do not route near the switching traces. Do not share the same trace with the signal routing to the DCIN pin OR diodes.
4	BOOT2	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
5	UGATE2	Run these two traces in parallel with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing the PHASE2 trace to high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFETs gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the output capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use the shortest PCB trace connection. Place these capacitors on the same PCB layer as the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation, but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
6	PHASE2	
7	LGATE2	Switching pin. Run the LGATE2 trace in parallel with the UGATE2 and PHASE2 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.
8	VDDP	Place the decoupling capacitor in the general proximity of the controller. Run the trace connecting to the VDD pin with sufficient width.
9	LGATE1	Switching pin. Run the LGATE1 trace in parallel with the UGATE1 and PHASE1 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.

Pin Number	Pin Name	Layout Guidelines
10	PHASE1	Run these two traces in parallel with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing the PHASE1 trace to the high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use the shortest PCB trace connection. Place these capacitors on the same PCB layer as the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
11	UGATE1	
12	BOOT1	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
13	ADPS	Run this trace with sufficient width parallel to the ADP pin trace.
14	CSIN	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current-sensing resistor to the IC. Place the Differential mode and common-mode RC filter components in the general proximity of the controller. Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
15	CSIP	
16	ADP	Run this trace with sufficient width parallel to the ADPS pin trace.
17	DCIN	Place the OR diodes and the RC filter in the general proximity of the controller. Run the VADP trace and VSYS trace to the OR diodes with sufficient width.
18	VDD	Place the RC filter connecting with the VDDP pin in the general proximity of the controller. Run the trace connecting to the VDDP pin with sufficient width.
19	FRWEN	No special consideration.
20	RVSEN	No special consideration.
21	SDA	Digital pins. No special consideration. Run the SDA and SCL traces in parallel.
22	SCL	
23	PROCHOT#	Digital pin, open-drain output. No special consideration.
24	FRWPG	Digital pin, open-drain output. No special consideration.
25	ADDR0	No special consideration.
26	RVSPG	Digital pin, open-drain output. No special consideration.
27	PROG	Signal pin. Place the PROG programming resistor in the general proximity of the controller.
28	COMPF	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.

Pin Number	Pin Name	Layout Guidelines
29	REF	Place the reference capacitor in the general proximity of the controller.
30	COMPR	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.
31	VOUT	Run a dedicated trace from the system bus to the pin and do not route near the switching traces.
32	ADDR1	No special consideration.

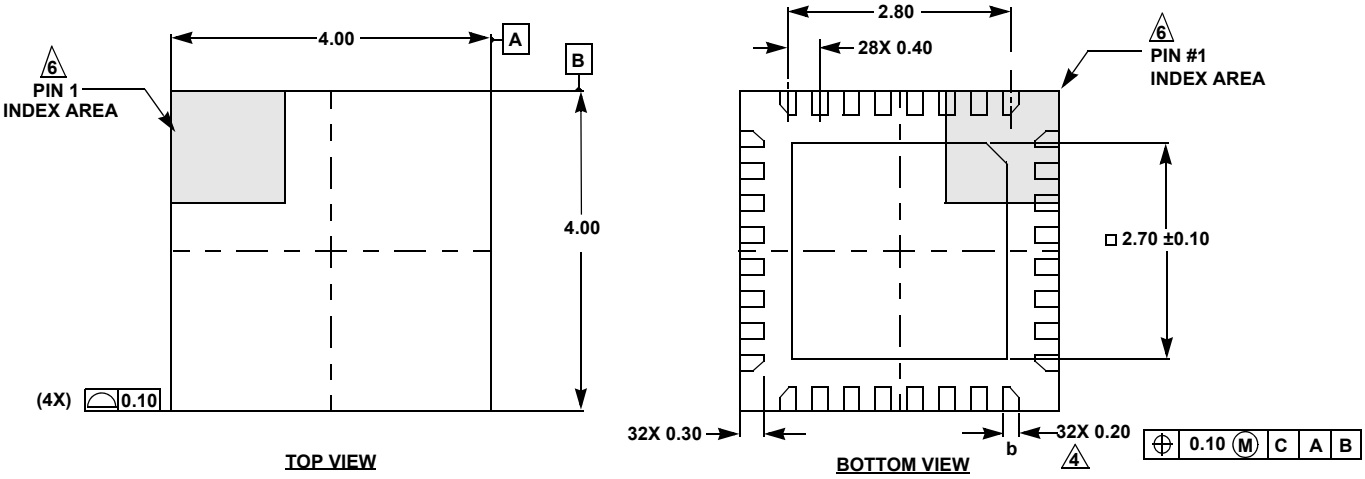
9. Revision History

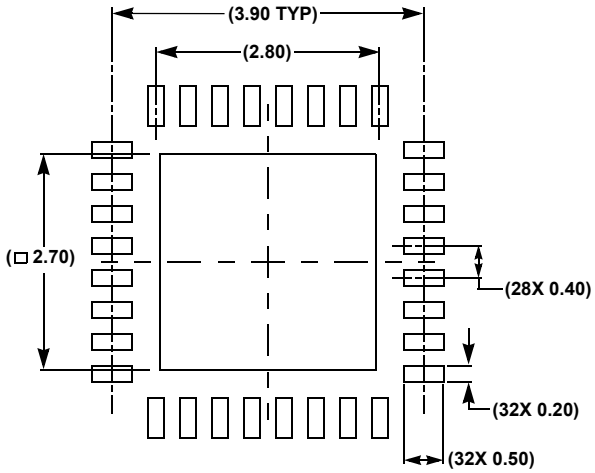
Rev.	Date	Description
4.00	Jul.18.19	Fixed incorrect cross references to Figure 23 throughout document. Updated block diagram (Figure 2 on page 5). Updated pin descriptions for pins 8, 17, and 18 on pages 7 and 8. Updated Figure 19 on page 17. Updated ForwardInputCurrent register's default value to 1.5A on page 20. Changed "<12:4>" to "12:2>" in Tables 5 and 6 on page 23. Added a paragraph to section 6.17 on page 40 and section 7.4 on page 44. Added section 7.6 "Selecting the DCIN Filter" on page 45. Added section 8 "Layout" on pages 46 through 48. Applied new template.
3.00	Oct.26.18	Changed 24V to 20V in the description on page 1. Updated the Ordering Information table on page 6 by adding tape and reel information to the table, updating Note 1, removing Note 2, and updating the package drawing information. Under "Absolute Maximum Ratings" on page 9 updated the following: - Changed VOUT, VOUTS, CSOP, CSON maximum specification from +27V to +24V. - Changed BOOT1, BOOT2 maximum specification from VDDP + 27V to VDDP + 25V. - Changed BOOT1-PHASE1, BOOT2-PHASE2 maximum specification from +0.3V to +6.5V and moved it up in the table. - Updated CSIP-CSIN, CSOP-CSON by adding a minimum specification and changing the maximum specification from 2mA to +0.3V. - Added a new row (RVSEN, FRWEN, SDA, SCL, FRWPG, RVSPG, PROCHOT#). Replaced POD L32.4x4A with the L32.4x4D. Removed About Intersil section and updated the disclaimer.
2.00	Nov.30.17	Added Way Overcurrent Protection (WOCP) function to datasheet.
1.00	Oct.5.17	Removed Way Overcurrent Protection (WOCP) function
0.00	Aug.15.17	Initial release

10. Package Outline Drawing

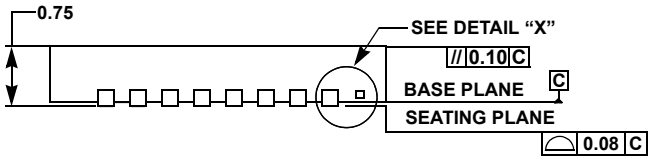
For the most recent package outline drawing, see L32.4x4D.

L32.4x4D
32 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/16

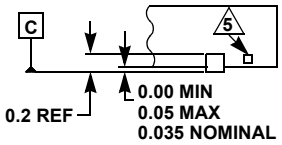




TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05.
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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