

High-Performance TTL and FAST Delay Lines

*TTLDL and
FSTD
14-pin DIP*

- 5 to 500 ns delays available.
- Five equal taps in 20% increments of total delay.
- Lumped constant, active series.
- Transfer-molded packaging for highest reliability.
- Available in low profile, .250 inch high military (MX) series for delays up to 100 ns – contact factory.
- Temperature coefficient ± 2 ns or $\pm 2\%$ (whichever is greater) at maximum delay, 0 to 70°C.
- Designed for leading edge timing. Trailing edge timing available.
- Compatible with Schottky TTL, FACT, ALS, and AS circuits.
- Military models with temperature range -55 to +125°C and ceramic package IC. Add suffix “M” to part number.
- Military models as above, but with ceramic package IC screened to MIL-STD 883C. Add suffix “MX” to part number.
- Military models as “MX” above, but with in-house burn-in and thermal shock, add suffix “MY”.
- 10-tap models available, contact factory for details.

HIGH PERFORMANCE 5-TAP TTL DELAY MODULES

PART NO.	TAP DELAYS (ns)					ALL TAPS	
	T _{D1}	T _{D2}	T _{D3}	T _{D4}	T _{D5}	T _{RO}	T _{FO}
TTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
TTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
TTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
TTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	2.0
TTLDL125	25.0	50.0	75.0	100.0	125.0	2.0	2.0
TTLDL150	30.0	60.0	90.0	120.0	150.0	2.0	5.0
TTLDL200	40.0	80.0	120.0	160.0	200.0	2.0	5.0
TTLDL250	50.0	100.0	150.0	200.0	250.0	2.0	5.0
TTLDL500	100.0	200.0	300.0	400.0	500.0	2.0	9.0

For TTL delay lines qualified to MIL-D-83532, refer to PSC information sheet entitled “QPL Active Delay Lines.”

Delay Characteristics measured at $V_{CC} = 5.0V$, 25°C, with 15 pf load per tap @ 1.5V level.
 Delay Tolerance ± 1.5 ns or 5%, whichever is greater.
 Rise time measured @ 0.8V to 2.0V levels.
 For minimum input pulse width -- contact factory. Designs with pulse widths of less than 15% of delay are available.



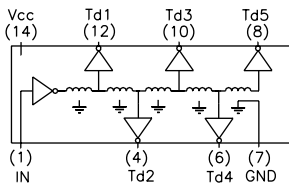
HIGH PERFORMANCE 5-TAP FAST DELAY MODULES

PART NO.	TAP DELAYS (ns)					ALL TAPS	
	T _{D1}	T _{D2}	T _{D3}	T _{D4}	T _{D5}	T _{RO}	T _{FO}
FSTDLO25	5.0	10.0	15.0	20.0	25.0	2.0	2.0
FSTDLO50	10.0	20.0	30.0	40.0	50.0	2.0	2.0
FSTDLO75	15.0	30.0	45.0	60.0	75.0	2.0	2.0
FSTDLO100	20.0	40.0	60.0	80.0	100.0	2.0	2.0
FSTDLO125	25.0	50.0	75.0	100.0	125.0	2.0	2.0
FSTDLO150	30.0	60.0	90.0	120.0	150.0	2.0	5.0
FSTDLO200	40.0	80.0	120.0	160.0	200.0	2.0	5.0
FSTDLO250	50.0	100.0	150.0	200.0	250.0	2.0	5.0
FSTDLO500	100.0	200.0	300.0	400.0	500.0	2.0	9.0

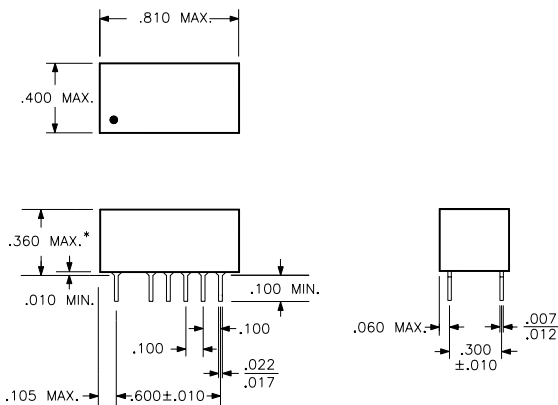
*TTLDL and
FSTDL
14-pin DIP*

Delay Characteristics measured at V_{CC} = 5.0V, 25°C, with 15 pf load per tap @ 1.5V level.
 Delay Tolerance ±1.5 ns or 5%, whichever is greater.
 Rise time measured @ 0.8V to 2.0V levels.
 For minimum input pulse width -- contact factory. Designs with pulse widths of less than 15% of delay are available.

SCHEMATIC



MECHANICAL OUTLINE



* FOR DELAY VALUES OF 100ns OR GREATER, MAX. HEIGHT IS 0.380 IN.

Notes

- Only the pins specified in the schematics are provided with each package.
- Pin numbers shown are for reference only and are not necessarily marked on unit.
- Lead material is electro tin plated (alloy 42) or solder dipped.
- All specifications are subject to change without notice.

TTLDL-5