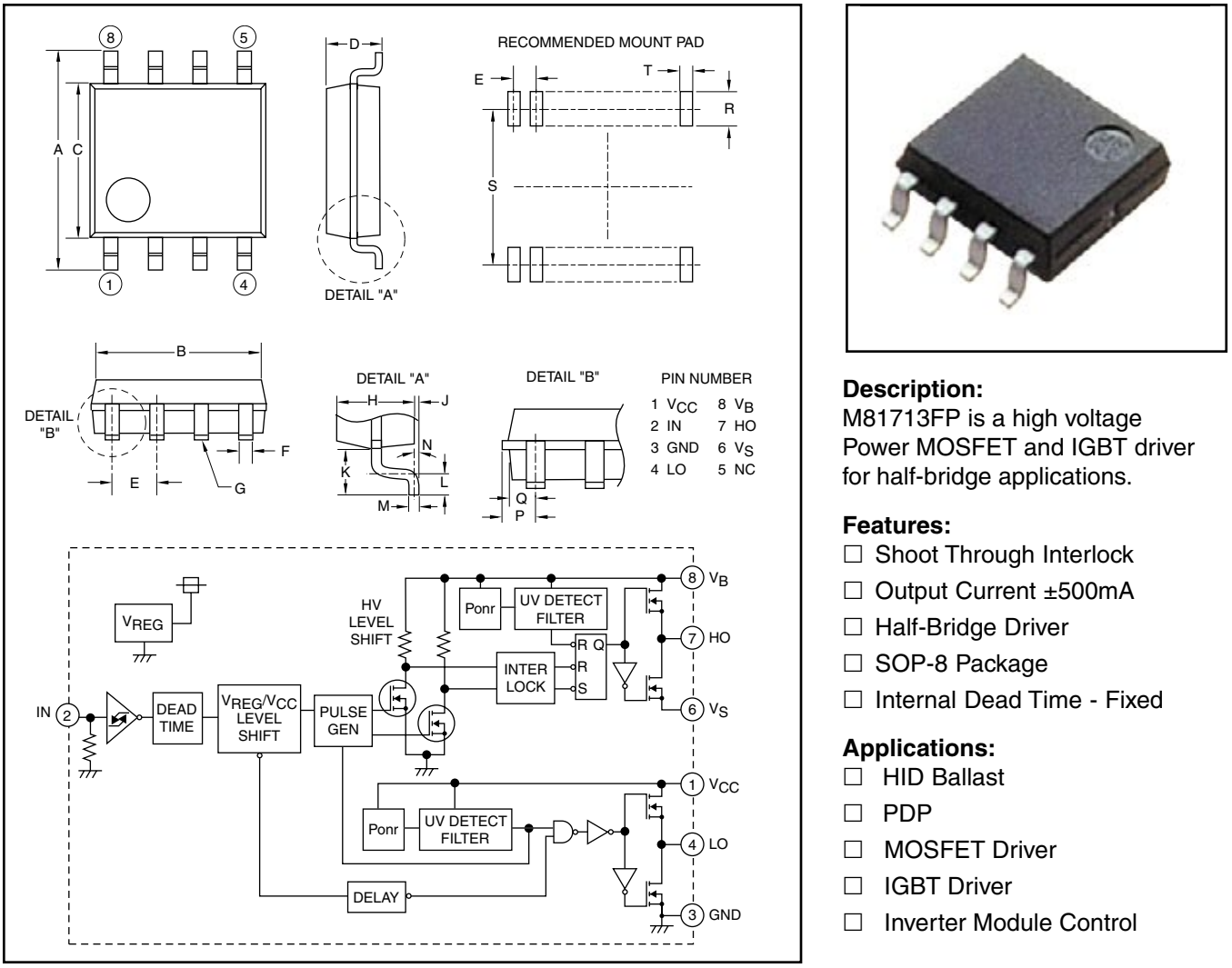
Powerex, Inc., 200 E. Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

HVIC

High Voltage
Half-Bridge Driver
600 Volts/±500mA



Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	0.24±0.01	6.2±0.3
B	0.2±0.008	5.0±0.2
C	0.17±0.008	4.4±0.2
D	0.08 Max.	1.9 Max.
E	0.05	1.27
F	0.015±0.002	0.4±0.05
G	0.004	0.1
H	0.06	1.5
J	0.002 Min.	0.05 Min.

Dimensions	Inches	Millimeters
K	0.04	0.9
L	0.015±0.008	0.4±0.2
M	0.006±0.002	0.15±0.05
N	10° Max.	10° Max.
P	0.03	0.745
Q	0.023	0.595
R	0.05 Min.	1.27 Min.
S	0.23	5.72
T	0.76	0.76

Description:
M81713FP is a high voltage Power MOSFET and IGBT driver for half-bridge applications.

Features:
- ☐ Shoot Through Interlock
- ☐ Output Current ±500mA
- ☐ Half-Bridge Driver
- ☐ SOP-8 Package
- ☐ Internal Dead Time - Fixed

Applications:
- ☐ HID Ballast
- ☐ PDP
- ☐ MOSFET Driver
- ☐ IGBT Driver
- ☐ Inverter Module Control

Ordering Information:
M81713FP is a ±500mA, 600 Volt HVIC, High Voltage Half-Bridge Driver

Absolute Maximum Ratings, T_a = 25°C unless otherwise specified

Characteristics	Symbol	M81713FP	Units
High Side Floating Supply Absolute Voltage	V_B	-0.5 ~ 624	Volts
High Side Floating Supply Offset Voltage	V_S	V_B-24 ~ V_B+0.5	Volts
High Side Floating Supply Voltage ($V_{BS} = V_B - V_S$)	V_{BS}	-0.5 ~ 24	Volts
High Side Output Voltage	V_{HO}	V_S-0.5 ~ V_B+0.5	Volts
Low Side Fixed Supply Voltage	V_{CC}	-0.5 ~ 24	Volts
Low Side Output Voltage	V_{LO}	-0.5 ~ V_{CC}+0.5	Volts
Logic Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	Volts
Allowable Offset Voltage Transient	dVs/dt	±50	V/ns
Package Power Dissipation (T_a = 25°C, On Board)	P_d	0.6	Watts
Linear Derating Factor (T_a > 25°C, On Board)	$K\theta$	6.0	mW/°C
Junction to Case Thermal Resistance	$R_{th(j-c)}$	50	°C/W
Junction Temperature	T_j	-20 ~ 150	°C
Operation Temperature	T_{opr}	-20 ~ 125	°C
Storage Temperature	T_{stg}	-40 ~ 150	°C

Recommended Operating Conditions

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High Side Floating Supply Absolute Voltage	V_B		V_S+10	—	V_S+20	Volts
High Side Floating Supply Offset Voltage	V_S	V_B > 10V	-5	—	500	Volts
High Side Floating Supply Voltage	V_{BS}	$V_B = V_B - V_S$	10	—	20	Volts
High Side Output Voltage	V_{HO}		V_S	—	V_B	Volts
Low Side Fixed Supply Voltage	V_{CC}		10	—	20	Volts
Logic Supply Voltage	V_{LO}		0	—	V_{CC}	Volts
Logic Input Voltage	V_{IN}		0	—	V_{CC}	Volts

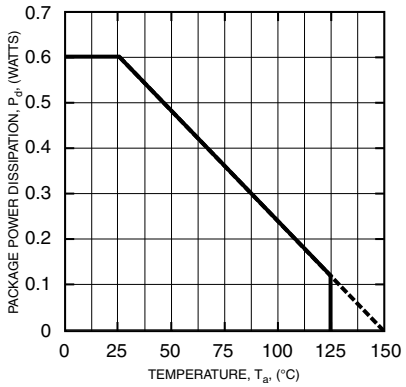
Electrical Characteristics, T_a = 25°C, $V_{CC} = V_{BS}$ (= $V_B - V_S$) = 15V unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Floating Supply Leakage Current	I_{FS}	$V_B = V_S$ = 600V	—	—	1.0	µA
V_{BS} Standby Current	I_{BS}	IN = 0V	—	0.2	0.5	mA
V_{CC} Standby Current	I_{CC}	IN = 0V	0.2	0.5	0.75	mA
High Level Output Voltage	V_{OH}	I_O = 0A, L_O, H_O	13.8	14.4	—	Volts
Low Level Output Voltage	V_{OL}	I_O = 0A, L_O, H_O	—	—	0.1	Volts
High Level Input Threshold Voltage	V_{IH}	H_{IN}, L_{IN}	2.1	3.0	4.0	Volts
Low Level Input Threshold Voltage	V_{IL}	H_{IN}, L_{IN}	0.6	1.5	2.0	Volts
High Level Input Bias Current	I_{IH}	V_{IN} = 5V	—	25	75	µA
Low Level Input Bias Current	I_{IL}	V_{IN} = 0V	—	—	1.0	µA
V_{BS} Supply UV Reset Voltage	V_{BSuvr}		8.0	8.9	9.8	Volts
V_{BS} Supply UV Hysteresis Voltage	V_{BSuvh}		0.5	0.7	—	Volts
V_{BS} Supply UV Filter Time	tV_{BSuv}		—	7.5	—	µs
V_{CC} Supply UV Reset Voltage	V_{CCuvr}		8.0	8.9	9.8	Volts
V_{CC} Supply UV Hysteresis Voltage	V_{CCuvh}		0.5	0.7	—	Volts

Electrical Characteristics, T_a = 25°C, V_{CC} = V_{BS} (= V_B – V_S) = 15V unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
V_{CC} Supply UV Filter Time	tV_{CCuv}		—	7.5	—	µs
Output High Level Short Circuit Pulsed Current	I_{OH}	V_O = 0V, P_W < 10µs	—	-500	—	mA
Output Low Level Short Circuit Pulsed Current	I_{OL}	V_O = 15V, P_W < 10µs	—	500	—	mA
Output High Level ON Resistance	R_{OH}	I_O = -200mA, R_{OH} = (V_{OH} – V_O)/I_O	—	30	—	Ω
Output Low Level ON Resistance	R_{OL}	I_O = 200mA, R_{OL} = V_O /I_O	—	12	—	Ω
Dead Time LO Turn-Off to HO Turn-ON and HO Turn-Off to LO Turn-On	t_{DEAD}	C_L = 1000pF between HO – V_S, LO-GND	0.5	—	1.0	µs
Power On Reset Voltage	V_{Ponr}		—	—	6	Volts
Power On Reset Filter Time	$t_{Ponr(FIL)}$		300	—	—	ns
Turn-On Propagation Delay	t_{dLH}	C_L = 1000pF between HO – V_S, LO – GND	0.6	0.9	1.2	µs
Turn-Off Propagation Delay	t_{dHL}	C_L = 1000pF between HO – V_S, LO – GND	0.1	0.15	0.2	µs
High Side Turn-On Rise Time	t_{rH}	C_L = 1000pF between LO – GND	—	75	180	ns
High Side Turn-Off Fall Time	t_{fH}	C_L = 1000pF between LO – GND	—	75	180	ns
Low Side Turn-On Rise Time	t_{rL}	C_L = 1000pF between LO – GND	—	75	180	ns
Low Side Turn-Off Fall Time	t_{fL}	C_L = 1000pF between LO – GND	—	75	180	ns

THERMAL DERATING FACTOR CHARACTERISTICS



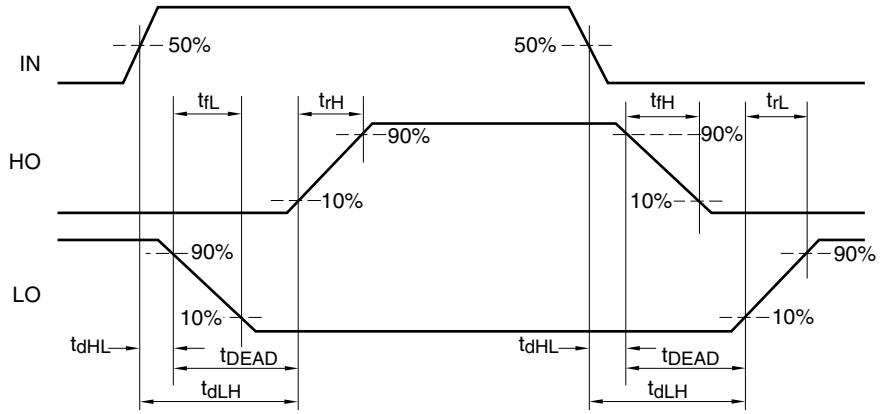
1. Input/Output Logic
   HO has positive logic with reference to IN. LO has negative logic with reference to IN.
2. Logic During UV (V_{CC}, V_{BS}) Error

Error Signal	HO	LO
UV Error (V_{CC})*	HO outputs "L" level as long as UV error for V_{CC} is detected. HO responds to IN if V_{CC} exceeds V_{CC} UV reset level.	LO is locked at "L" as long as UV error for V_{CC} is detected. After V_{CC} exceeds V_{CC} UV reset level, the lock for LO is removed and responds to IN signal.
UV Error (V_{BS})	HO is locked at "L" as long as UV error for V_{BS} is detected. After V_{BS} exceeds V_{BS} UV reset level, the lock for HO is removed following an "L" state of the IN signal, and then HO responds to the input.	LO is independent of V_{BS} to respond to IN.

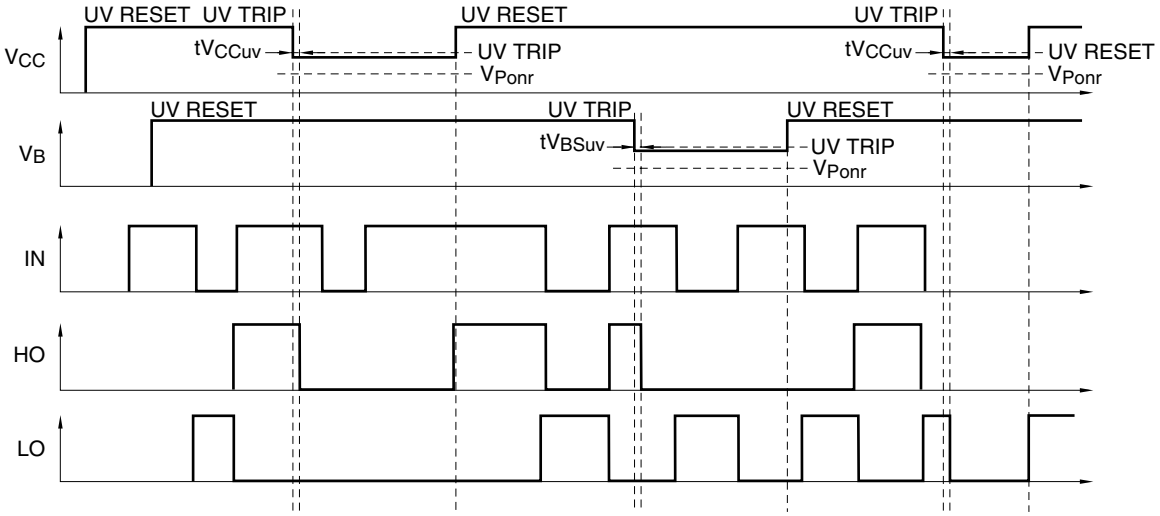
*If UV error for V_{CC} is detected when HO is in "H" level and the falling speed for V_{CC} exceeds 0.03V/µm, the OFF signal for HO might not be transimitted from low side to high side and then HO stays "H".

3. Allowable Supply Voltage Transient
   It is recommended supplying V_{CC} first and V_{BS} second. In the case of shutting off supply voltage, it is recommended to shut off V_{BS} first and V_{CC} second. At the time of starting, V_{CC} and V_{BS}, the power supply should be increased slowly (below 50V/µs). If it is increased rapidly, output signal (HO or LO) may be "H".

INPUT/OUTPUT TIMING DIAGRAM



UV SEQUENCE



Ponr (Power-On-Reset) SEQUENCE