MTMC8E28

Dual N-channel MOS FET

For lithium-ion secondary battery protection circuit

■ Overview

The MTMC8E28 features the industry's lowest on-resistance, which has been realized by leading-edge fine processing, and the adoption of ultra-miniature package, which is most suitable for battery packs for mobile devices.

■ Features

- Low on-resistance: R_{on} = 15 mΩ (typ.) (V_{GS} = 4.5 V)
- Mini type package and surface mounting type
  2.9 mm × 2.8 mm (height 0.8 mm)
- Drain common 2 elements
- Halogen free

■ Absolute Maximum Ratings T_a = 25°C

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	20	V
Gate-source surrender voltage	V_{GSS}	±10	V
Drain current	I_D	7.0	A
Peak drain current	I_{DP}	42	A
Power dissipation *	P_D	1.0	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) *: Glass epoxy board: 25.4 mm × 25.4 mm × 0.8 mm
Copper foil of the drain portion should have a area of 300 mm² or more
P_D absolute maximum rating without a heat shink: 400 mW

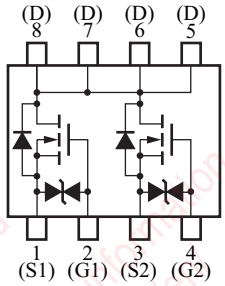
■ Package

- Code
  WMini8-F1
- Pin Name

1: Source 1	5: Drain
2: Gate 1	6: Drain
3: Source 2	7: Drain
4: Gate 2	8: Drain

■ Marking Symbo: 4A

■ Internal Connection

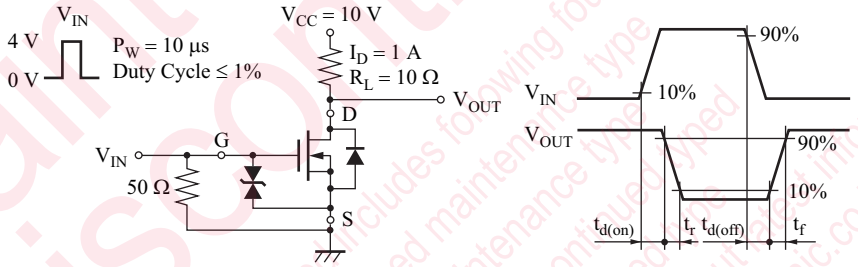


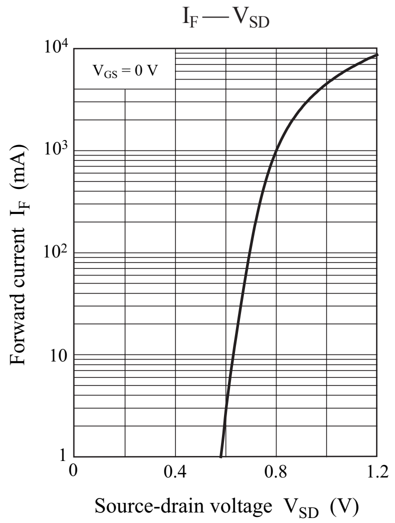
■ Electrical Characteristics T_a = 25°C±3°C

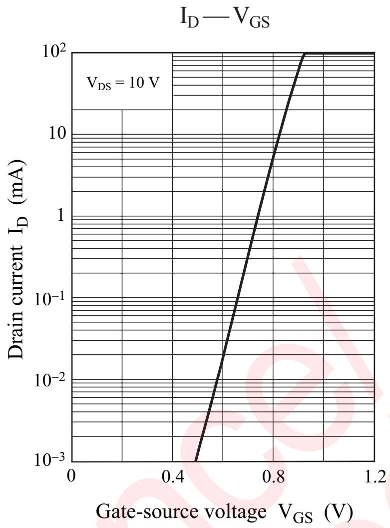
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = 1 mA, V_{GS} = 0	20			V
Drain-source cutoff current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0			1.0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0			±10	μA
Gate threshold voltage	V_{TH}	I_D = 1.0 mA, V_{DS} = 10.0 V	0.4	0.85	1.3	V
Drain-source ON resistance 1	$R_{DS(on)}1$	I_D = 2.0 A, V_{GS} = 4.5 V		15	21	mΩ
Drain-source ON resistance 2	$R_{DS(on)}2$	I_D = 2.0 A, V_{GS} = 3.7 V		18	25	mΩ
Drain-source ON resistance 3	$R_{DS(on)}3$	I_D = 1.0 A, V_{GS} = 2.5 V		22	33	mΩ
Forward transfer admittance	$\|Y_{fs}\|$	I_D = 1.0 A, V_{DS} = 10 V	3.0			S
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz		1 500		pF
Short-circuit output capacitance (Common source)	C_{oss}			110		pF
Reverse transfer capacitance (Common source)	C_{rss}			100		pF
Turn-on delay time *	$t_{d(on)}$	V_{DD} = 10 V, V_{GS} = 0 V to 4 V, I_D = 1.0 A		14		ns
Turn-off delay time *	$t_{d(off)}$	V_{DD} = 10 V, V_{GS} = 4 V to 0 V, I_D = 1.0 A		18		ns
Rise time *	t_r	V_{DD} = 10 V, V_{GS} = 0 V to 4 V, I_D = 1.0 A		130		ns
Fall time *	t_f	V_{DD} = 10 V, V_{GS} = 4 V to 0 V, I_D = 1.0 A		80		ns

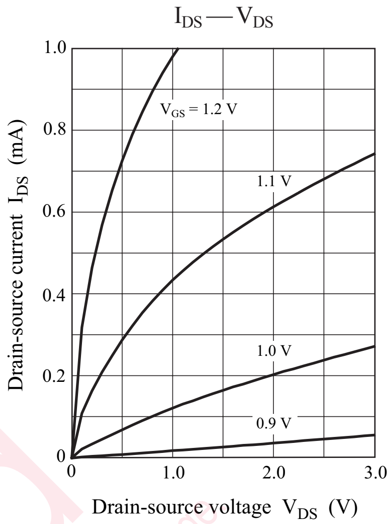
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

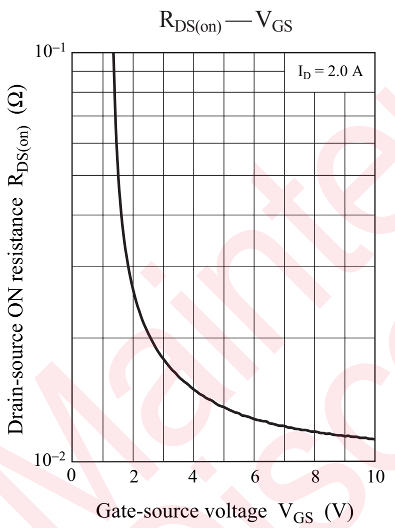
2. *: Test circuit

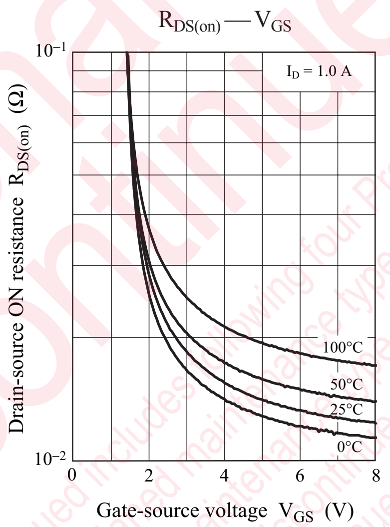


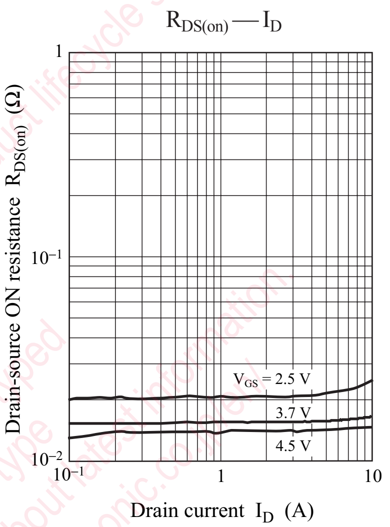


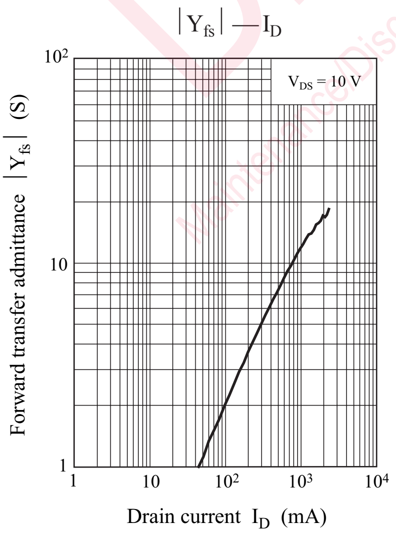


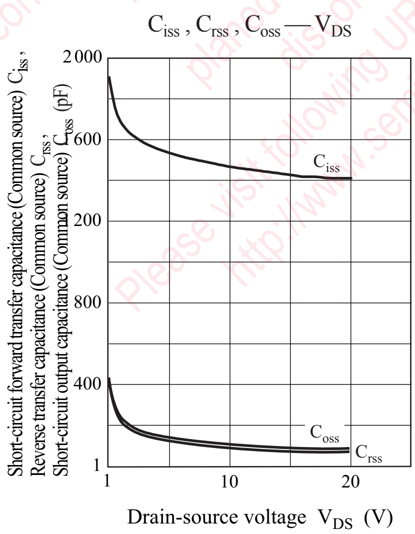






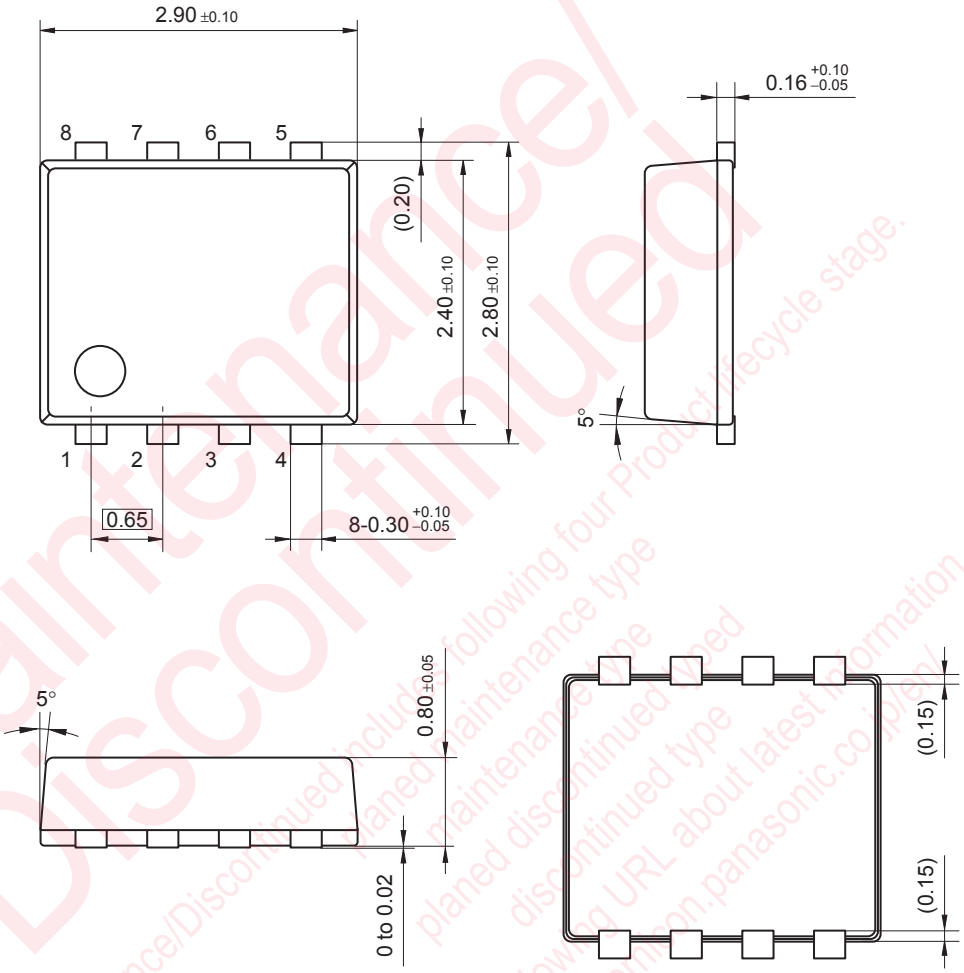





C_{iss}, C_{rss}, C_{oss} — V_{DS}
C_{iss}
C_{oss}
C_{rss}
Short-circuit forward transfer capacitance (Common source) C_{iss},
Reverse transfer capacitance (Common source) C_{rss},
Short-circuit output capacitance (Common source) C_{oss} (pF)
2 000
600
200
800
400
1
1
10
20
Drain-source voltage V_{DS} (V)

WMini8-F1

Unit: mm



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