NCV51511

High-Frequency, High Side and Low Side Gate Driver

The NCV51511 is high side and low side gate−drive IC designed for high−voltage, high−speed, driving MOSFETs operating up to 80 V.

The NCV51511 integrates a driver IC and a bootstrap diode. The driver IC features low delay time and matched PWM input propagation delays, which further enhance the performance of the part.

The high speed dual gate drivers are designed to drive both the high−side and low−side of N−Channel MOSFETs in a half bridge or synchronous buck configuration. The floating high−side driver is capable of operating with supply voltages of up to 80 V. In the dual gate driver, the high side and low side each have independent inputs to allow maximum flexibility of input control signals in the application. The PWM input signal (high level) can be 3.3 V, 5 V or up to V_{DD} logic input to cover all possible applications. The bootstrap diode for the high−side driver bias supply is integrated in the chip. The high−side driver is referenced to the switch node (HS) which is typically the source pin of the high−side MOSFET and drain pin of the low−side MOSFET. The low−side driver is referenced to V_{SS} which is typically ground. The functions contained are the input stages, UVLO protection, level shift, bootstrap diode, and output driver stages.

Features

- Drives two N−Channel MOSFETs in High & Low Side
- Integrated Bootstrap Diode for High Side Gate Drive
- Bootstrap Supply Voltage Range up to 100 V
- 3 A Source, 6 A Sink Output Current Capability
- Drives 1nF Load with Typical Rise/Fall Times of 6 ns/4 ns
- TTL Compatible Input Thresholds
- Wide Supply Voltage Range 8 V to 16 V (Absolute Maximum 18 V)
- Fast Propagation Delay Times (Typ. 30 ns)
- 2 ns Delay Matching (Typical)
- Under−Voltage Lockout (UVLO) Protection for Drive Voltage
- Industry−Standard Pinouts, SOIC 8 with Exposed PAD
- Automotive Qualified to AEC−Q100:
  - Operating temperature range from −40°C to 150°C
  - Reliability at 150°C for 2,016 hrs
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- 48 V Converters for HEV/EV
- Half−Bridge and Full−Bridge Converters
- Synchronous−Buck Converters

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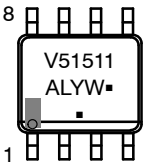
SOIC8−EP
CASE 751AC

MARKING DIAGRAM



V51511	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

TYPICAL APPLICATIONS

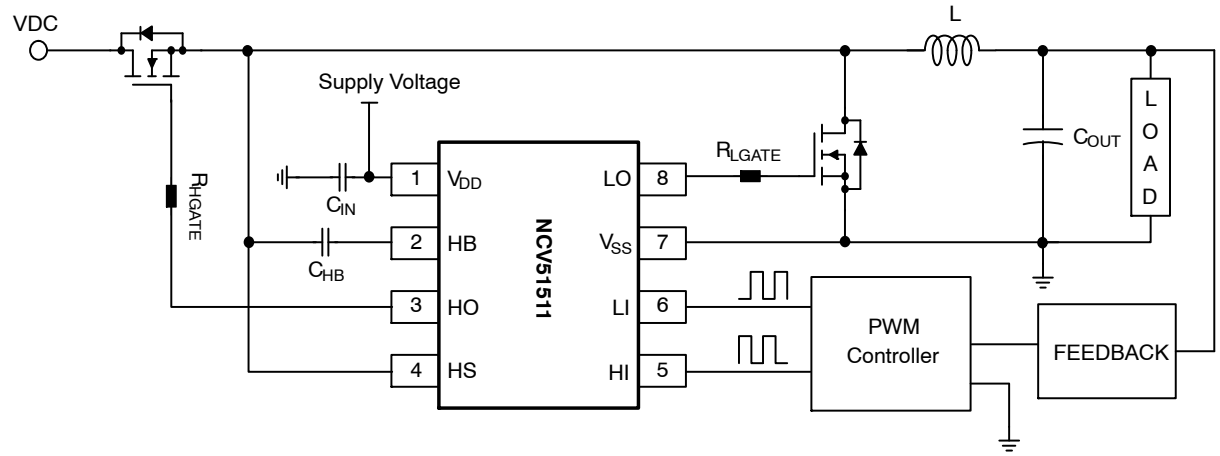


Figure 1. Application Schematic – Synchronous Buck Converter

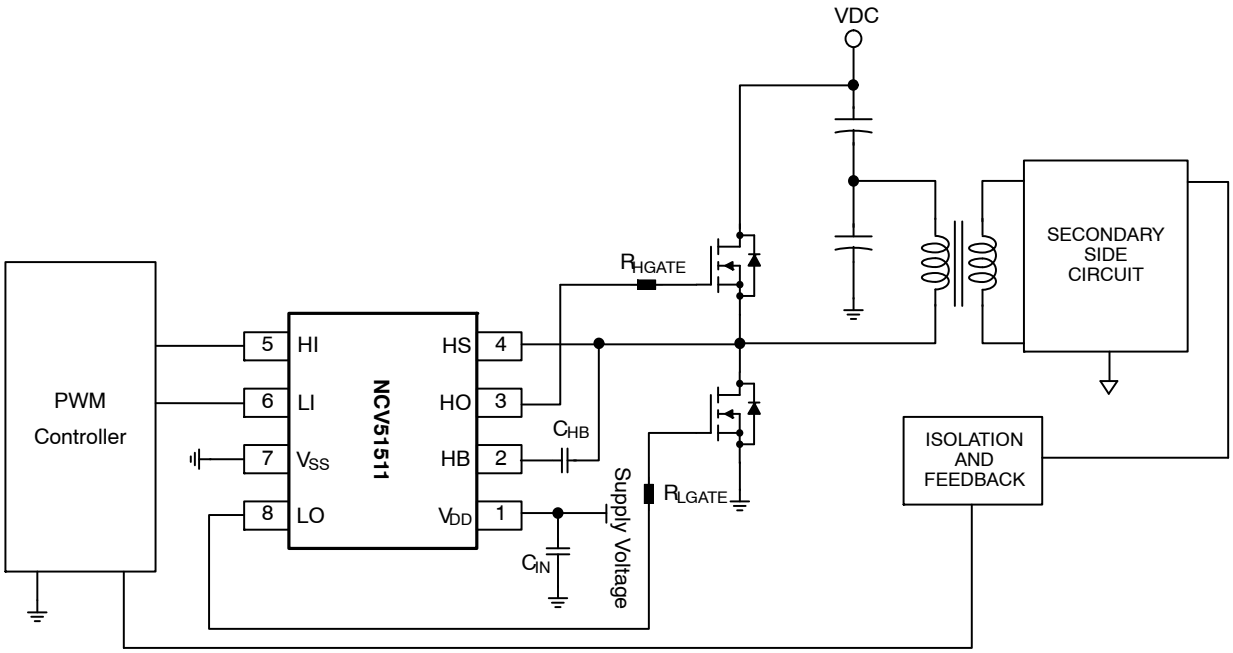


Figure 2. Application Schematic – Half Bridge Converter

BLOCK DIAGRAM

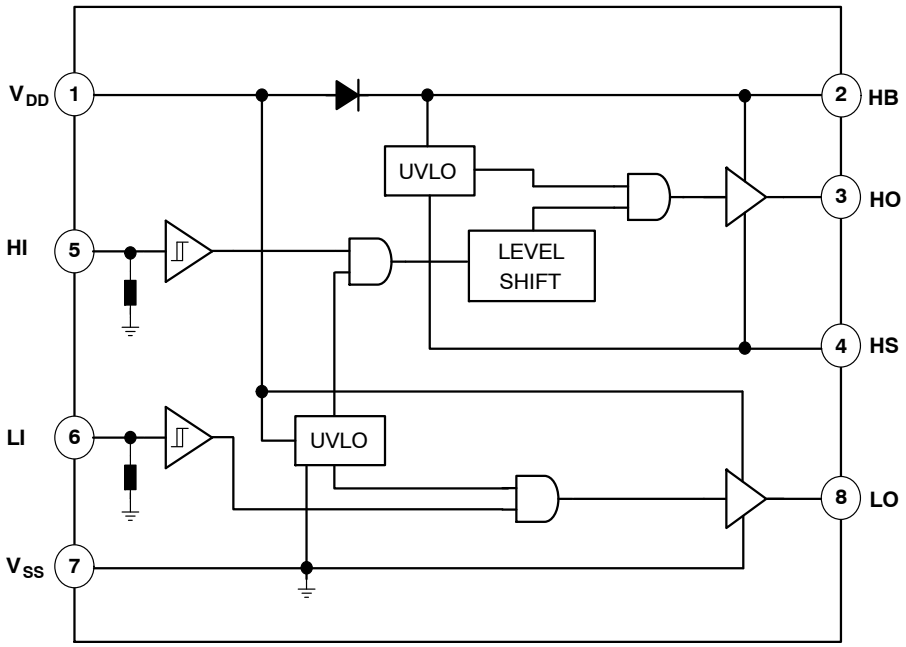


Figure 3. Simplified Block Diagram

PIN CONNECTIONS

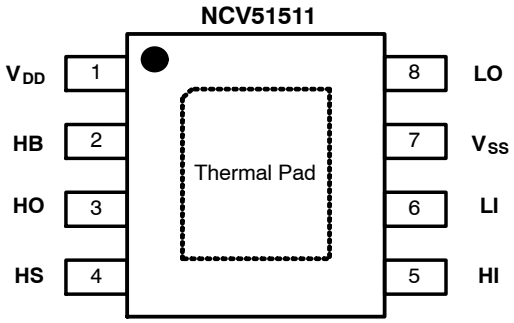


Figure 4. Pin Assignments – SOIC8–EP (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Pin Name	Description
1	V_{DD}	Logic and low–side gate driver power supply voltage
2	HB	High–side floating supply
3	HO	High–side driver output
4	HS	High–voltage floating supply return
5	HI	Logic input for High–side gate driver output
6	LI	Logic input for Low–side gate driver output
7	V_{SS}	Logic Ground
8	LO	Low–side driver output
–	Exposed PAD	Can either be left open or connected to V_{SS}. We recommend EPAD to be connected to V_{SS} plane for improved thermal performance.

Table 2. MAXIMUM RATINGS

All voltage parameters are referenced to V_{SS}, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Low−Side and Logic Fixed Supply Voltage	−0.3	18	V
V_{HS}	High−Side Floating Supply Offset Voltage(Note 1)	−1	100	V
	Repetitive Pulse (< 100 ns)(Note 2)	$-(24 - V_{DD})$	100	V
V_{LO}	Low−Side Output Voltage, LO Pin	−0.3	V_{DD} + 0.3	V
	Repetitive Pulse (< 100 ns)(Note 2)	−2	V_{DD} + 0.3	V
V_{HO}	High−Side Floating Output Voltage, HO Pin	V_{HS} − 0.3	V_{HB} + 0.3	V
	Repetitive Pulse (< 100 ns)(Note 2)	V_{HS} − 2	V_{HB} + 0.3	V
V_{LI}, V_{HI}	Logic Input Voltage	−0.3	V_{DD} + 0.3	V
V_{HB}	High−Side Floating Supply Voltage	−0.3	100	V
$V_{HB} - V_{HS}$	V_{HS} to V_{HB} Supply Voltage	−0.3	18	V
P_D	Power Dissipation (Note 3)		2.5	W
T_J,	Operating Junction Temperature	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The V_{HS} negative voltage capability can be calculated using (V_{HB} −V_{HS})−18 V base on V_{HB}, due to its dependence on V_{DD} voltage level.
2. Verified at bench characterization.
3. JEDEC standard: JESD51−2, JESD51−3. Mounted on 76.2 x 114.3 x1.6 mm PCB (FR−4 glass epoxy material).

Table 3. ESD AND MSL

Symbol	Parameters		Value	Unit.s
ESD_{HBM}	Electrostatic Discharge Capability	Human Body Model,per AEC Q100−002	2000	V
ESD_{CDM}		Charged Device Model, AEC Q100−011	1000	
MSL	Moisture Sensitivity Level		2	Level

Table 4. THERMAL INFORMATION (Note 4)

Symbol	Parameter	Value	Units
θ_{JA}	Thermal Resistance Junction−Air (Note 4)	39	°C/W
ψ_{JL}	Thermal characterization parameter Junction−Lead	15	°C/W
ψ_{JT}	Thermal characterization parameter Junction−Case (TOP)	6	°C/W

4. As mounted on a 76.2 x 114.3 x 1.6 mm FR4 substrate with a Multi−layer of 1 oz copper traces and heat spreading area. As specified for a JEDEC 51−7 conductivity test PCB. Test conditions were under natural convection or zero air flow

Table 5. RECOMMENDED OPERATING RANGES

All voltage parameters are referenced to V_{SS}

Symbol	Parameters	Test Condition	Min.	Max.	Units
V_{DD}	Supply Voltage	DC	8	16	V
V_{HS}	High Side Floating Return	DC	−1	80	V
		Repetitive Pulse (< 100 ns)	$-(24 - V_{DD})$	100	V
V_{HB}	Voltage on HB	DC	V_{HS} + 8	V_{HS} + 16	V
dV_{SW}/dt	Voltage Slew Rate on SW			50	V/ns
T_J	Operating Temperature		−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ELECTRICAL CHARACTERISTICS

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, T_A = T_J = −40°C to 150°C, no load on HO or LO, unless otherwise noted.

Symbol	Parameters	Test Condition	Min.	Typ.	Max.	Units
Power Supply Section						
I_{DD}	V_{DD} Quiescent Current	V_{HI} = 0 V; V_{LI} = 0 V		0.17	0.3	mA
I_{DDO}	V_{DD} Operating Current	f_{SW} = 500 kHz		1.5	3.0	mA
I_{HB}	HB Quiescent Current	V_{HI} = 0 V; V_{LI} = 0 V		0.1	0.2	mA
I_{HBO}	HB Operating Current	f_{SW} = 500 kHz		1.9	3.0	mA
I_{HBS}	HB to V_{SS} Quiescent Current	V_{HS} = V_{HB} = 80 V		0	10	μA
I_{HBSO}	HB to V_{SS} Operating Current	f_{SW} = 500 kHz		0.3	1.0	mA
V_{DDR}	V_{DD} UVLO Threshold	V_{DD} Rising	6.2	6.8	7.4	V
V_{DDH}	V_{DD} UVLO Hysteresis			0.6		V
V_{HBR}	HB UVLO Threshold	HB Rising	5.5	6.3	7.2	V
V_{HBH}	HB UVLO Hysteresis			0.4		V
Input Logic Section						
V_{IH}	High Level Input Voltage Threshold		1.80	2.2	2.50	V
V_{IL}	Low Level Input Voltage Threshold		1.3	1.7	2.0	V
V_{IHYS}	Input Logic Voltage Hysteresis			0.5		V
R_{IN}	Input Pull−down Resistance			100		kΩ
Bootstrap Diode						
V_{FL}	Forward Voltage @ Low Current	I_{VDD-HB} = 100 μA		0.55	0.8	V
V_{FH}	Forward Voltage @ High Current	I_{VDD-HB} = 100 mA		0.8	1.0	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.7	1.5	Ω
t_{BS} (Note 5)	Diode Turn−off Time	I_F = 20 mA, I_{REV} = 0.5 A		20		ns
Low Side Driver						
V_{OLL}	Low Level Output Voltage	I_{LO} = 100 mA		0.06	0.15	V
V_{OHL}	High Level Output Voltage	I_{LO} = −100 mA, V_{OHL} = V_{DD} − V_{LO}		0.16	0.28	V
I_{OHL} (Note 5)	Peak Pull−up Current	V_{LO} = 0 V		3		A
I_{OLL} (Note 5)	Peak Pull−down Current	V_{LO} = 12 V		6		A
t_{R_LO}	LO Rise Time	10% to 90%, C_{LOAD} = 1 nF		6		ns
t_{F_LO}	LO Fall Time	90% to 10%, C_{LOAD} = 1 nF		4		ns
t_{R_LO1}	LO Rise Time	3 V to 9 V, C_{LOAD} = 100 nF		300	500	ns
t_{F_LO1}	LO Fall Time	9 V to 3 V, C_{LOAD} = 100 nF		140	300	ns
t_{LPHL}	LI = Low Propagation Delay	V_{LI} Falling to V_{LO} Falling, C_{LOAD} = 0		28	45	ns
t_{LPLH}	LI = High Propagation Delay	V_{LI} Rising to V_{LO} Rising, C_{LOAD} = 0		30	47	ns
High Side Driver						
V_{OLH}	Low Level Output Voltage	I_{HO} = 100 mA		0.06	0.15	V
V_{OHH}	High Level Output Voltage	I_{HO} = −100 mA, V_{OHH} = V_{HB} − V_{HO}		0.16	0.28	V
I_{OHH} (Note 5)	Peak Pull−up Current	V_{HO} = 0 V		3		A
I_{OLH} (Note 5)	Peak Pull−down Current	V_{HO} = 12 V		6		A
t_{R_HO}	HO Rise Time	10% to 90%, C_{LOAD} = 1 nF		6		ns
t_{F_HO}	HO Fall Time	90% to 10%, C_{LOAD} = 1 nF		4		ns
t_{R_HO1}	HO Rise Time	3 V to 9 V, C_{LOAD} = 100 nF		300	500	ns
t_{F_HO1}	HO Fall Time	9 V to 3 V, C_{LOAD} = 100 nF		140	300	ns
t_{HPHL}	HI = Low Propagation Delay	V_{HI} Falling to V_{HO} Falling, C_{LOAD} = 0		28	45	ns
t_{HPLH}	HI = High Propagation Delay	V_{HI} Rising to V_{HO} Rising, C_{LOAD} = 0		30	47	ns

Table 6. ELECTRICAL CHARACTERISTICS

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, T_A = T_J = −40°C to 150°C, no load on HO or LO, unless otherwise noted.

Symbol	Parameters	Test Condition	Min.	Typ.	Max.	Units
Delay Matching						
t_{MON}	HI Turn−OFF to LI Turn−ON			2	10	ns
t_{MOFF}	LI Turn−OFF to HI Turn−ON			2	10	ns
Minimum Pulse Width						
t_{PW}	Minimum Pulse Width for HI and LI (Note 5)				50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These parameters are guaranteed by design.

TYPICAL CHARACTERISTICS

Typical characteristics are provided at 25°C and V_{DD}, V_{HB} = 12 V unless otherwise noted.

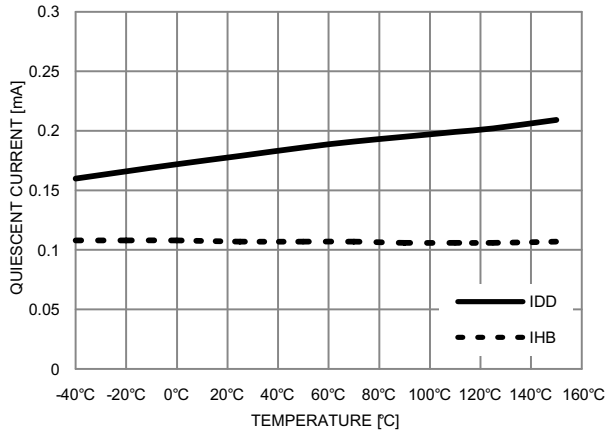


Figure 5. Quiescent Current vs. Temperature

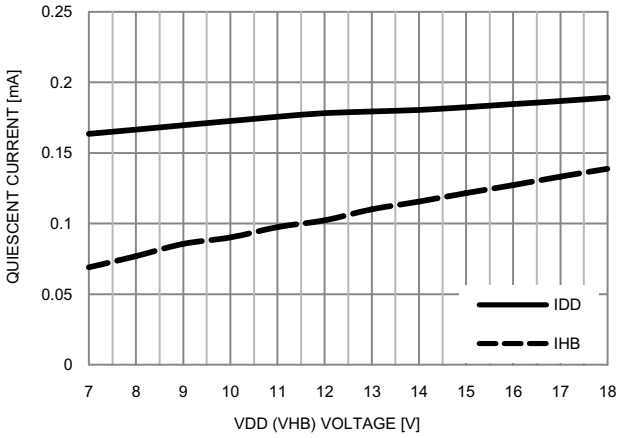


Figure 6. Quiescent Current vs. V_{DD} (V_{HB})

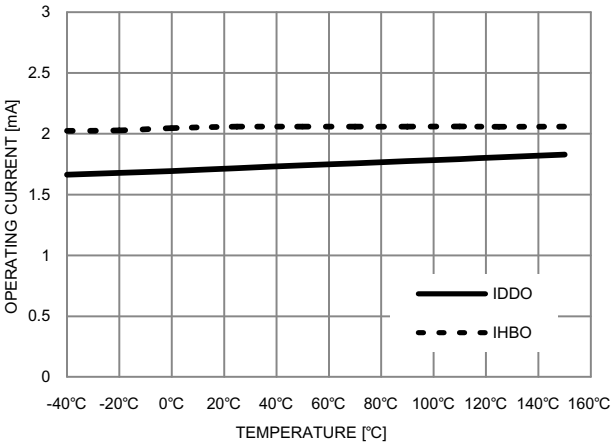


Figure 7. Operating Current vs. Temperature

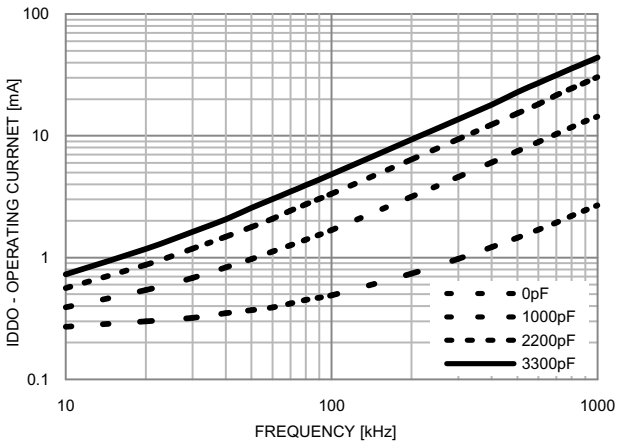


Figure 8. I_{DD} Operating Current vs. Frequency

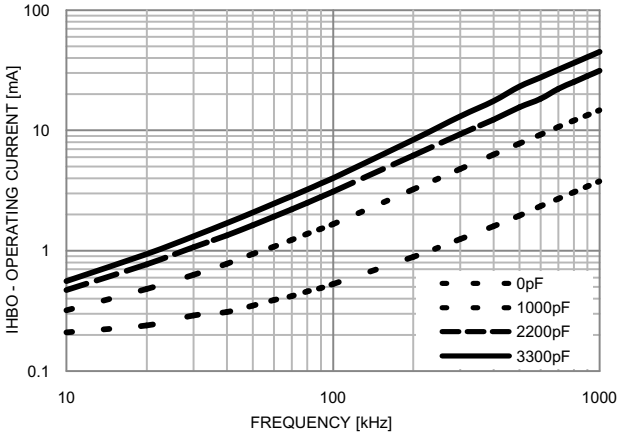


Figure 9. I_{HB} Operating Current vs. Frequency

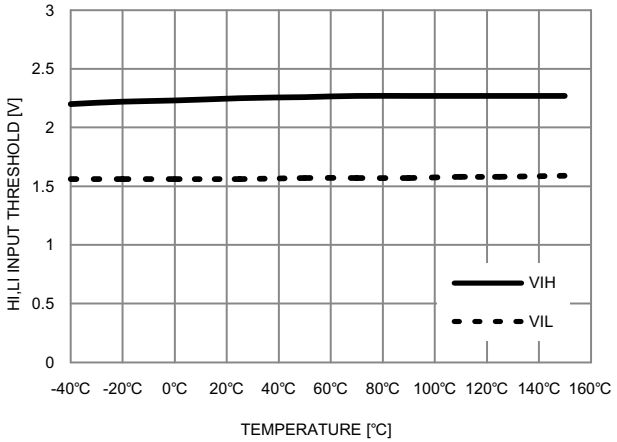


Figure 10. Input Threshold vs. Temperature

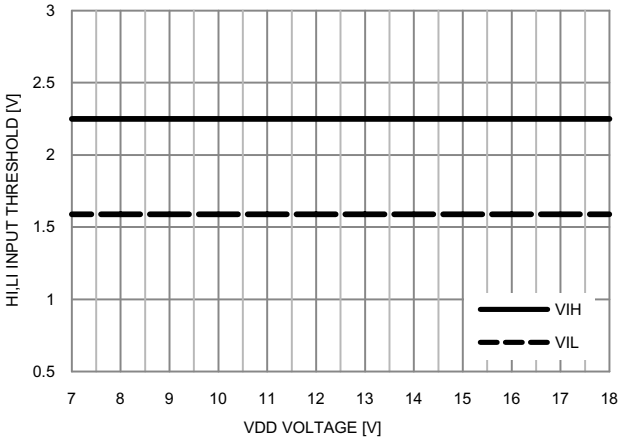


Figure 11. Input Threshold vs. V_{DD}

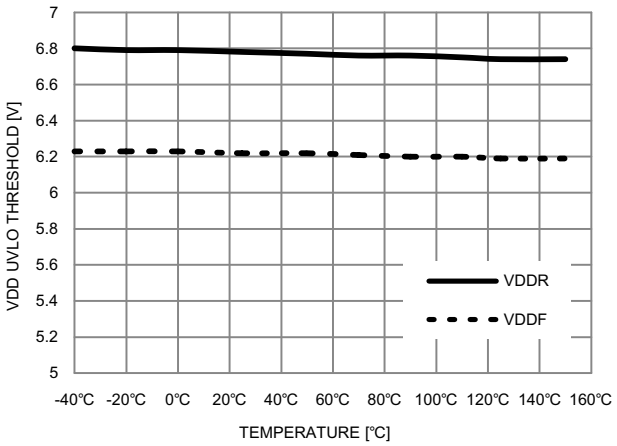


Figure 12. V_{DD} UVLO Threshold vs. Temperature

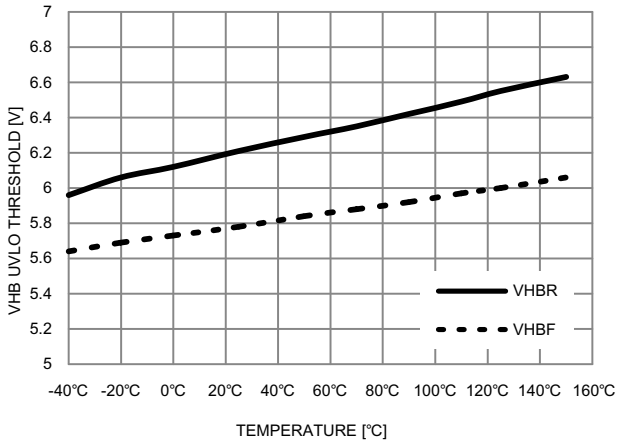


Figure 13. V_{HB} UVLO Threshold vs. Temperature

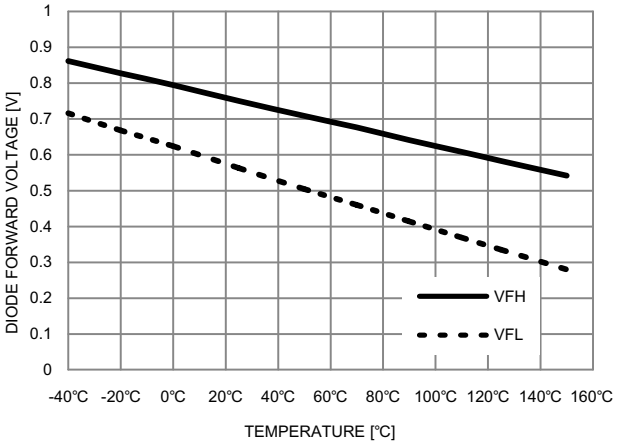


Figure 14. Bootstrap Diode V_F vs. Temperature

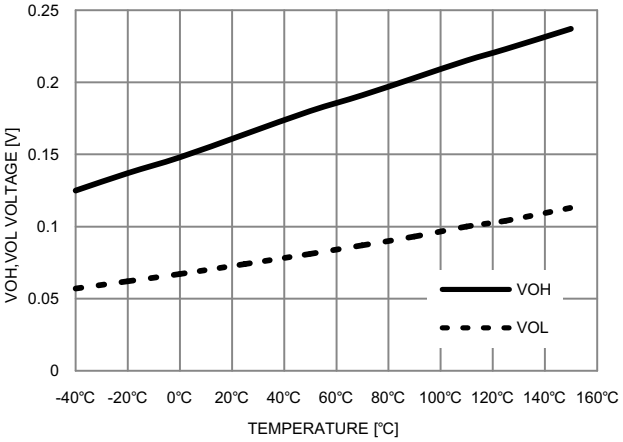


Figure 15. V_{OH}, V_{OL} Voltage vs. Temperature

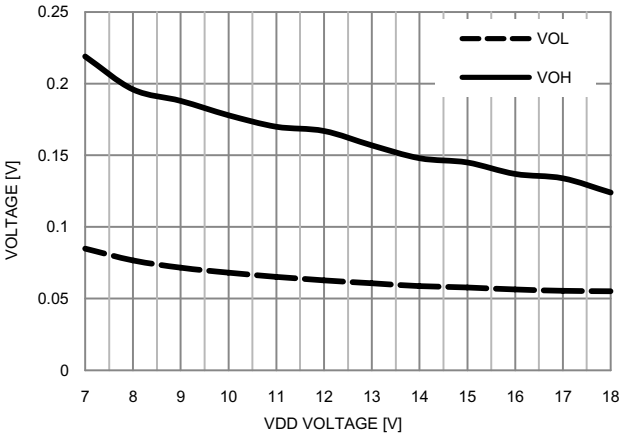


Figure 16. V_{OH}, V_{OL} Voltage vs. V_{DD} (V_{HB})

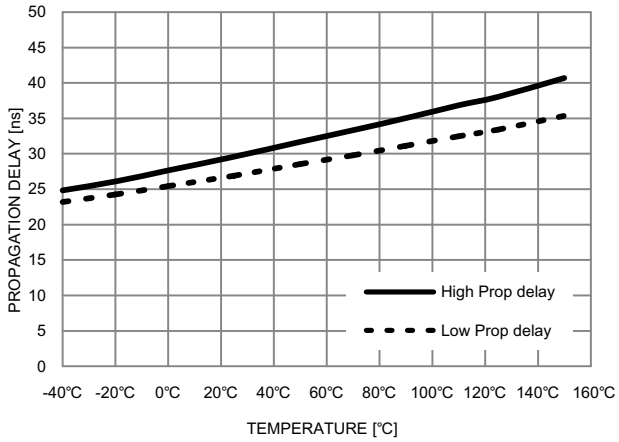


Figure 17. Low Side Propagation Delay vs. Temperature

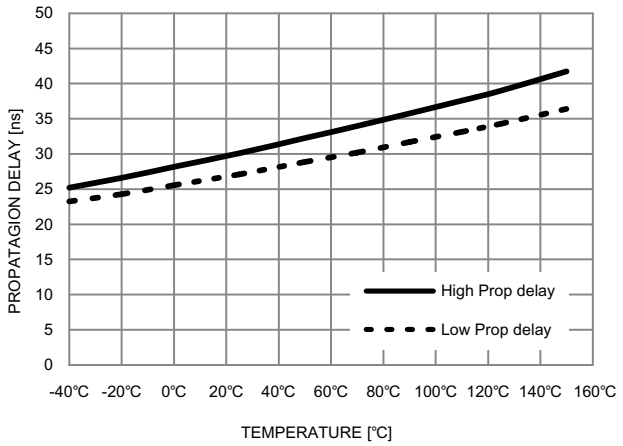


Figure 18. High Side Propagation Delay vs. Temperature

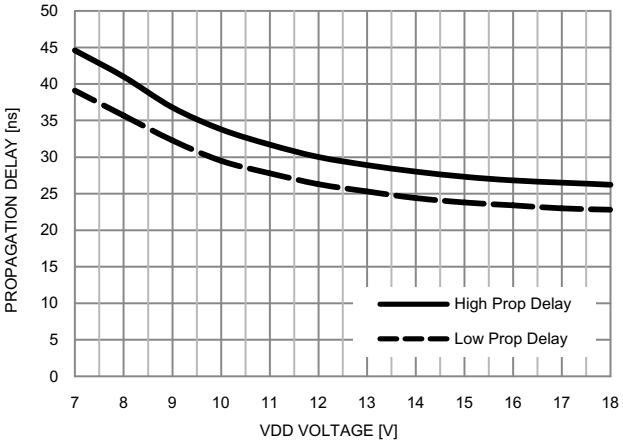


Figure 19. Low Side Propagation Delay vs. V_{DD}

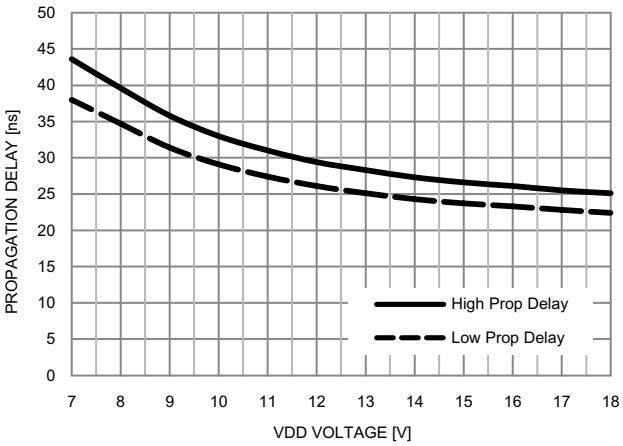


Figure 20. High Side Propagation Delay vs. V_{HB}

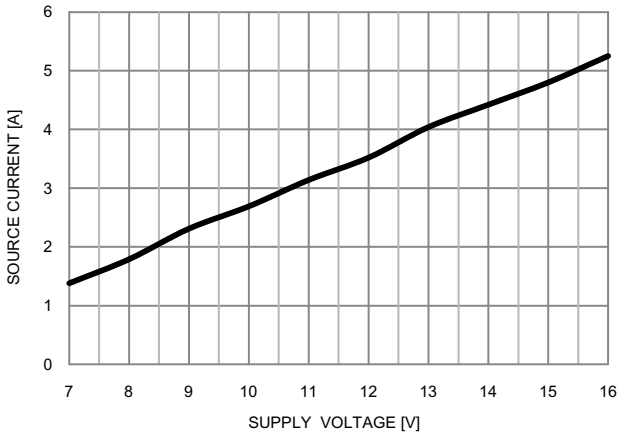


Figure 21. HO, LO Peak Source Current vs. Supply Voltage

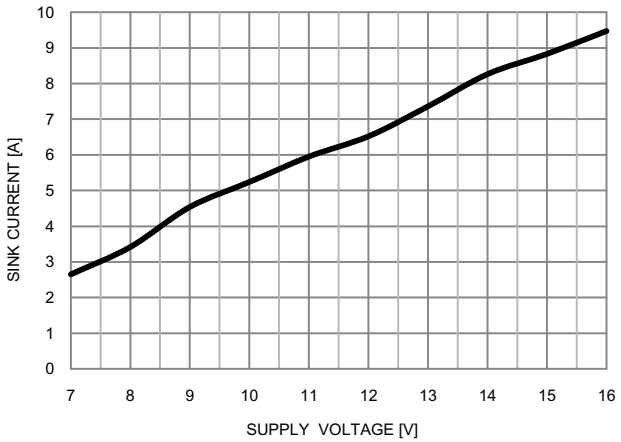


Figure 22. HO, LO Peak Sink Current vs. Supply Voltage

Switching Time Definitions

Figure 23 shows the switching time waveforms definitions of the turn on and off propagation delay times.

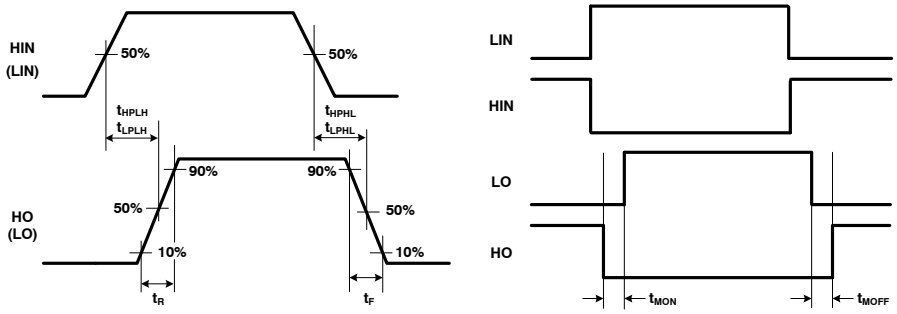


Figure 23. Timing Diagrams

Input to Output Definitions

Figure 24 shows an input to output timing diagram for overall operation.

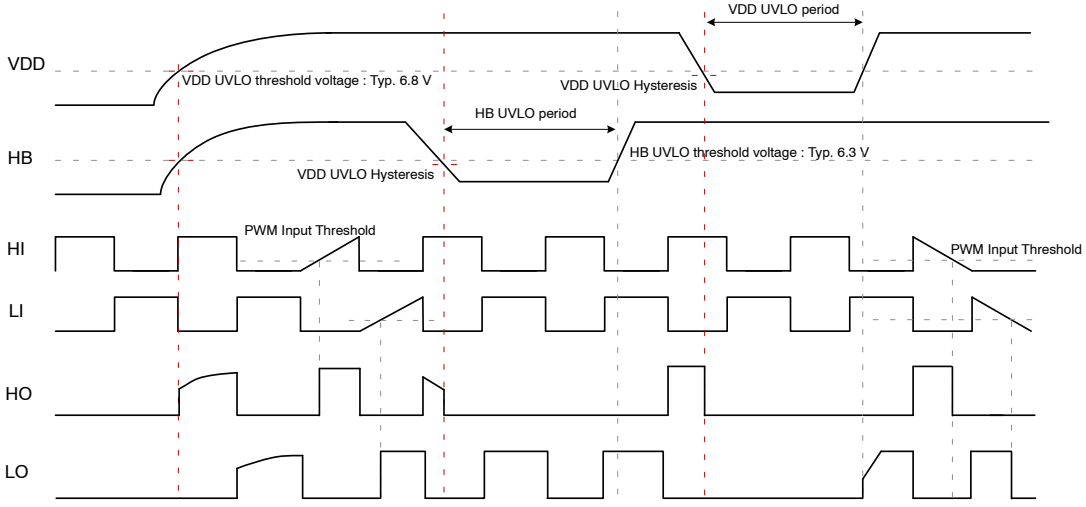


Figure 24. Overall Operation Timing Diagram

APPLICATIONS INFORMATION

The NCV51511 is designed to drive high side and the low side N−channel power MOSFETs in a half bridge or synchronous buck. The driver IC integrates a bootstrap diode for high side driver bias supply. High side and Low side outputs are independently controlled by each of input control signals with TTL or logic compatibility. The floating high side driver can operate with supply voltage up to 80 V. The NCV51511 functions consist of the input stage, level shift, bootstrap diode, Under−Voltage Lockout (UVLO) protection and output stage. The UVLO function is included in both the high−and low side.

Input Stage

The input pins (HI,LI) of gate driver devices are based on a TTL compatible input threshold logic that is independent of the V_{DD} supply voltage. The PWM input signal (high level) can be 3.3 V, 5 V or up to VDD logic input to accommodate all possible applications. The input impedance of the NCV51511 is 100 kΩ nominal. The 100 kΩ is a pull−down resistance to ground (GND). The logic level compatible input provides a 2.2 V rising threshold and a 1.7 V falling threshold.

Level Shift

The level shift circuit is the interface from the high side input to the high side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low side driver.

To control the high side output drive utilizes a widely used technique for high side level shifter circuit so called pulsed latch level translators.

Bootstrap Diode

The NCV51511 integrates a high voltage bootstrap diode to generate the high side bias. It is provided to charge high side gate drive bootstrap capacitor. The diode anode is connected to V_{DD} and cathode connected to HB. The boot capacitor should be connected externally to HB and the HS pins, the HB capacitor charge is refreshed every switching cycle when HS transitions to ground. The bootstrap diode provides fast recovery times, and a low resistance value of 0.7 Ω typ.

Under−Voltage Lockout (UVLO)

Both high side and low side drivers have independent UVLO protections which monitor the V_{DD} supply voltage and HB bootstrap voltage. The function of the UVLO circuits is to ensure that there are enough supply voltages (V_{DD} and HB) to correctly bias high side and low side circuits. This also ensures that the gate of external MOSFETs are driven at an optimum voltage. The V_{DD} UVLO disables both high side and low side drivers when V_{DD} is below the specified threshold. The rise V_{DD} threshold is 6.8 V with 0.6 V hysteresis. The HB UVLO disables only the high side driver when the HB to HS differential voltage is below the specified threshold. The HB UVLO rise threshold is 6.3 V with 0.4 V hysteresis.

Output Stage

The NCV51511 output stage is able to Sink/Source 3.0 A /6.0 A typical which can effectively charge and discharge a 1 nF load in few ns. High−speed switching, low resistance and high current capability of both high side and low side drivers allow for efficient switching operation. The low side driver is referenced from V_{DD} to V_{SS} and the high side is referenced from HB to HS. The device logic status shows as below.

Table 7. DEVICE LOGIC STATUS

	HI	LI	HO	LO
Status	L	L	L	L
	L	H	L	H
	H	L	H	L
	H	H	H	H
	X	X	L	L

Select Bootstrap Capacitor

The maximum allowable voltage drop across the bootstrap capacitor to ensure enough gate−source voltage is highly dependent to the internal under−voltage Lockout level of the gate drive IC, and the voltage level at the source connection of switching node HS. The maximum allowable drop voltage can be obtained by (eq.1)

$$\Delta V_{HB} = V_{DD} - V_f - V_{HB,UVLO} \quad \text{(eq. 1)}$$

Where:

- V_{DD}: Gate drive IC supply voltage
- V_f : Static forward voltage drop of bootstrap diode
- $V_{HB,UVLO}$: HB Under−Voltage Lockout level

The total charge (Q_{BS}) required by the bootstrap capacitor can be calculated by summing the Q_g of the MOSFET and the charge required for the level shifter in the gate drive IC which is negligible quantity to compared Q_g of the MOSFET.

$$Q_{BS} = Q_g + (I_{HBS} \times T_{ON}) \quad \text{(eq. 2)}$$

Where:

- Q_{BS}: Total gate charge of bootstrap capacitor
- Q_g: Gate charge of the MOSFET
- I_{HBS}: Quiescent current in High side gate drive IC.
- T_{ON}: Turning−on time of high−side MOSFET

The guiding criteria for calculating the minimum required bootstrap capacitance can be obtained through (eq.3).

$$C_{BOOT.MIN} \geq \frac{Q_{BS}}{\Delta V_{HB}} \quad \text{(eq. 3)}$$

Select External Bootstrap Series Resistor

The NCV51511 utilizes high−speed gate driving for synchronous buck and half bridge applications. In these applications, voltage ringing can be generated by parasitic inductance of the primary power path, consisting of the input capacitor and switching MOSFETs (C_{oss}).

To reduce this ringing phenomenon, the first step is to optimize the PCB layout to reduce parasitic components of the power path. The second step is to add a series resistor with the bootstrap capacitor to slow down the turn−on transition of the high side MOSFET.

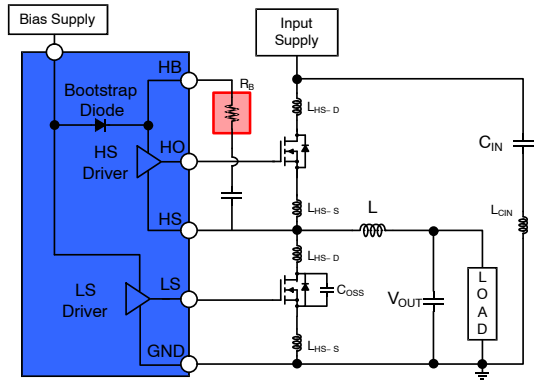


Figure 25. Application Circuit with Parasitic Components

Figure 25 shows the synchronous buck with the parasitic component at the power path. Each of parasitic inductance and low side C_{OSS} of MOSFET made up the ringing phenomenon at the HS node, when the high side turns on. When the bootstrap series resistor R_B installed with bootstrap capacitor, the bootstrap resistor limits the current available to charge the gate of the high side MOSFET, increasing the time needed to turn the high side MOSFET on. The increased switching time slows the HS node rate of rising and can have a significant impact on the peak voltage on the HS node.

We recommend selecting less than 10 Ω for R_B.

$$I_{BOOT(PEAK)} = \frac{V_{DD} - V_f}{R_B} \quad \text{(eq. 4)}$$

Select Gate Resistor

The gate resistor is also sized to reduce a ringing voltage of the HS node by parasitic inductances and capacitances. But, it limits the current capability of the gate driver output by the resistance value. The limited current capability value by the gate resistor can be obtained (eq.5).

$$I_{OHH} = \frac{V_{DD} - V_f - V_{OHH}}{R_{gate}}$$

$$I_{OLH} = \frac{V_{DD} - V_f - V_{OLH}}{R_{gate}}$$

$$I_{OHL} = \frac{V_{DD} - V_{OHL}}{R_{gate}}$$

$$I_{OLL} = \frac{V_{DD} - V_{OLL}}{R_{gate}} \quad \text{(eq. 5)}$$

Where:

- I_{OHH}: High side peak source current
- I_{OLH}: High side peak sink current
- I_{OHL}: Low side peak source current
- I_{OLL}: Low side peak sink current
- V_f : Bootstrap diode forward voltage drop
- V_{OHH}: High level output voltage drop (high side)
- V_{OLH}: Low level output voltage drop (high side)
- V_{OHL}: High level output voltage drop (low side)
- V_{OLL}: Low level output voltage drop (low side)

Gate Driver Power Dissipation

The total power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are:

- The static and dynamic losses related to the switching frequency
- Output load capacitance losses on high and low side drivers
- Internal consumption supply voltage, V_{DD}

The static losses are due to the quiescent current from the voltage supplies V_{DD} and ground in low side driver and the leakage current in the level shifting stage in high side driver, which are dependent on the voltage supplied on the HS pin and proportional to the duty cycle when only the high side power device is turned on. The quiescent current is consumed by the device through all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state. The effect of the static losses within the gate driver can be safely assumed to be negligible thanks to the NCV51511 low 0.17 mA quiescent current.

The dynamic losses are defined as follows: In the low side driver, the dynamic losses are due to two different sources. One is due to whenever a load capacitor is charged or discharged through a gate resistor, half of the energy that

goes into the capacitance is dissipated in the resistor. The losses in the gate driver resistance, internal and external to the gate driver, and the switching losses of the internal CMOS circuitry. The dynamic losses of the high side driver also have two different sources. One is due to the level shifting circuit and the other is to the charging and discharging of the capacitance of the high side. The static losses are neglected here because the total IC power dissipation is mainly dynamic losses of gate drive IC and can be estimated as:

$$P_{DGATE} = 2 \times C_L \times f_S \times V_{DD}^2 [W] \quad \text{(eq. 6)}$$

The bootstrap circuit power dissipation is the sum of the bootstrap diode losses and the bootstrap resistor losses if any exist. The bootstrap diode loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to switching frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor, resulting in more losses.

PCB Layout Guideline

NCV51511 is a high speed and high current high side and low side driver. To avoid any device malfunction during device operation, it is very important that there is very low parasitic inductance in the current switching path. It is very important that the best layout practices are followed for the PCB layout of the NCV51511. The following should be considered before beginning a PCB layout using the NCV51511.

- The gate driver should be located as close as possible of switching MOSFET.
- The V_{DD} capacitor and bootstrap capacitor should be located as near as possible to the device.
- In order to reduce a ringing voltage of the HS node, the space between high side source and low side drain of the MOSFET should be small as possible.
- The exposed pad should be connected to GND plane and use at least four or more vias for improved thermal performance.
- Avoid driver input pulse signal close to the HS node.

One of recommendation layout pattern for the driver is shown in Figure 26.

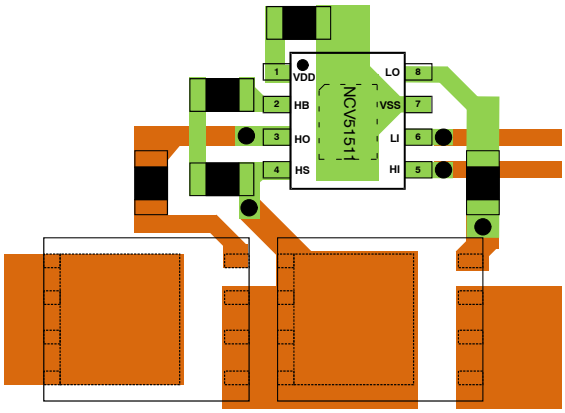


Figure 26. Layout Recommendation

ORDERING INFORMATION

Device	Output Configuration	Temperature Range (°C)	Package	Shipping†
NCV51511PDR2G	High Side and Low Side	−40 to 150	SOIC8−EP (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

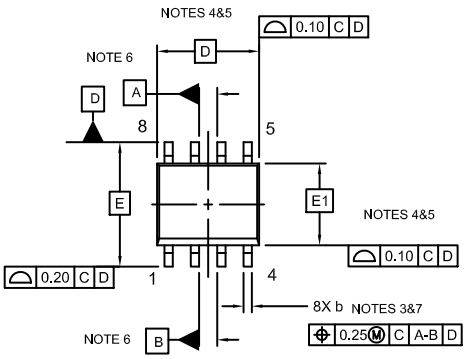
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE D

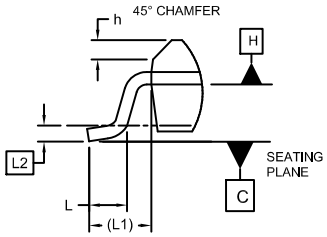
DATE 02 APR 2019

NOTES:

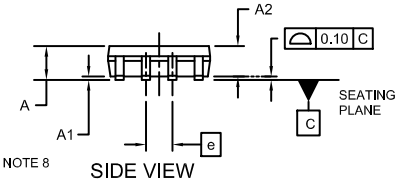
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



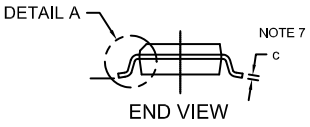
TOP VIEW



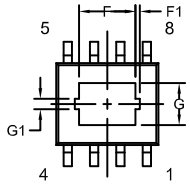
DETAIL A



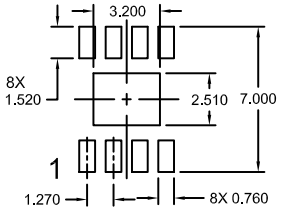
SIDE VIEW



END VIEW



BOTTOM VIEW

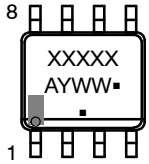


RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	−−−	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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