1/3-Inch Wide-VGA CMOS Digital Image Sensor

MT9V032C12STM (Monochrome, Pb-Free)
MT9V032C12STC (Color, Pb-Free)

Features

- Micron® DigitalClarity® CMOS imaging technology
- Array format: Wide-VGA, active 752H x 480V (360,960 pixels)
- Global shutter photodiode pixels; simultaneous integration and readout
- Monochrome or color: Near_IR enhanced performance for use with non-visible NIR illumination
- Readout modes: Progressive or interlaced
- Shutter efficiency: >99%
- Simple two-wire serial interface
- Register lock capability
- Window size: User programmable to any smaller format (QVGA, CIF, QCIF, and so on). Data rate can be maintained independent of window size
- Binning: 2 x 2 and 4 x 4 of the full resolution
- ADC: On-chip, 10-bit column-parallel (option to operate in 12-bit to 10-bit companding mode)
- Automatic controls: Auto exposure control (AEC) and auto gain control (AGC); variable regional and variable weight AEC/AGC
- Support for four unique serial control register IDs to control multiple imagers on the same bus
- Data output formats:
  - Single sensor mode:
    10-bit parallel/stand-alone
    8-bit or 10-bit serial LVDS
  - Stereo sensor mode:
    Interspersed 8-bit serial LVDS

Applications

- Security
- High dynamic range imaging
- Unattended surveillance
- Stereo vision
- Video as input
- Machine vision
- Automation
- Traffic camera

Table 1: Key Performance Parameters

Parameter	Value
Optical format	1/3-inch
Active imager size	4.51mm(H) x 2.88mm(V) 5.35mm diagonal
Active pixels	752H x 480V
Pixel size	6.0µm x 6.0µm
Color filter array	Monochrome or color RGB Bayer pattern
Shutter type	Global shutter—TrueSNAP™
Maximum data rate/ master clock	26.6 MPS/26.6 MHz
Full resolution	752 x 480
Frame rate	60 fps (at full resolution)
ADC resolution	10-bit column-parallel
Responsivity	4.8 V/lux-sec (550nm)
Dynamic range	>55dB linear; >80—100dB in HiDy mode
Supply voltage	3.3V ±0.3V (all supplies)
Power consumption	<320mW at maximum data rate; 100µW standby current
Operating temperature	–30°C to +70°C
Packaging	48-pin CLCC
Output gain	15.3 e-/LSB
Read noise	25 e-PRMS at 1X
Dark current	9,042 e-/pix/s at 55°C

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9V032C12STM ES	48-pin CLCC (mono)
MT9V032C12STC ES	48-pin CLCC (color)
MT9V032C12STMD ES	Demo kit (mono)
MT9V032C12STMH ES	Demo kit headboard only (mono)
MT9V032C12STCD ES	Demo kit (color)
MT9V032C12STCH ES	Demo kit headboard only (color)

General Description

The Micron Imaging MT9V032 is a 1/3-inch wide-VGA format CMOS active-pixel digital image sensor with global shutter and high dynamic range (HDR) operation. The sensor has specifically been designed to support the demanding interior and exterior unattended surveillance imaging needs, which makes this part ideal for a wide variety of imaging applications in real-world environments.

This wide-VGA CMOS image sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The active imaging pixel array is 752H x 480V. It incorporates sophisticated camera functions on-chip—such as binning 2 x 2 and 4 x 4, to improve sensitivity when operating in smaller resolutions—as well as windowing, column and row mirroring. It is programmable through a simple two-wire serial interface.

The MT9V032 can be operated in its default mode or be programmed for frame size, exposure, gain setting, and other parameters. The default mode outputs a wide-VGA-size image at 60 frames per second (fps).

An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. A 12-bit resolution companded for 10-bits for small signals can be alternatively enabled, allowing more accurate digitization for darker areas in the image.

In addition to a traditional, parallel logic output the MT9V032 also features a serial low-voltage differential signaling (LVDS) output. The sensor can be operated in a stereo-camera mode, and the sensor, designated as a stereo-master, is able to merge the data from itself and the stereo-slave sensor into one serial LVDS stream.

Figure 1: Block Diagram

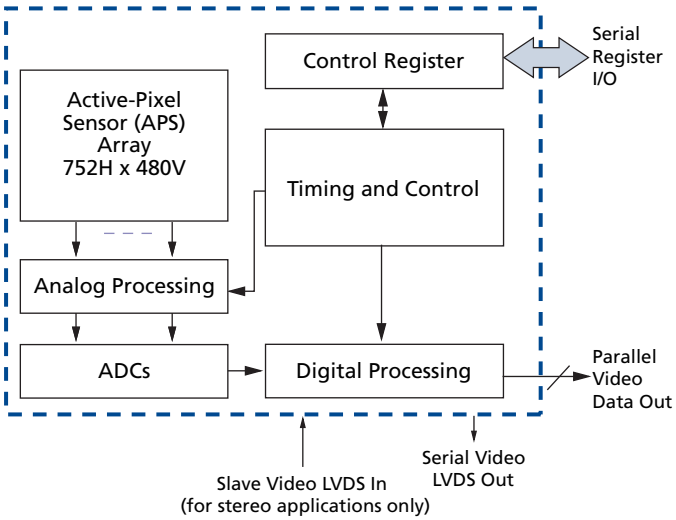
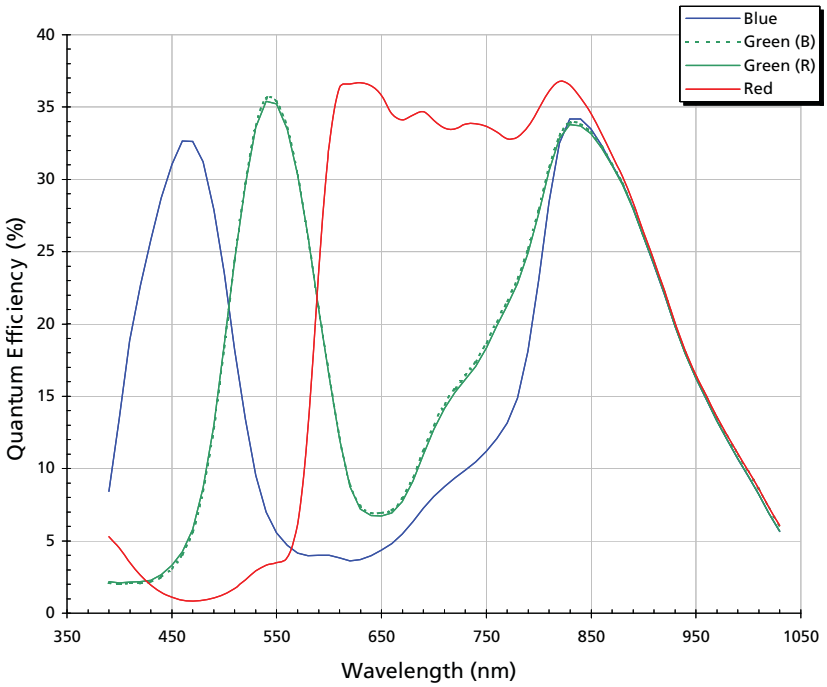


Figure 2: MT9V032 Quantum Efficiency vs. Wavelength



Pin Descriptions

Figure 3 shows the package pinout for the MT9V032. Table 3 on page 5 provides the pin descriptions.

Figure 3: 48-Pin CLCC Package Pinout Diagram

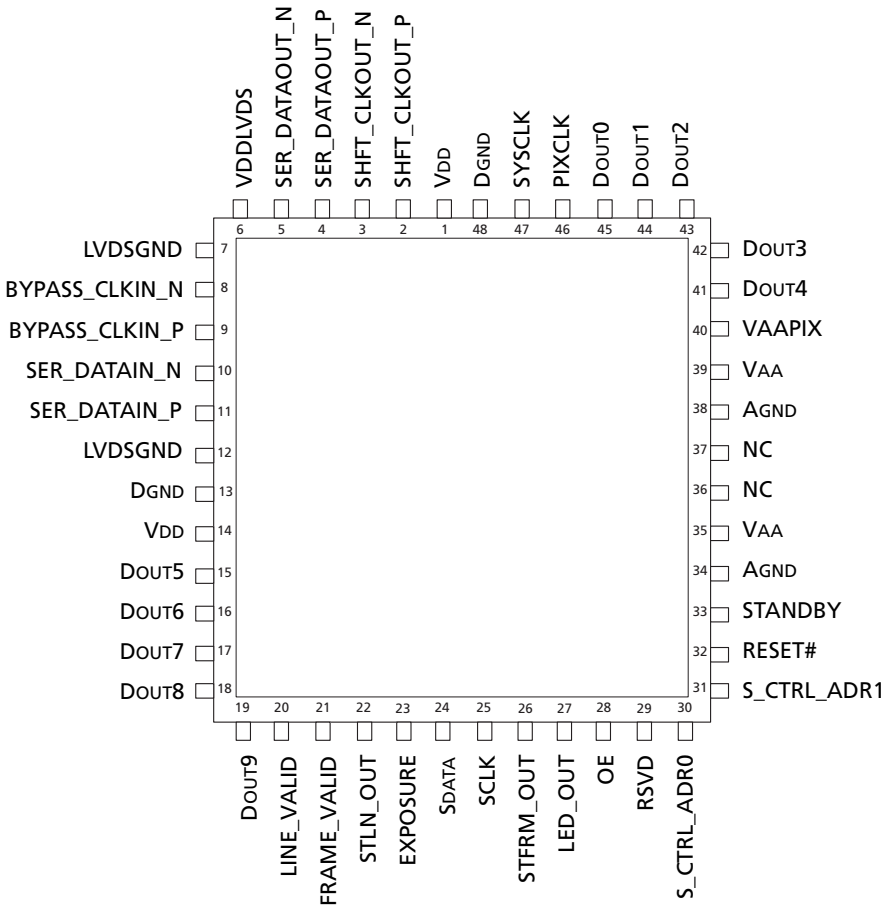


Table 3: Pin Descriptions

Only pins DOUT0 through DOUT9 may be tri-stated

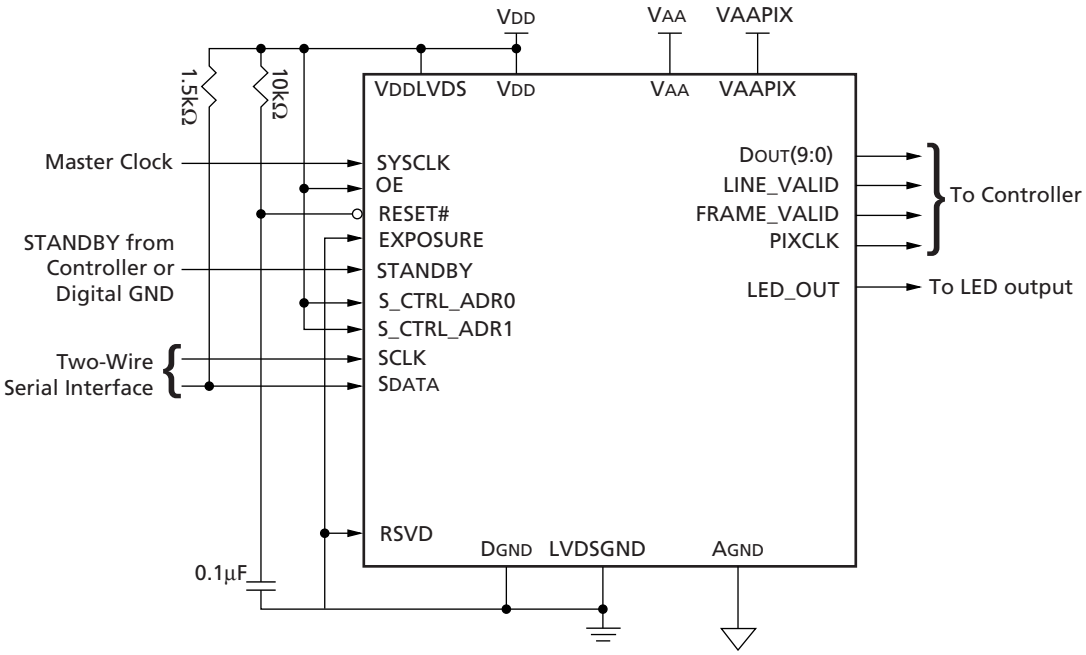
Pin Number	Symbol	Type	Description	Notes
29	RSVD	Input	Connect to DGND.	1
10	SER_DATAIN_N	Input	Serial data in for stereoscopy (differential negative). Tie to 1kΩ pull-up (to 3.3V) in non-stereoscopy mode.	
11	SER_DATAIN_P	Input	Serial data in for stereoscopy (differential positive). Tie to DGND in non-stereoscopy mode.	
8	BYPASS_CLKIN_N	Input	Input bypass shift-CLK (differential negative). Tie to 1KΩ pull-up (to 3.3V) in non-stereoscopy mode.	
9	BYPASS_CLKIN_P	Input	Input bypass shift-CLK (differential positive). Tie to DGND in non-stereoscopy mode.	
23	EXPOSURE	Input	Rising edge starts exposure in slave mode.	
25	SCLK	Input	Two-wire serial interface clock. Connect to VDD with 1.5K resistor even when no other two-wire serial interface peripheral is attached.	
28	OE	Input	DOUT enable pad, active HIGH.	2
30	S_CTRL_ADR0	Input	Two-wire serial interface slave address bit 3.	
31	S_CTRL_ADR1	Input	Two-wire serial interface slave address bit 5.	
32	RESET#	Input	Asynchronous reset. All registers assume defaults.	
33	STANDBY	Input	Shut down sensor operation for power saving.	
47	SYSCLK	Input	Master clock (26.6 MHz).	
24	SDATA	I/O	Two-wire serial interface data. Connect to VDD with 1.5K resistor even when no other two-wire serial interface peripheral is attached.	
22	STLN_OUT	I/O	Output in master mode—start line sync to drive slave chip in-phase; input in slave mode.	
26	STFRM_OUT	I/O	Output in master mode—start frame sync to drive a slave chip in-phase; input in slave mode.	
20	LINE_VALID	Output	Asserted when DOUT data is valid.	
21	FRAME_VALID	Output	Asserted when DOUT data is valid.	
15	DOUT5	Output	Parallel pixel data output 5.	
16	DOUT6	Output	Parallel pixel data output 6.	
17	DOUT7	Output	Parallel pixel data output 7.	
18	DOUT8	Output	Parallel pixel data output 8	
19	DOUT9	Output	Parallel pixel data output 9.	
27	LED_OUT	Output	LED strobe output.	
41	DOUT4	Output	Parallel pixel data output 4.	
42	DOUT3	Output	Parallel pixel data output 3.	
43	DOUT2	Output	Parallel pixel data output 2.	
44	DOUT1	Output	Parallel pixel data output 1.	
45	DOUT0	Output	Parallel pixel data output 0.	
46	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.	
2	SHFT_CLKOUT_N	Output	Output shift CLK (differential negative).	
3	SHFT_CLKOUT_P	Output	Output shift CLK (differential positive).	
4	SER_DATAOUT_N	Output	Serial data out (differential negative).	
5	SER_DATAOUT_P	Output	Serial data out (differential positive).	

Table 3: Pin Descriptions (continued)
Only pins DOUT0 through DOUT9 may be tri-stated

Pin Number	Symbol	Type	Description	Notes
1, 14	VDD	Supply	Digital power 3.3V.	
35, 39	VAA	Supply	Analog power 3.3V.	
40	VAAPIX	Supply	Pixel power 3.3V.	
6	VDDLVDS	Supply	Dedicated power for LVDS pads.	
7, 12	LVDSGND	Ground	Dedicated GND for LVDS pads.	
13, 48	DGND	Ground	Digital GND.	
34, 38	AGND	Ground	Analog GND.	
36, 37	NC	NC	No connect.	3

Notes:
1. Pin 29 (RSVD) must be tied to GND.
2. Output Enable (OE) tri-states signals DOUT0–DOUT9. No other signals are tri-stated with OE.
3. No connect. These pins must be left floating for proper operation.

Figure 4: Typical Configuration (Connection)—Parallel Output Mode



Note: LVDS signals are to be left floating.

Electrical Specifications

Table 4: DC Electrical Characteristics
V_{PWR} = 3.3V ±0.3V; T_A = Ambient = 25°C

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage		V_{PWR} -0.5	–	V_{PWR} +0.3	V
V_{IL}	Input low voltage		-0.3	–	0.8	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{PWR} or V_{GND}	-15.0	–	15.0	µA
V_{OH}	Output high voltage	I_{OH} = -4.0mA	V_{PWR} -0.7	–	–	V
V_{OL}	Output low voltage	I_{OL} = 4.0mA	–	–	0.3	V
I_{OH}	Output high current	V_{OH} = V_{DD} - 0.7	-9.0	–	–	mA
I_{OL}	Output low current	V_{OL} = 0.7	–	–	9.0	mA
V_{AA}	Analog power supply	Default settings	3.0	3.3	3.6	V
I_{PWRA}	Analog supply current	Default settings	–	35.0	60.0	mA
V_{DD}	Digital power supply	Default settings	3.0	3.3	3.6	V
I_{PWRD}	Digital supply current	Default settings, C_{LOAD}= 10pF	–	35.0	60	mA
VAAPIX	Pixel array power supply	Default settings	3.0	3.3	3.6	V
I_{PIX}	Pixel supply current	Default settings	0.5	1.4	3.0	mA
V_{LVDS}	LVDS power supply	Default settings	3.0	3.3	3.6	V
I_{LVDS}	LVDS supply current	Default settings	11.0	13.0	15.0	mA
I_{PWRA} Standby	Analog standby supply current	STDBY = V_{DD}	2	3	4	µA
I_{PWRD} Standby Clock Off	Digital standby supply current with clock off	STDBY = V_{DD}, CLKIN = 0 MHz	1	2	4	µA
I_{PWRD} Standby Clock On	Digital standby supply current with clock on	STDBY= V_{DD}, CLKIN = 27 MHz	–	1.05	–	mA

Table 5: LVDS Driver DC Specifications
V_{PWR} = 3.3V ±0.3V; T_A = Ambient = 25°C

Symbol	Definition	Condition	Min	Typ	Max	Unit
|V_{OD}|	Output differential voltage	R_{LOAD} = 100 Ω ±1%	250	–	400	mV
|DV_{OD}|	Change in V_{OD} between complementary output states		–	–	50	mV
V_{OS}	Output offset voltage		1.0	1.2	1.4	mV
DV_{OS}	Change in V_{OS} between complementary output states		–	–	35	mV
I_{OS}	Output current when driver shorted to ground			±10	±12	mA
I_{OZ}	Output current when driver is tri-state			±1	±10	µA

Table 6: LVDS Receiver DC Specifications

V_{PWR} = 3.3V ±0.3V; T_A = Ambient = 25°C

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{IDTH+}	Input differential	| V_{GPD}| <925mV	-100	–	100	mV
Iin	Input current		–	–	±20	µA

Caution Stresses greater than those listed in Table 7 may cause permanent damage to the device.

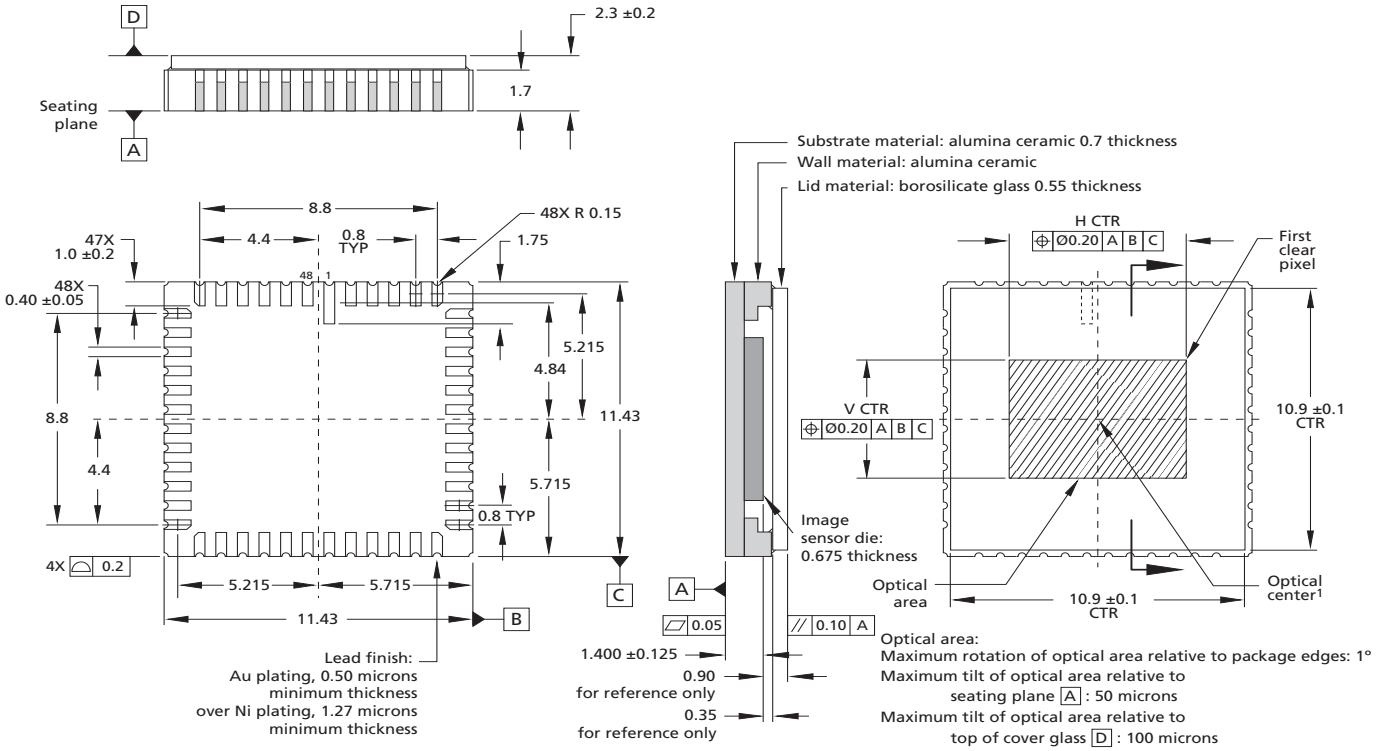
Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{SUPPLY}	Power supply voltage (all supplies)	-0.3	4.5	V
I_{SUPPLY}	Total power supply current	–	200	mA
I_{GND}	Total ground current	–	200	mA
V_{IN}	DC input voltage	-0.3	$V_{DD}Q$ + 0.3	V
V_{OUT}	DC output voltage	-0.3	$V_{DD}Q$ + 0.3	V
T_{STG}	Storage temperature	-40	+125	°C

Note: These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Package Dimensions

Figure 5: 48-Pin CLCC Package Outline Drawing



Notes:
1. Optical center = package center.
2. All dimensions are in millimeters.

Appendix A – Serial Configurations

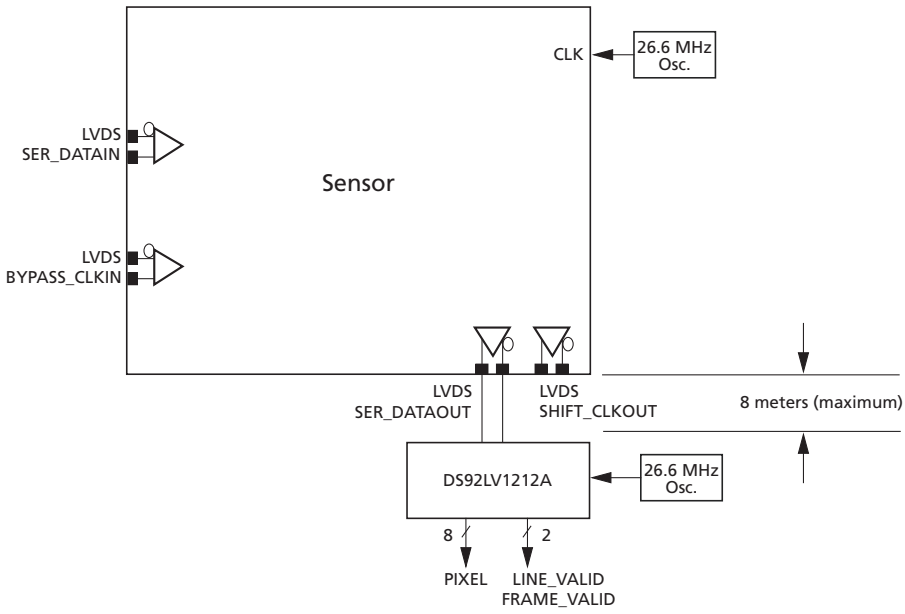
With the LVDS serial video output, the deserializer can be up to 8 meters from the sensor. The serial link can save on the cabling cost of 14 wires (DOUT[9:0], LINE_VALID, FRAME_VALID, PIXCLK, GND). Instead, just three wires (two serial LVDS, one GND) are sufficient to carry the video signal.

Configuration of Sensor for Stand-Alone Serial Output with Internal PLL

In this configuration, the internal PLL generates the shift-clk (x12). The LVDS pins SER_DATAOUT_P and SER_DATAOUT_N must be connected to a deserializer (clocked at approximately the same system clock frequency).

Figure 6 shows how a standard off-the-shelf deserializer (National Semiconductor DS92LV1212A) can be used to retrieve the standard parallel video signals of DOUT[9:0], LINE_VALID and FRAME_VALID.

Figure 6: Stand-Alone Topology



8-bit configuration shown

Typical configuration of the sensor:

1. Power up sensor.
2. Enable LVDS driver (set R0xB3[4]= 0).
3. De-assert LVDS power-down (set R0xB1[1] = 0.
4. Issue a soft reset (set R0x0C[0] = 1 followed by R0x0C[0] = 0.

If necessary:

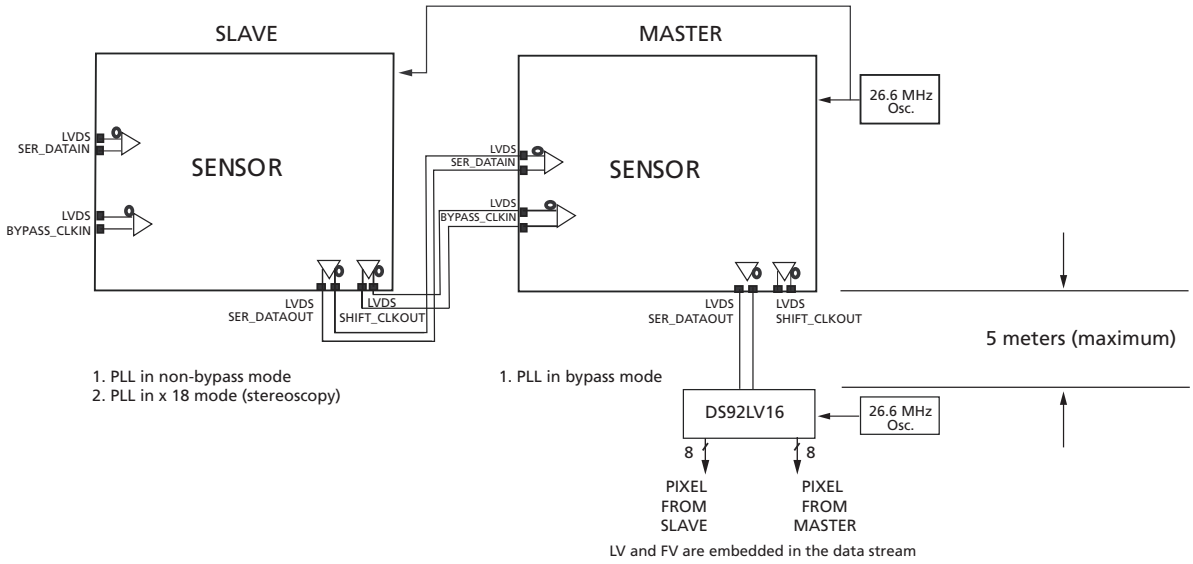
5. Force sync patterns for the deserializer to lock (set R0xB5[0] = 1).
6. Stop applying sync patterns (set R0xB5[0] = 0).

Configuration of Sensor for Stereoscopic Serial Output with Internal PLL

In this configuration the internal PLL generates the shift-clk (x18) in phase with the system-clock. The LVDS pins SER_DATAOUT_P and SER_DATAOUT_N must be connected to a deserializer (clocked at approximately the same system clock frequency).

Figure 7 shows how a standard off-the-shelf deserializer can be used to retrieve back DOUT(9:2) for both the master and slave sensors. Additional logic is required to extract out LINE_VALID and FRAME_VALID embedded within the pixel data stream.

Figure 7: Stereoscopic Topology



Typical configuration of the master and slave sensors:

1. Power up the sensors.
2. Broadcast WRITE to de-assert LVDS power-down (set R0xB1[1] = 0).
3. Individual WRITE to master sensor putting its internal PLL into bypass mode (set R0xB1[0] = 1).
4. Broadcast WRITE to both sensors to set the stereoscopy bit (set R0x07[5] = 1).
5. Make sure all resolution, vertical blanking, horizontal blanking, window size, and AEC/AGC configurations are done through broadcast WRITE to maintain lockstep.
6. Broadcast WRITE to enable LVDS driver (set R0xB3[4] = 0).
7. Broadcast WRITE to enable LVDS receiver (set R0xB2[4] = 0).
8. Individual WRITE to master sensor, putting its internal PLL into bypass mode (set R0xB1[0] = 1).
9. Individual WRITE to slave sensor, enabling its internal PLL (set R0xB1[0] = 0).
10. Individual WRITE to slave sensor, setting it as a stereo slave (set R0x07[6] = 1).
11. Individual WRITEs to master sensor to minimize the inter-sensor skew (set R0xB2[2:0], R0xB3[2:0], and R0xB4[1:0] appropriately). Use R0xB7 and R0xB8 to get lockstep feedback from stereo_error_flag.
12. Broadcast WRITE to issue a soft reset (set R0x0C[0] = 1 followed by R0x0C[0] = 0).

Note: The stereo_error_flag is set if a mismatch has occurred at a reserved byte (slave and master sensor's codes at this reserved byte must match). If the flag is set, steps 11 and 12 are repeated until the stereo_error_flag remains cleared.

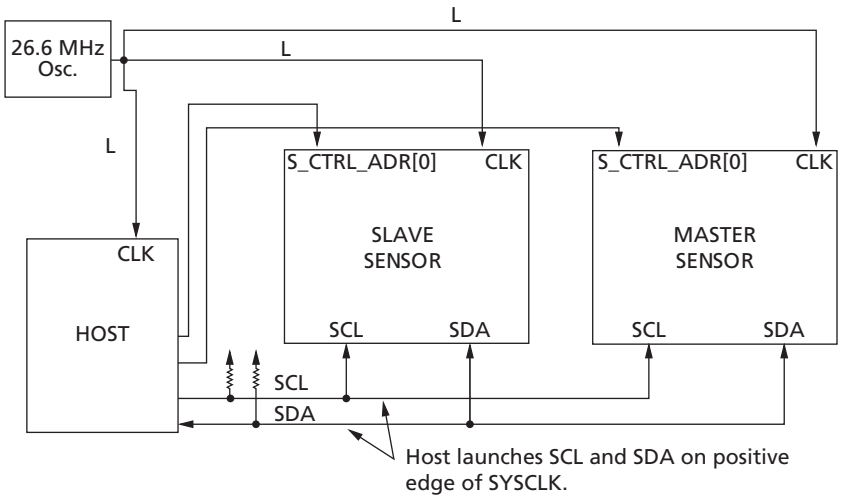
Broadcast and Individual Writes for Stereoscopic Topology

In stereoscopic mode, the two sensors are required to run in lockstep. This implies that control logic in each sensor is in exactly the same state as its pair on every clock. To ensure this, all inputs that affect control logic must be identical and arrive at the same time at each sensor.

These inputs include:

- system clock
- system reset
- two-wire serial interface clk - SCL
- two-wire serial interface data - SDA

Figure 8: Two-Wire Serial Interface Configuration in Stereoscopic Mode



All system clock lengths (L) must be equal.
SCL and SDA lengths to each sensor (from the host) must also be equal.

The setup in Figure 8 shows how the two sensors can maintain lockstep when their configuration registers are written through the two-wire serial interface. A WRITE to configuration registers would either be broadcast (simultaneous WRITES to both sensors) or individual (WRITE to just one sensor at a time). READs from configuration registers would be individual (READs from just one sensor at a time).

One of the two serial interface slave address bits of the sensor is hardwired. The other is controlled by the host. This allows the host to perform either a broadcast or a one-to-one access.

Broadcast WRITES are performed by setting the same S_CTRL_ADR input bit for both slave and master sensor. Individual WRITES are performed by setting opposite S_CTRL_ADR input bit for both slave and master sensor. Similarly, individual READs are performed by setting opposite S_CTRL_ADR input bit for both slave and master sensor.

Revision History

Rev. B 3/28/2007

- Updated package drawing