October 2018

FTCO3V85A1

3-Phase Automotive Power Module for DC-DC Converter

General Description

The FTCO3V85A1 is an 80V low Rds(on) automotive qualified power module, featuring a 3-phase MOSFET bridge optimized for Automotive 48V-12V interleaved DC -DC converter system, It includes a precision shunt resistor for current sensing, an NTC for temperature sensing, and an RC snubber circuit.

The module utilizes ON's trench MOSFET technology and it is designed to provide a very compact and high efficiency solution for DC-DC converter system. The Power module is 100% lead free, RoHs and UL compliant.

Benefits

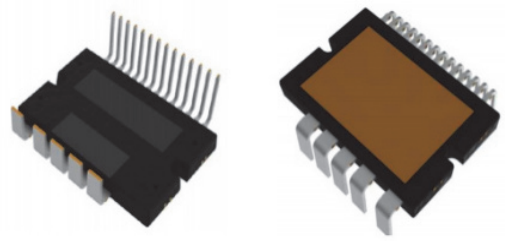
- Low junction-sink thermal resistance
- Low power loss for high efficiency in DC-DC system design
- Low electrical resistance
- Compact DC-DC converter design
- Highly integrated compact design
- Better EMI and electrical isolation
- Easy and reliable installation
- High current handling
- Improved overall system reliability

Features

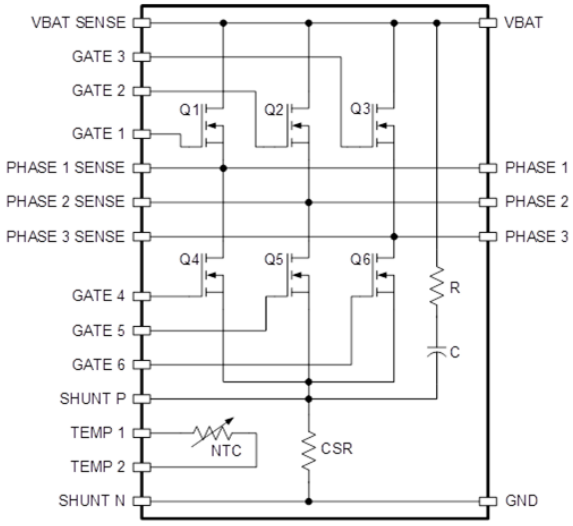
- 3-Phase 1.5kW 48V-12V interleaved DC-DC converter
- 80V-125A trench MOSFETs for high-side
  80V-160A trench MOSFETs for low-side
- Precise shunt current sensing
- Temperature sensing
- DBC substrate
- 100% lead free and RoHS compliant 2000/53/C directive.
- UL94V-0 compliant
- Isolation rating of 2500Vrms/min
- Mounting through screws
- Automotive qualified

Applications

- DC-DC converter



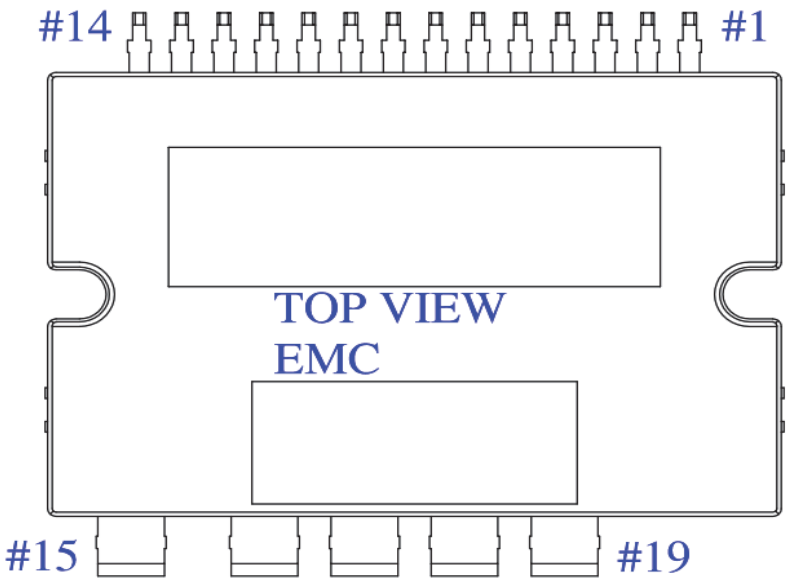
Package



Schematic

@2017 Semiconductor Components Industries, LLC

Pin Configuration

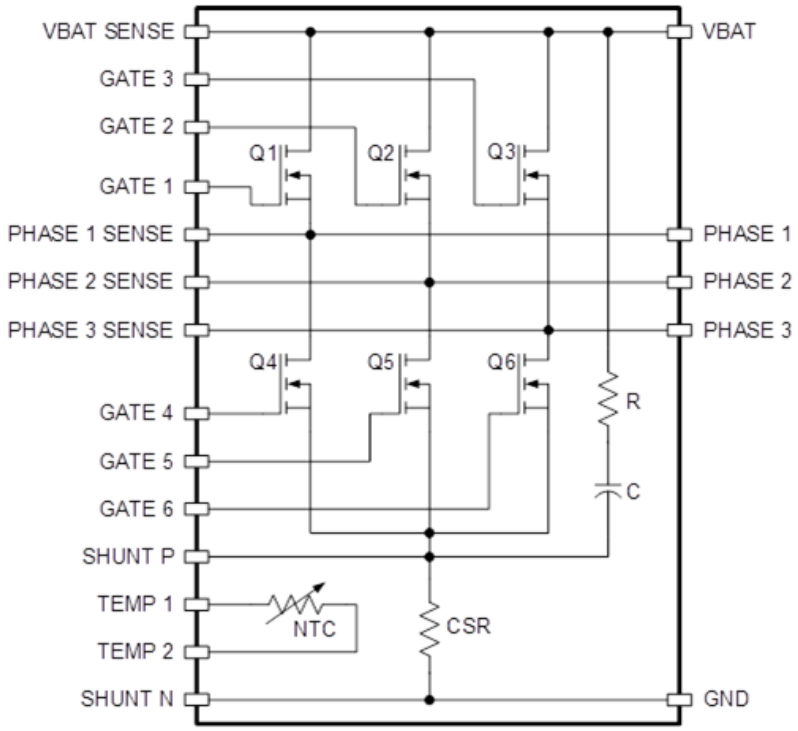


Pin Description

Pin Number	Pin Number	Pin Descriptions
1	TEMP 1	NTC Thermistor Terminal 1
2	TEMP 2	NTC Thermistor Terminal 2
3	PHASE 3 SENSE	Source of Q3 and Drain of Q6
4	GATE 3	Gate of Q3, high side Phase 3 MOSFET
5	GATE 6	Gate of Q6, low side Phase 3 MOSFET
6	PHASE 2 SENSE	Source of Q2 and Drain of Q5
7	GATE 2	Gate of Q2, high side Phase 2 MOSFET
8	GATE 5	Gate of Q5, low side Phase 2 MOSFET
9	PHASE 1 SENSE	Source of Q1 and Drain of Q4
10	GATE 1	Gate of Q1, high side Phase 1 MOSFET
11	VBAT SENSE	Sense pin for battery voltage and Drain of high side MOSFETs
12	GATE 4	Gate of Q4, low side Phase 1 MOSFET
13	SHUNT P	Positive CSR sense pin and source connection for low side MOSFETs
14	SHUNT N	Negative CSR sense pin and sense pin for battery return
15	VBAT	Battery voltage power lead
16	GND	Battery return power lead
17	PHASE 1	Phase 1 power lead
18	PHASE 2	Phase 2 power lead
19	PHASE 3	Phase 3 power lead

@2017 Semiconductor Components Industries, LLC

Internal Equivalent Circuit



Flammability Information

All materials present in the power module meet UL flammability rating class 94V-0 or higher.

Solder

Solder used is a lead free SnAgCu alloy.

Compliance to RoHS

The Power Module is 100% lead free and RoHS compliant with the 2000/53/C directive.

@2017 Semiconductor Components Industries, LLC

Absolute Maximum Ratings (T_J = 25°C, Unless Otherwise Specified)

Symbol	Parameter	Rating	Unit
V_{DS}(Q1~Q6)	Drain to Source Voltage	80	V
V_{GS}(Q1~Q6)	Gate to Source Voltage	±20	V
I_D (high-side)	Drain Current Continuous (TC = 25°C, TJ = 175°C, VGS = 10V) (*Note 1)	125	A
I_D (low-side)	Drain Current Continuous (TC = 25°C, TJ = 175°C, VGS = 10V) (*Note 1)	160	A
E_{AS}(Q1~Q3)	Single Pulse Avalanche Energy (*Note 2)	190	mJ
E_{AS}(Q4~Q6)	Single Pulse Avalanche Energy (*Note 2)	324	mJ
P_D(high-side)	Power dissipation (TC = 25°C, TJ = 175°C)	115	W
P_D(low-side)	Power dissipation (TC = 25°C, TJ = 175°C)	135	W
T_J	Maximum Junction Temperature	175	°C
T_{STG}	Storage Temperature	125	°C

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
Rthjc Thermal Resistance Junction to case, Single FET, (*Note 3)	Q1 Thermal Resistance J -C	-	1.0	1.3	°C/W
	Q2 Thermal Resistance J -C	-	1.0	1.3	°C/W
	Q3 Thermal Resistance J -C	-	1.0	1.3	°C/W
	Q4 Thermal Resistance J -C	-	0.8	1.1	°C/W
	Q5 Thermal Resistance J -C	-	0.8	1.1	°C/W
	Q6 Thermal Resistance J -C	-	0.8	1.1	°C/W
T_J	Maximum Junction Temperature	-		175	°C
T_S	Operating Sink Temperature	-40		120	°C
T_{STG}	Storage Temperature	-40		125	°C

Notes:

* Note 1 - Max value not to exceed Tj=175°C based on max limitation of Rthjc thermal limitation and Rdson. Defined by design, not subject production testing.
* Note 2 - For Q1-Q3: Starting TJ = 25°C, L = 0.08mH, IAS = 69A, VDD = 80V during inductor charging and VDD = 0V during time in avalanche. For Q4-Q6: Starting TJ = 25°C, L = 0.08mH, IAS = 90A, VDD = 80V during inductor charging and VDD = 0V during time in avalanche.
* Note 3 - Test method compliant with MIL STD 883-1012.1.

@2017 Semiconductor Components Industries, LLC

Electrical Characteristics (T_J = 25°C, Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	D-S Breakdown Voltage (Inverter MOSFETs)	V_{GS} = 0V, I_D = 250μA	80	-	-	V
V_{GS}	Gate to Source Voltage (Inverter MOSFETs)	Gate-to-Source Voltage	-20	-	20	V
V_{TH}	Threshold Voltage (Q1-Q6)	V_{GS} = V_{DS}, I_D = 250μA, T_J = 25°C	2	3	4	V
V_{SD}	MOSFET Body Diode Forward Voltage	V_{GS} = 0V, I_S = 80A, T_J = 25°C	-	-	1	V
$R_{DS(ON)Q1}$	Inverter High Side MOSFETs Q1 (See *Note4)	V_{GS} = 10V, I_D = 80A, T_J = 25°C	-	2.4	3.5	mΩ
$R_{DS(ON)Q2}$	Inverter High Side MOSFETs Q2 (See *Note4)	V_{GS} = 10V, I_D = 80A, T_J = 25°C	-	2.4	3.5	mΩ
$R_{DS(ON)Q3}$	Inverter High Side MOSFETs Q3 (See *Note4)	V_{GS} = 10V, I_D = 80A, T_J = 25°C	-	2.5	3.7	mΩ
$R_{DS(ON)Q4}$	Inverter Low Side MOSFETs Q4 (See *Note4)	V_{GS} = 10V, I_D = 80A, T_J = 25°C	-	1.9	2.6	mΩ
$R_{DS(ON)Q5}$	Inverter Low Side MOSFETs Q5 (See *Note4)	V_{GS} = 10V, I_D = 80A, T_J = 25°C	-	2.1	2.8	mΩ
$R_{DS(ON)Q6}$	Inverter Low Side MOSFETs Q6 (See *Note4)	V_{GS} = 10V, I_D = 80A, T_J = 25°C	-	2.4	3.1	mΩ
I_{GSS}	Inverter MOSFETs (UH,UL,VH,VL,WH,WL)	V_{GS} = ±20V, V_{DS} = 0V, T_J = 25°C	-	-	±100	nA
I_{DSS}	Inverter MOSFETs Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 80V, T_J = 25°C	-	-	2	μA
Total loop resistance VLINK(+) - V0 (-)		V_{GS} = 10V, I_D = 80A, T_J = 25°C	-	5.9	7.5	mΩ

* Note 4 - High side Q1,Q2,Q3 have same die size and Rdson, Low side Q4,Q5,Q6 have same die size and Rdson. For lowest power loss, High and Low side MOSFETs have different die size and Rdson. The different Rdson values listed in the datasheet are due to the different access points available inside the module for Rdson measurement. While the high side MOSFETs (Q1, Q2, Q3) have source sense wire bonds, the low side MOSFETs (Q4, Q5, Q6) do not have source sense wire bonds, thus resulting in higher Rdson values.

Temperature Sense (NTC Thermistor)

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Voltage	Current=1mA, Temperature=25°C	7.5	-	12	V

Current Sense Resistor

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Resistance	Current Senset resistor current = 80A (See *Note5)	0.47	-	0.51	mΩ

* Note 5 - Module level measurement.

	Components	Spec	Quantity	Size
1	MOSFET	PT7 80V,bare die Rdson 2.25mΩ typical	3ea (Q1-Q3)	195 mil x 95 mil
2	MOSFET	PT7 80V,bare die Rdson 1.35mΩ typical	3ea (Q4-Q6)	200 mil x 145 mil
3	Resistor	1ohm 0.5W	1ea	142 mil x 55 mil
4	Capacitor	0.022uF 100V	1ea	79 mil x 49 mil
5	CSR	1% tolerance, 0.5ohm	1ea	250 mil x 120 mil
6	NTC	1% tolerance, 10kohm	1ea	63 mil x 32 mil

@2017 Semiconductor Components Industries, LLC

Dynamic Characteristic

C_{iss}	Input Capacitance	V_{DS} = 40V, V_{GS} = 0V, f = 1MH$_Z$ for Q1-Q3 (High side MOSFET)		-	6320	-	pF
C_{oss}	Output Capacitance			-	1030	-	pF
C_{rss}	Reverse Transfer Capacitance			-	32	-	pF
C_{iss}	Input Capacitance	V_{DS} = 40V, V_{GS} = 0V, f = 1MH$_Z$ for Q4-Q6 (Low side MOSFET)		-	10000	-	pF
C_{oss}	Output Capacitance			-	1400	-	pF
C_{rss}	Reverse Transfer Capacitance			-	95	-	pF
R_G	Gate Resistance	V_{GS} = 0V, f = 1MH$_Z$ for Q1-Q3 (High side MOSFET)		-	2.1	-	Ω
R_G	Gate Resistance	V_{GS} = 0V, f = 1MH$_Z$ for Q4-Q6 (Low side MOSFET)		-	3.3	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V	V_{DD} = 64V, I_D = 80A, I_g = 1mA	-	86	112	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 to 2V		-	12	18	nC
Q_{gs}	Gate to Source Gate Charge	for Q1-Q3 (High side MOSFET)		-	30	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge			-	18	-	nC
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V	V_{DD} = 64V, I_D = 80A, I_g = 1mA	-	131	150	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 to 2V		-	18	21	nC
Q_{gs}	Gate to Source Gate Charge	for Q4-Q6 (Low side MOSFET)		-	47	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge			-	24	-	nC

Typical Characteristics (The dynamic, switching characteristics and graphs are in reference to the FDBL86366_F085 (TOLL) datasheet (High side MOSFET)

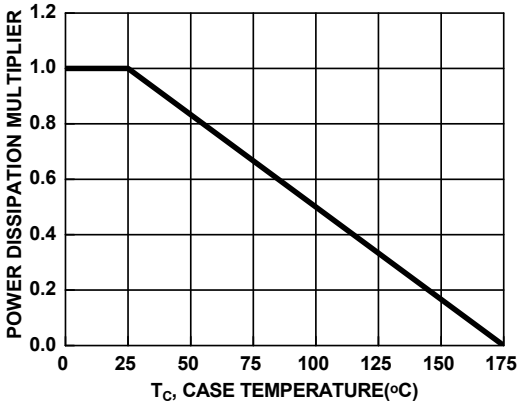


Figure 1. Normalized Power Dissipation vs. Case Temperature

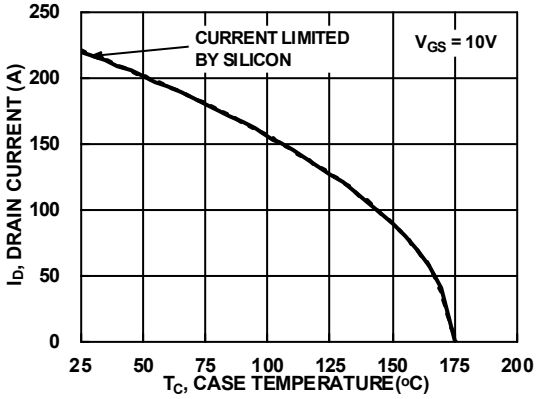


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

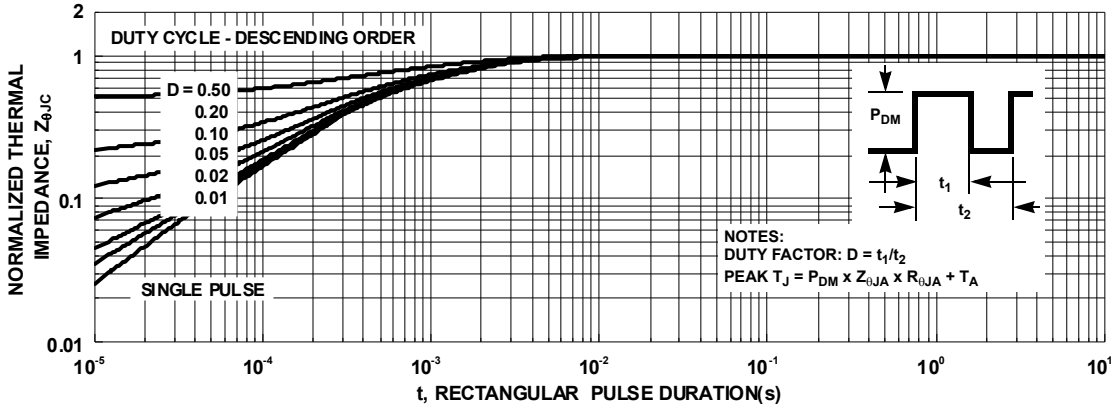


Figure 3. Normalized Maximum Transient Thermal Impedance

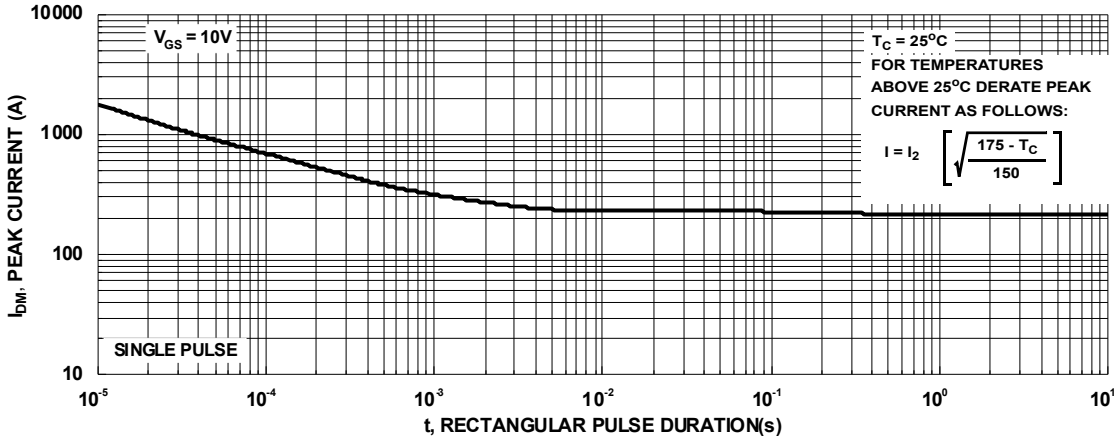


Figure 4. Peak Current Capability

Typical Characteristics (The dynamic, switching characteristics and graphs are in reference to the FDBL86366_F085 (TOLL) datasheet (High side MOSFET)

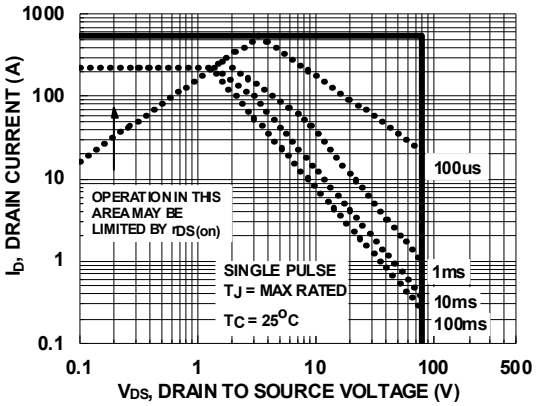


Figure 5. Forward Bias Safe Operating Area

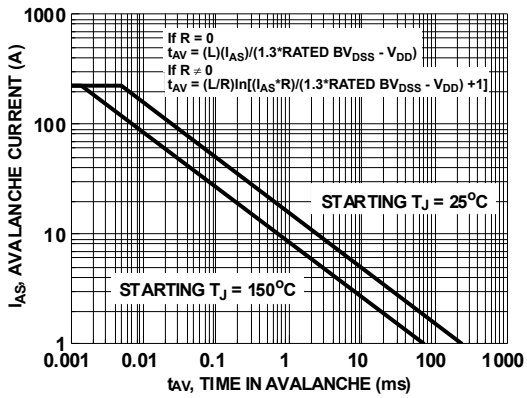


Figure 6. Unclamped Inductive Switching Capability

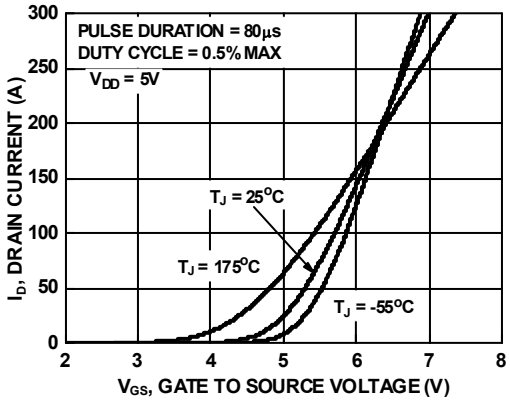


Figure 7. Transfer Characteristics

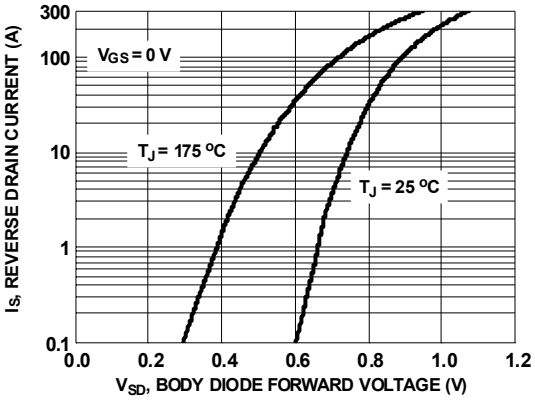


Figure 8. Forward Diode Characteristics

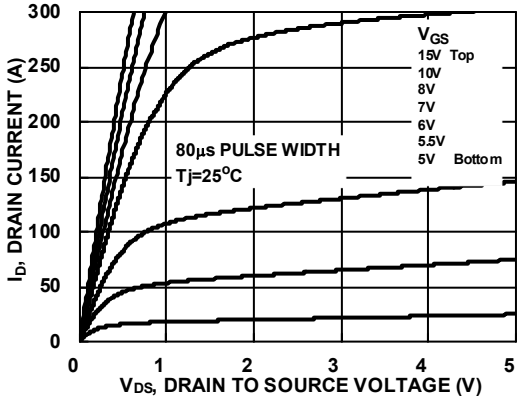


Figure 9. Saturation Characteristics

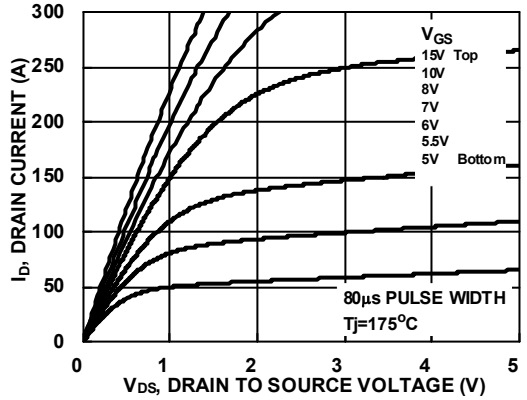


Figure 10. Saturation Characteristics

Typical Characteristics (The dynamic, switching characteristics and graphs are in reference to the FDBL86366_F085 (TOLL) datasheet (High side MOSFET)

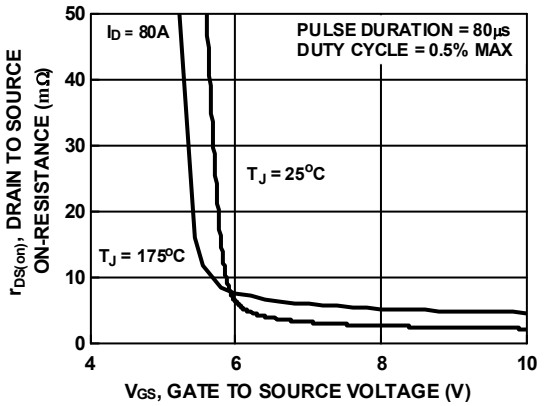


Figure 11. R_{DSON} vs. Gate Voltage

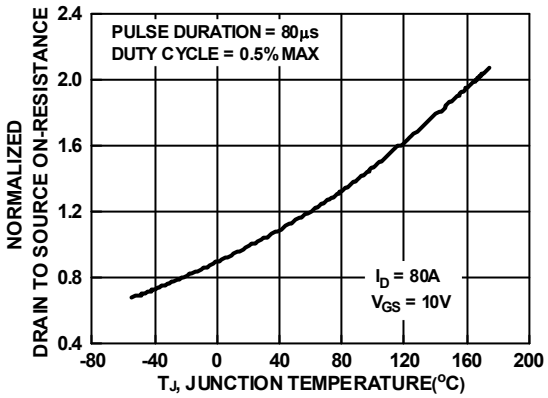


Figure 12. Normalized R_{DSON} vs. Junction Temperature

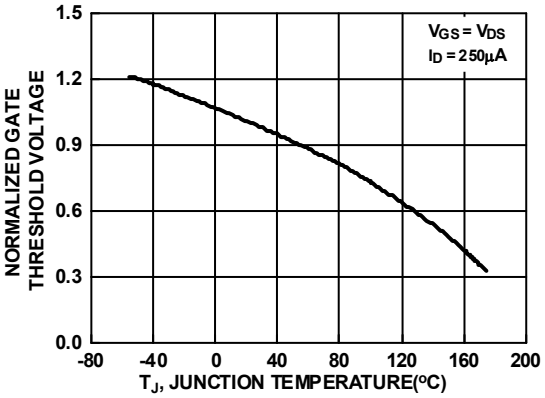


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

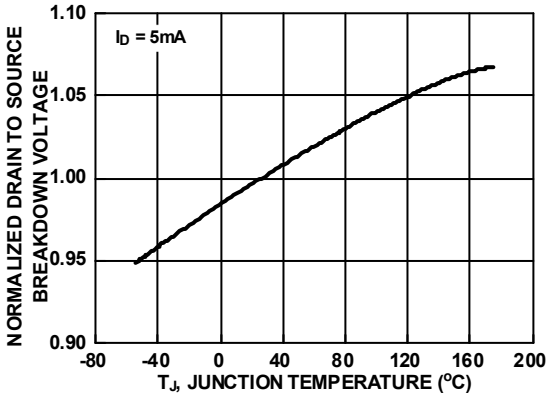


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

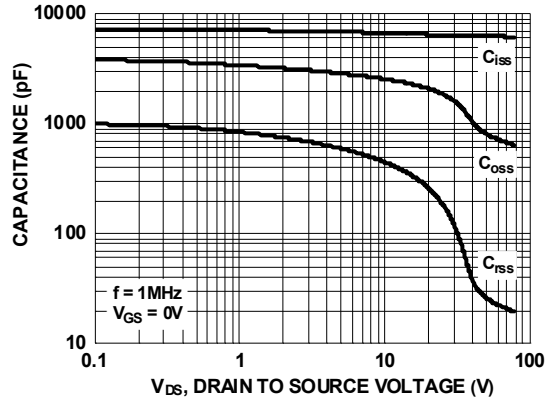


Figure 15. Capacitance vs. Drain to Source Voltage

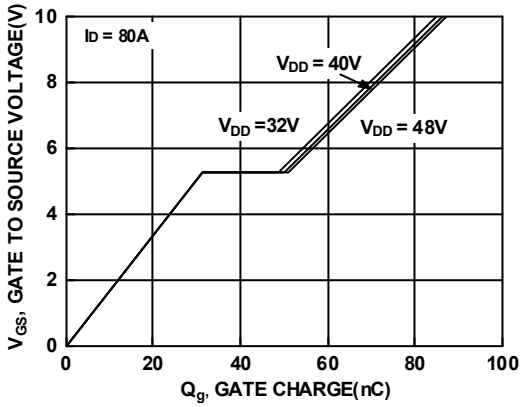


Figure 16. Gate Charge vs. Gate to Source Voltage

Typical Characteristics (The dynamic, switching characteristics and graphs are in reference to the FDBL86363_F085 (TOLL) datasheet (Low side MOSFET)

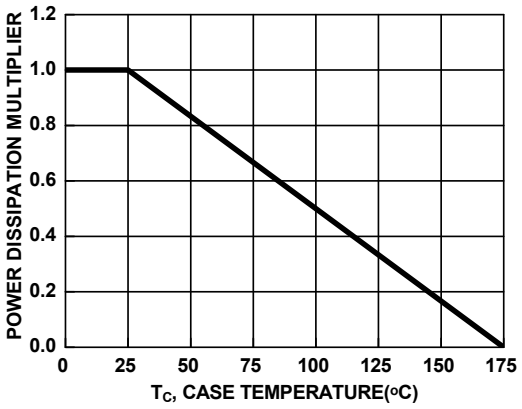


Figure 1. Normalized Power Dissipation vs. Case Temperature

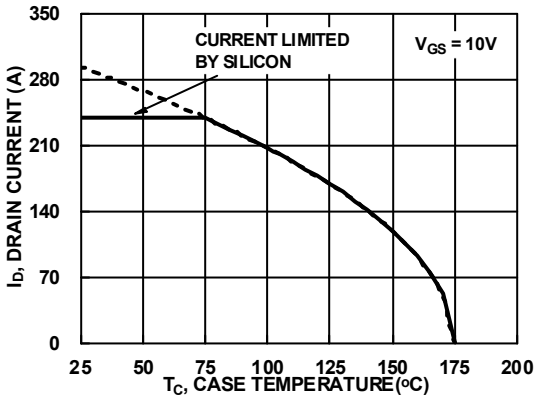


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

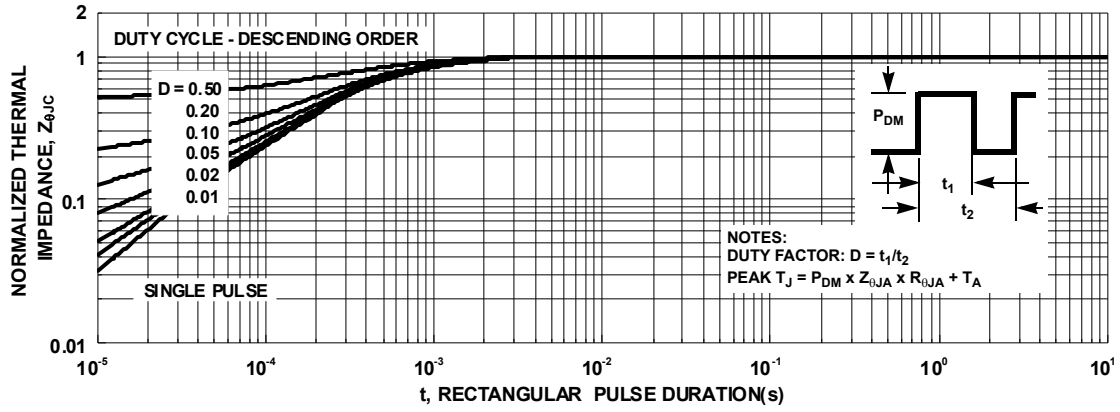


Figure 3. Normalized Maximum Transient Thermal Impedance

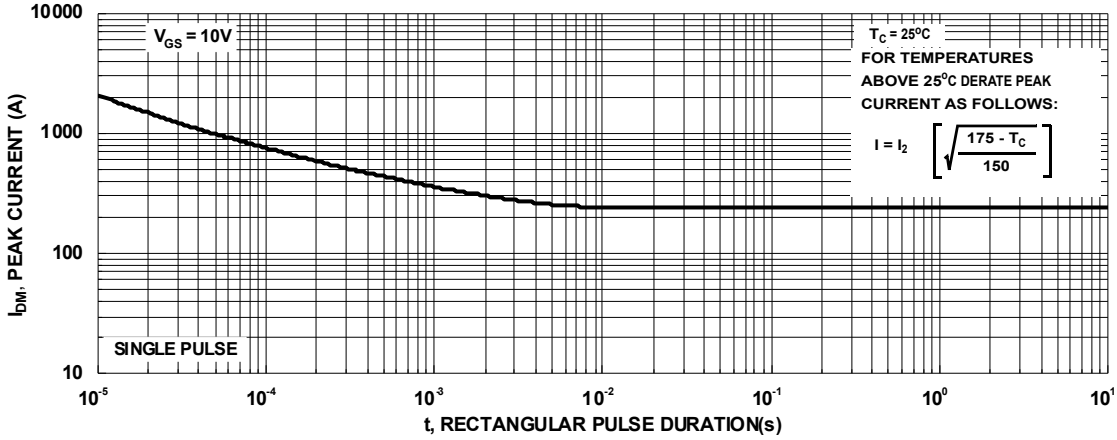


Figure 4. Peak Current Capability

Typical Characteristics (The dynamic, switching characteristics and graphs are in reference to the FDBL86363_F085 (TOLL) datasheet (Low side MOSFET)

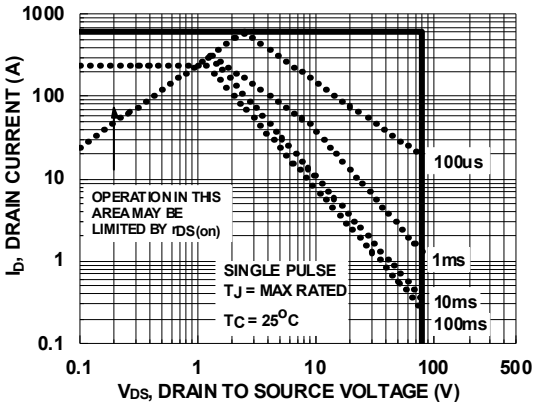


Figure 5. Forward Bias Safe Operating Area

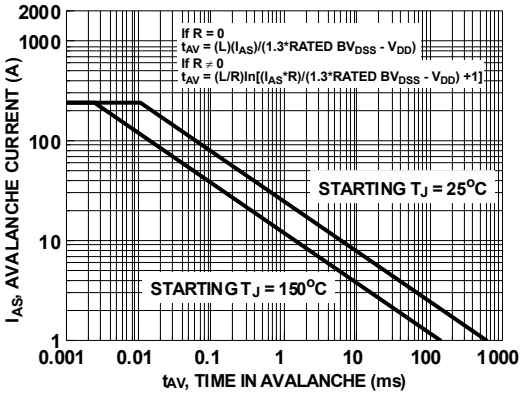


Figure 6. Unclamped Inductive Switching Capability

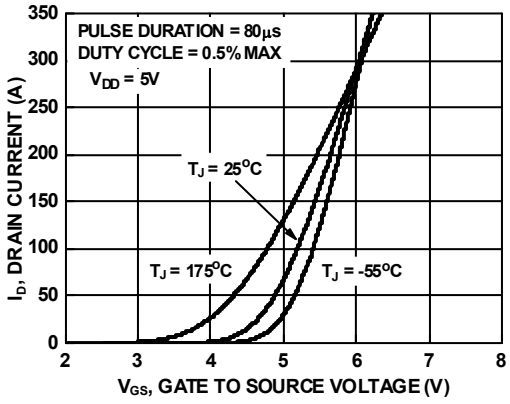


Figure 7. Transfer Characteristics

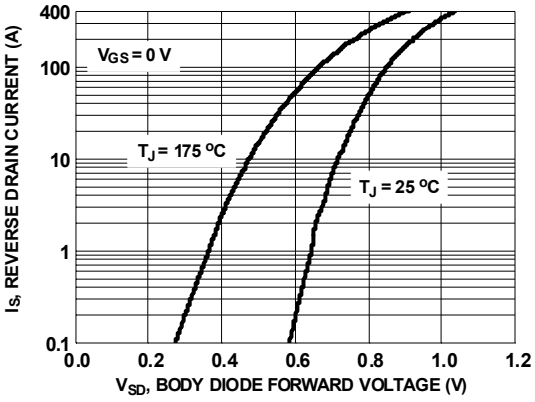


Figure 8. Forward Diode Characteristics

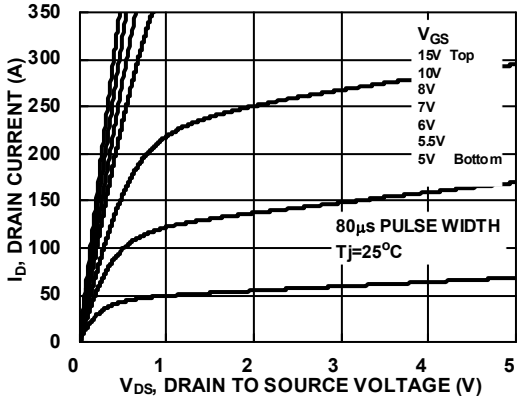


Figure 9. Saturation Characteristics

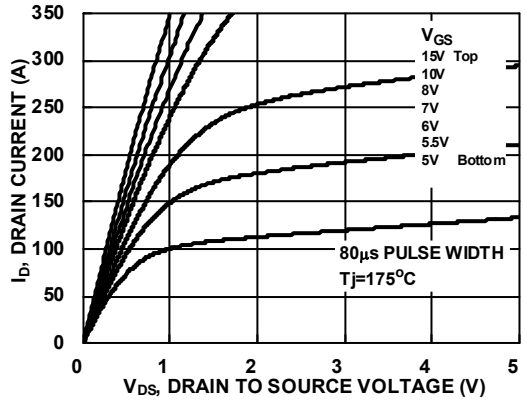


Figure 10. Saturation Characteristics

Typical Characteristics (The dynamic, switching characteristics and graphs are in reference to the FDBL86363_F085 (TOLL) datasheet (Low side MOSFET)

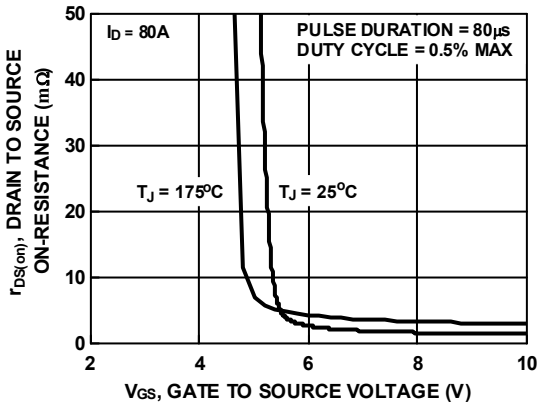


Figure 11. R_{DSON} vs. Gate Voltage

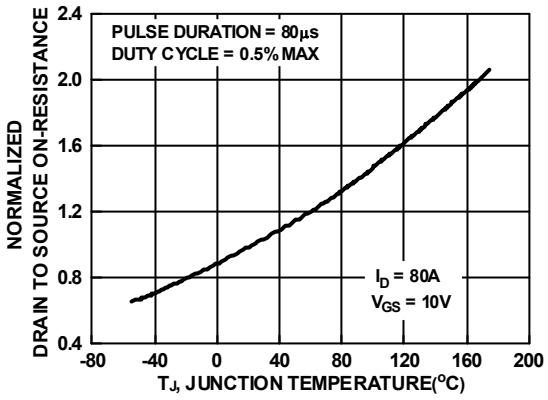


Figure 12. Normalized R_{DSON} vs. Junction Temperature

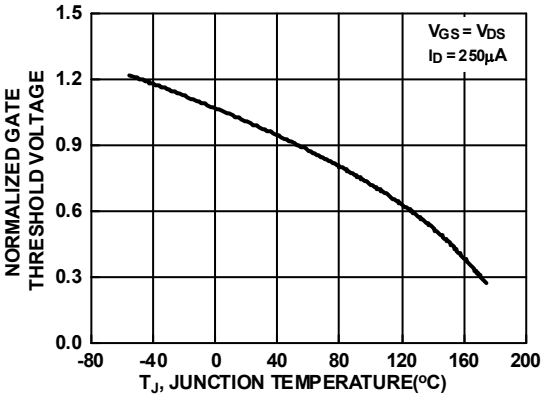


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

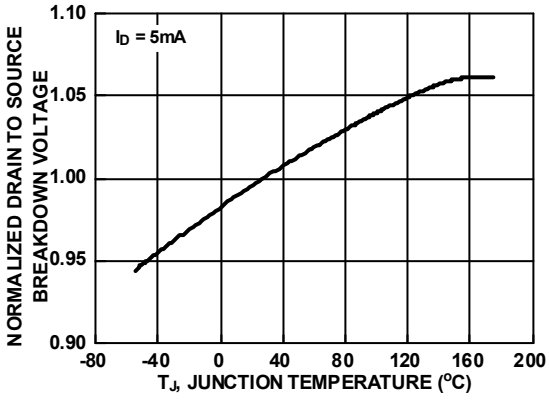


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

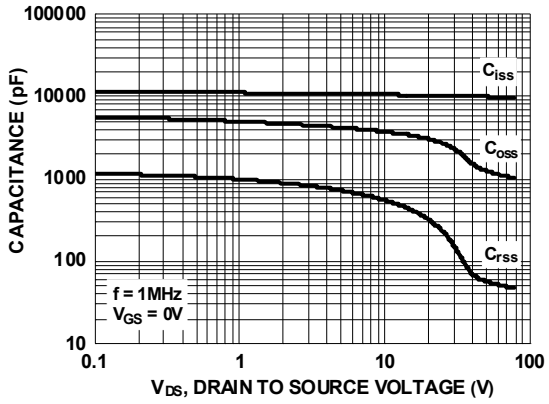


Figure 15. Capacitance vs. Drain to Source Voltage

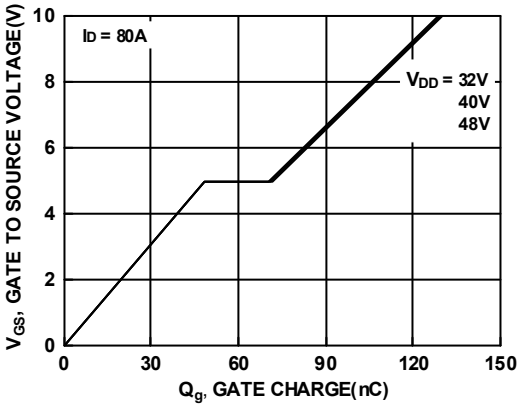
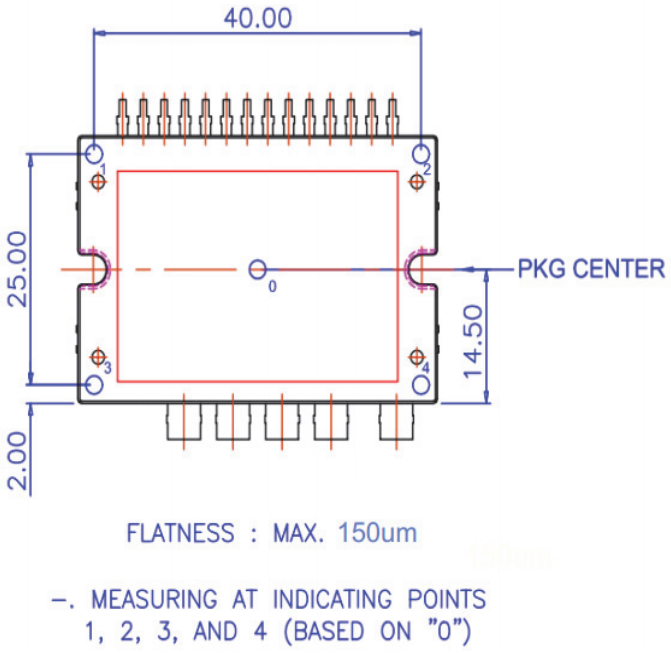


Figure 16. Gate Charge vs. Gate to Source Voltage

Mechanical Characteristics and Ratings

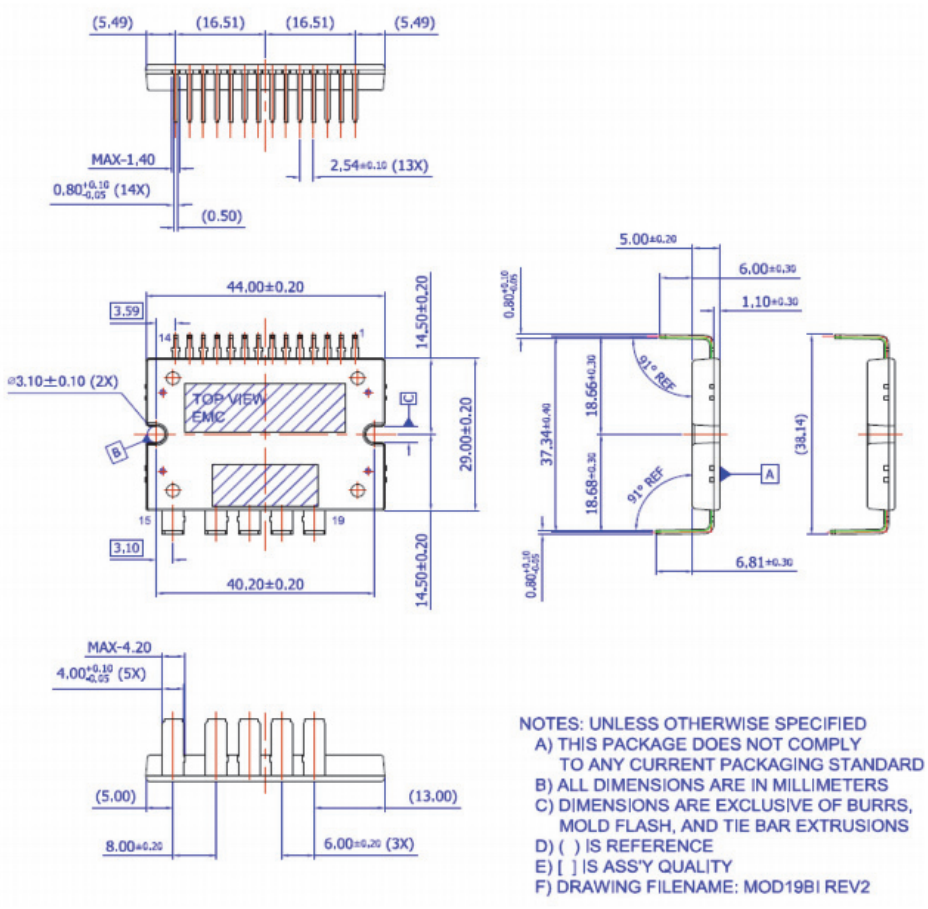
Parameter	Condition	Limits			Units
		Min.	Typ.	Max.	
Device Flatness	Note Fig.15	0	-	+150	μm
Mounting Torque	Mounting Screw: -M3, Recommended 0.7N.m	0.4	-	0.8	N.m
Weight		-	20	-	g



Package Marking and Ordering Information

Device Marking	Packing Type	Quantity
FTCO3V85A1	Tube	11

Detailed Package Outline Drawings



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE
E) [ ] IS ASS'Y QUALITY
F) DRAWING FILENAME: MOD19BI REV2

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada.
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative