

FQP11N40C, FQPF11N40C

QFET[®] MOSFET, N-Channel

400 V, 10.5 A, 530 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

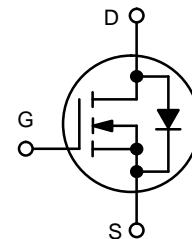
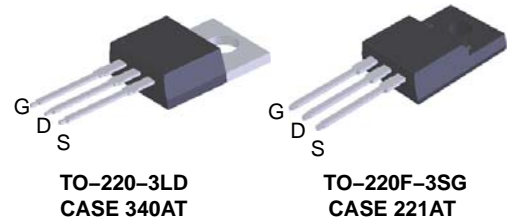
Features

- 10.5 A, 400 V, $R_{DS(on)} = 530 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 5.25 \text{ A}$
- Low Gate Charge (Typ. 28 nC)
- Low Crss (Typ. 85 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant



ON Semiconductor[®]

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ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

FQP11N40C, FQPF11N40C

ORDERING INFORMATION

Device	Device Marking	Package	Shipping
FQP11N40C	FQP11N40C	TO-220 (Pb-Free)	1,000 Units / Tube
FQPF11N40C	FQPF11N40C	TO-220 Fullpack, TO-220F-3SG (Pb-Free)	1,000 Units / Tube

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	FQP11N40C	FQPF11N40C	Unit
V_{DSS}	Drain to Source Voltage	400		V
I_D	Drain Current –Continuous ($T_C = 25^\circ\text{C}$) –Continuous ($T_C = 100^\circ\text{C}$)	10.5	10.5 *	A
		6.6	6.6 *	A
I_{DM}	Drain Current – Pulsed (Note 1)	42	42 *	A
V_{GSS}	Gate to Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	360		mJ
I_{AR}	Avalanche Current (Note 1)	11		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	13.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) – Derate above 25°C	135	44	W
		1.07	0.35	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to 150		$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $L = 5.7 \text{ mH}$, $I_{AS} = 10.5 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 10.5 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	FQP11N40C	FQPF11N40C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.93	2.86	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	62.5	$^\circ\text{C}/\text{W}$

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	400			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.54		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 400 V, V _{GS} = 0 V			1	μA
		V _{DS} = 320 V, T _C = 125°C			10	μA
I _{GSSF}	Gate–Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate–Body Leakage Current, Reverse	V _{GS} = –30 V, V _{DS} = 0 V			–100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0		4.0	V
r _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 5.25 A		0.43	0.53	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 5.25 A		7.1		s

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		840	1090	pF
C _{oss}	Output Capacitance			250	325	pF
C _{rss}	Reverse Transfer Capacitance			85	110	pF

Switching Characteristics

t _{d(on)}	Turn–On Delay Time	V _{DD} = 200 V, I _D = 10.5 A, R _G = 25 Ω (Note 4)		14	40	ns
t _r	Turn–On Rise Time			89	190	ns
t _{d(off)}	Turn–Off Delay Time			81	170	ns
t _f	Turn–Off Fall Time			81	170	ns
Q _g	Total Gate Charge	V _{DS} = 320 V, I _D = 10.5 A, R _G = 25 Ω (Note 4)		28	35	nC
Q _{gs}	Gate–Source Charge			4		nC
Q _{gd}	Gate–Drain Charge			15		nC

Drain–Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain–Source Diode Forward Current				10.5	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current				42	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 10.5 A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 10.5 A, dI _F /dt = 100 A/μs		290		ns
Q _{rr}	Reverse Recovery Charge			2.4		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

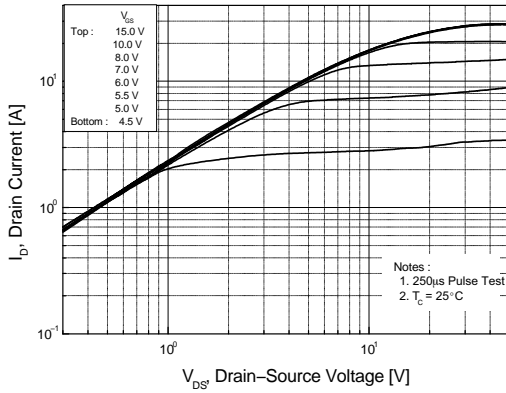


Figure 1. On-Region Characteristics

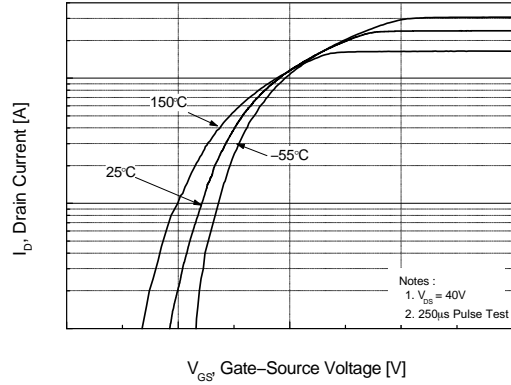


Figure 2. Transfer Characteristics

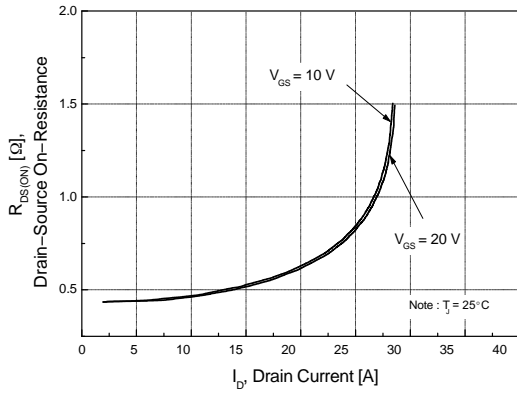


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

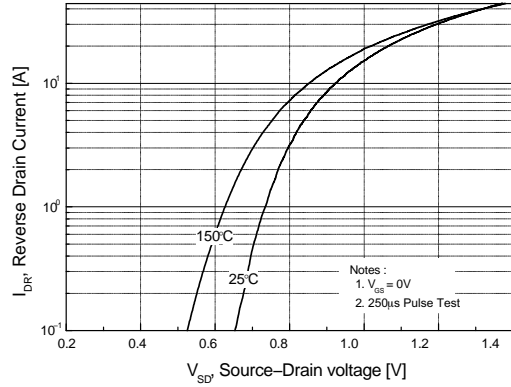


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

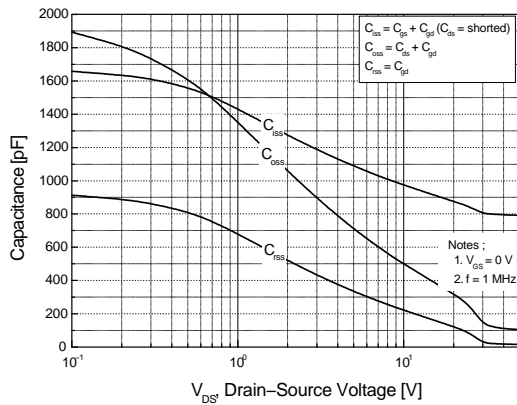


Figure 5. Capacitance Characteristics

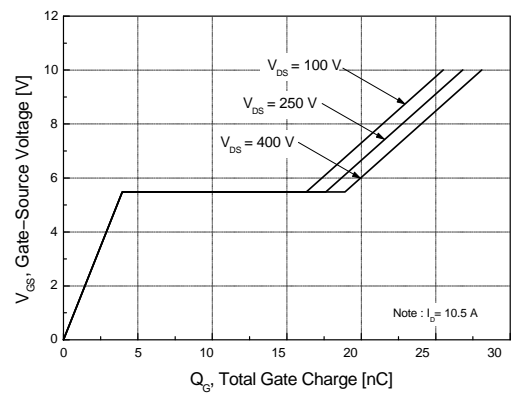


Figure 6. Gate Charge Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS

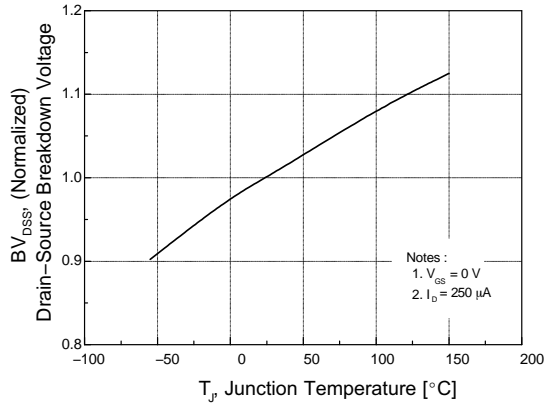


Figure 7. Breakdown Voltage Variation vs. Temperature

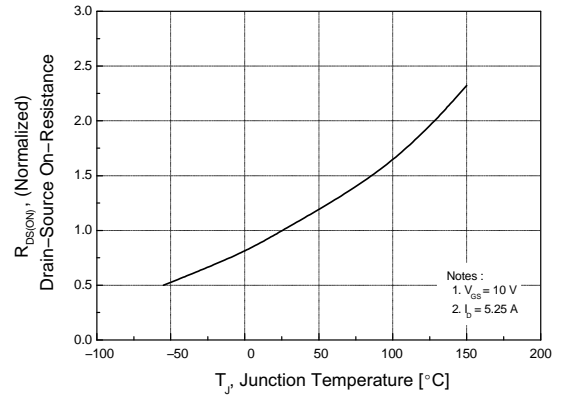


Figure 8. On-Resistance Variation vs. Temperature

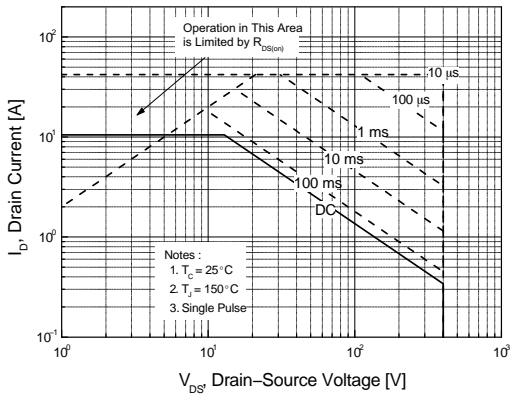


Figure 9. Maximum Safe Operating Area of FQP11N40C

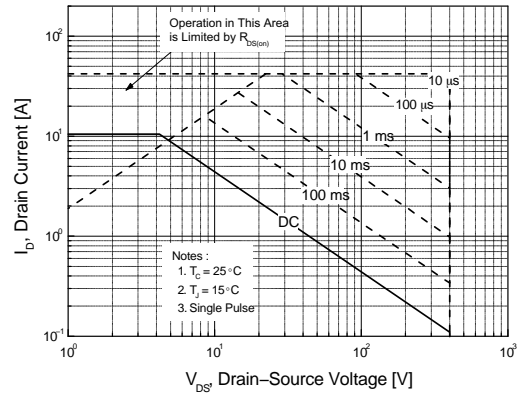


Figure 10. Maximum Safe Operating Area of FQPF11N40C

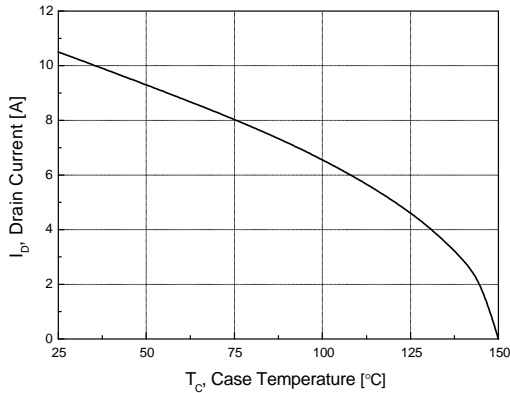


Figure 11. Maximum Drain Current

FQP11N40C, FQPF11N40C

TYPICAL PERFORMANCE CHARACTERISTICS

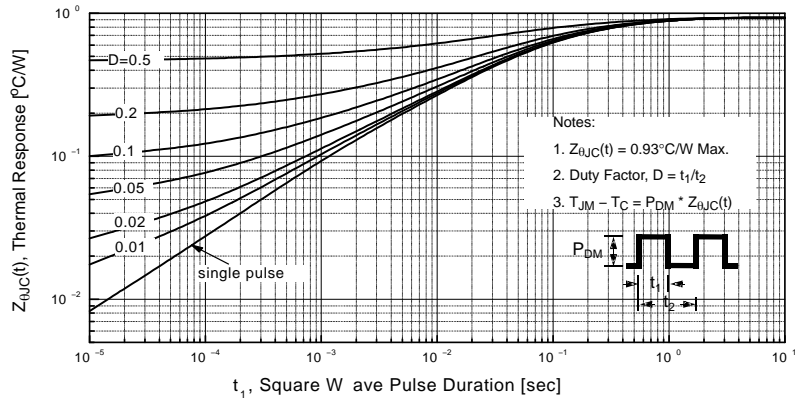


Figure 12. Transient Thermal Response Curve of FQP11N40C

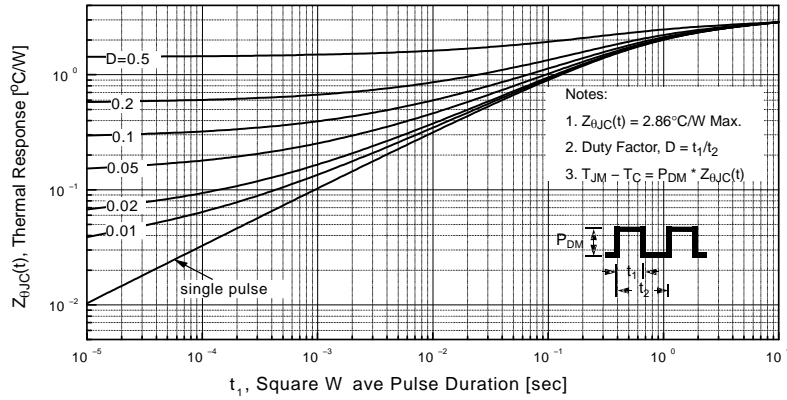


Figure 13. Transient Thermal Response Curve of FQPF11N40C

FQP11N40C, FQPF11N40C

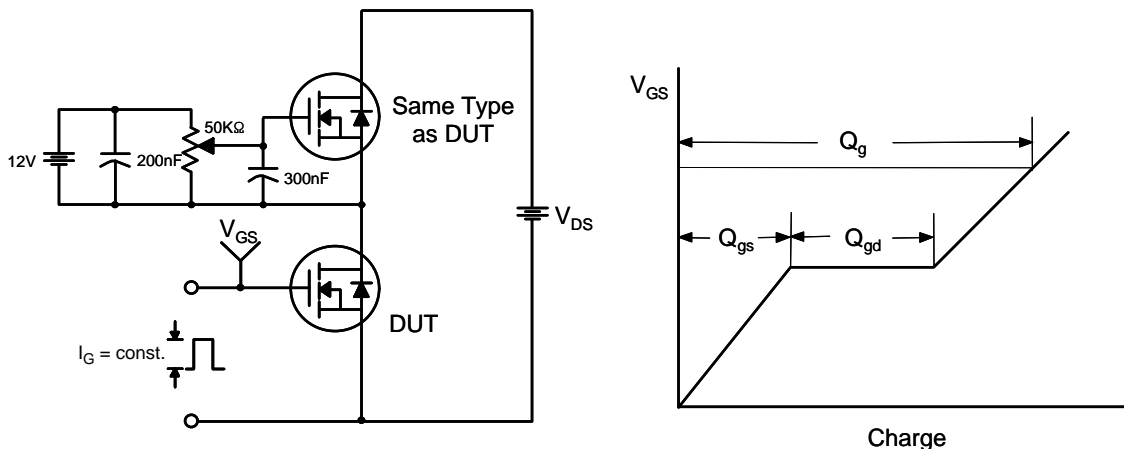


Figure 14. Gate Charge Test Circuit & Waveform

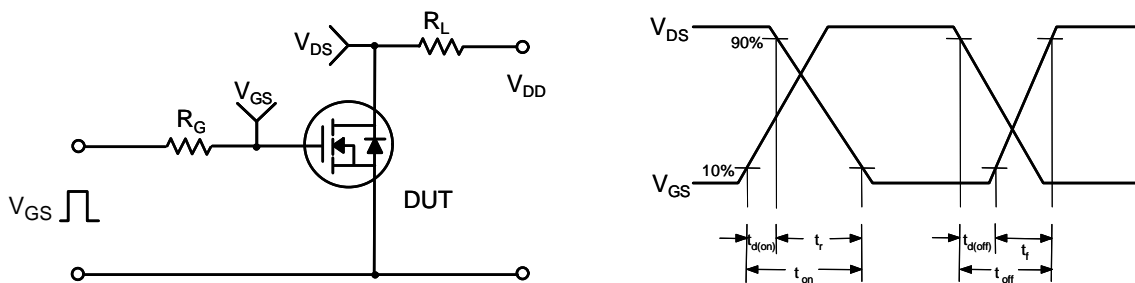


Figure 15. Resistive Switching Test Circuit & Waveforms

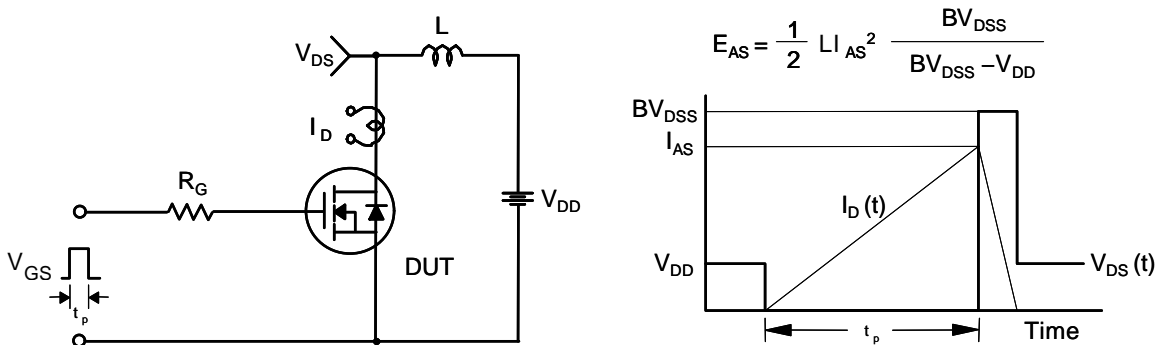


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

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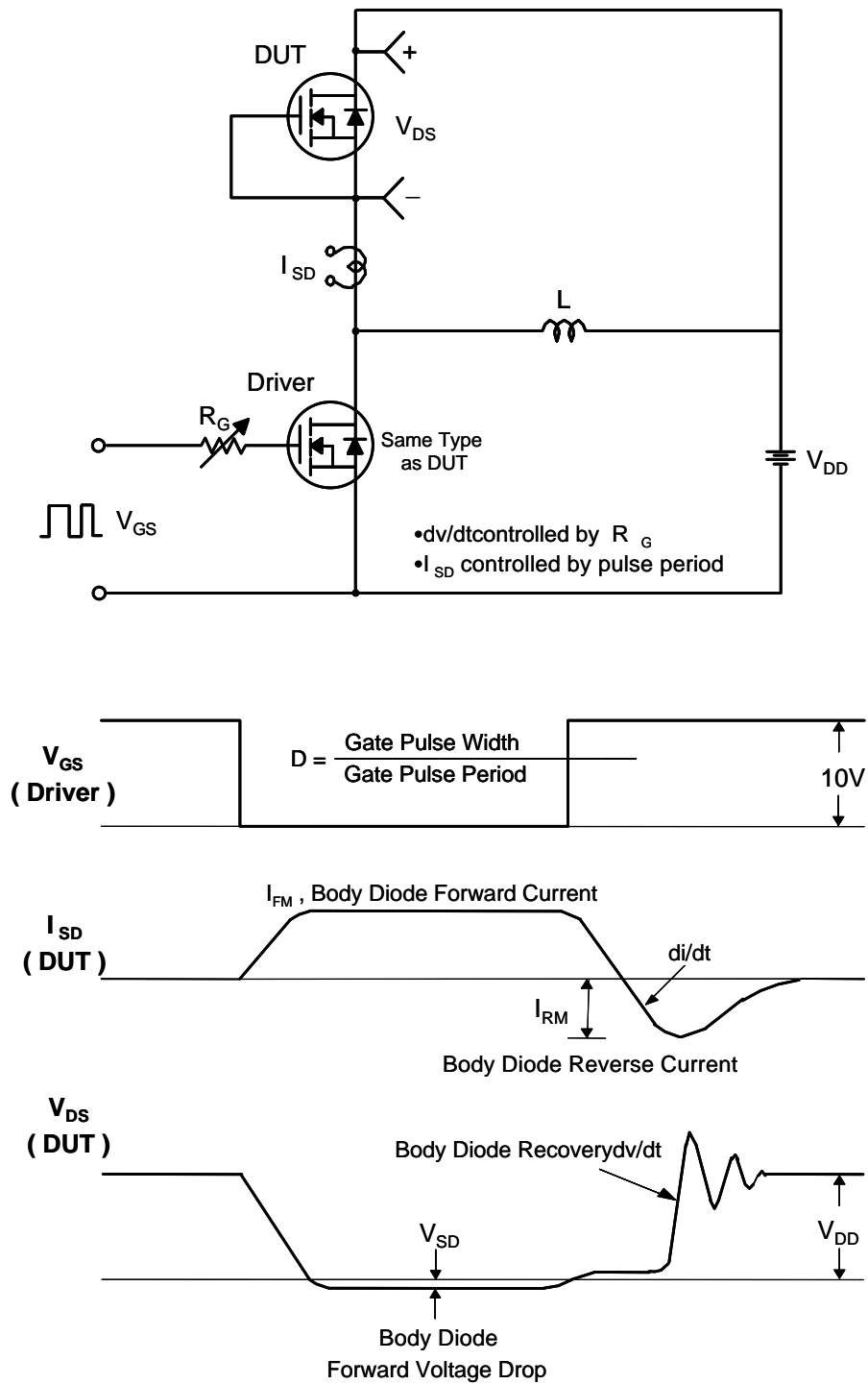


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

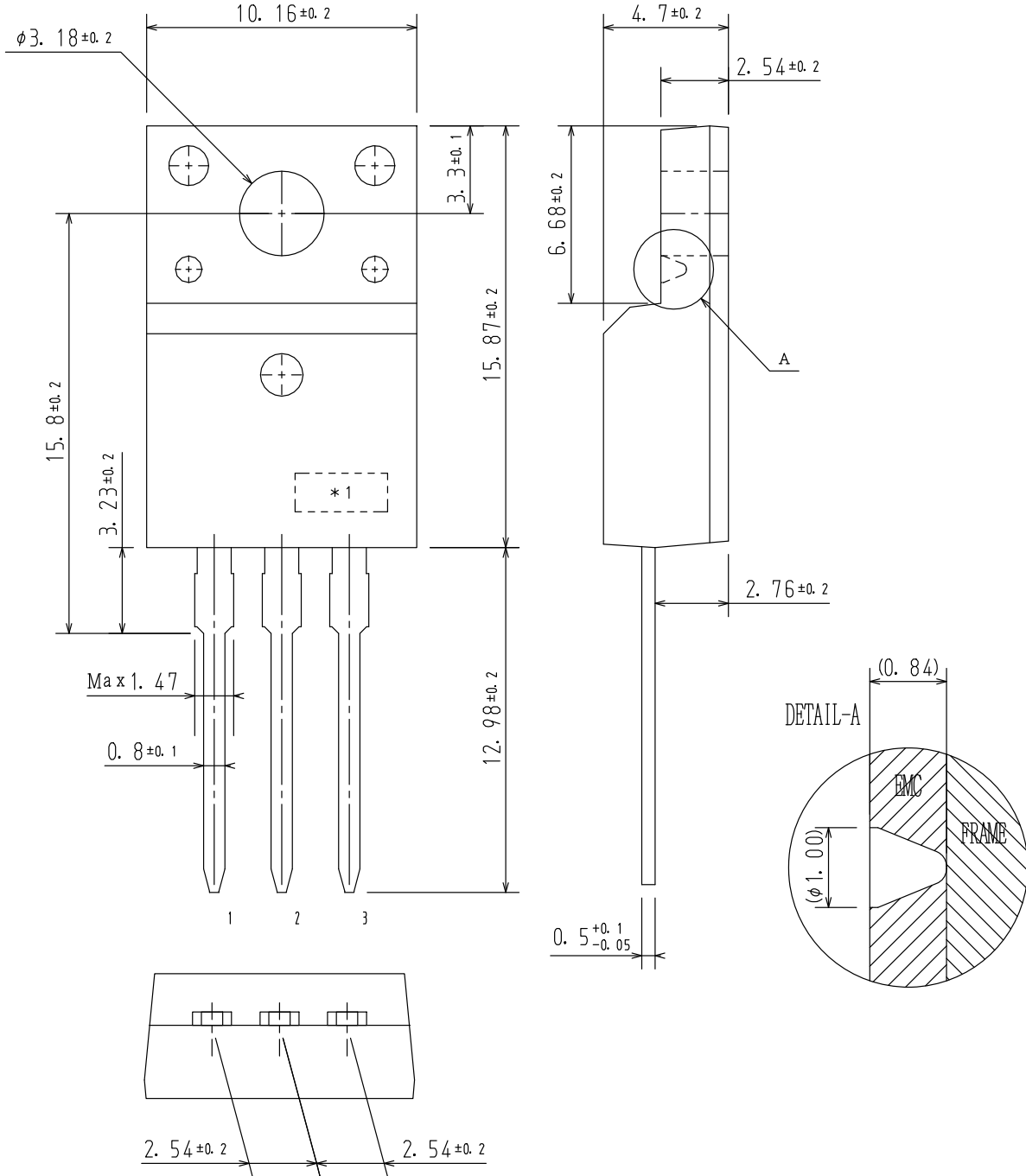
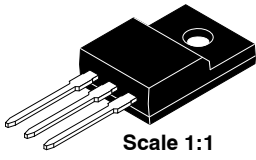
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



TO-220 Fullpack, 3-Lead / TO-220F-3SG
CASE 221AT
ISSUE A

DATE 12 NOV 2013



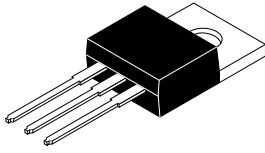
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

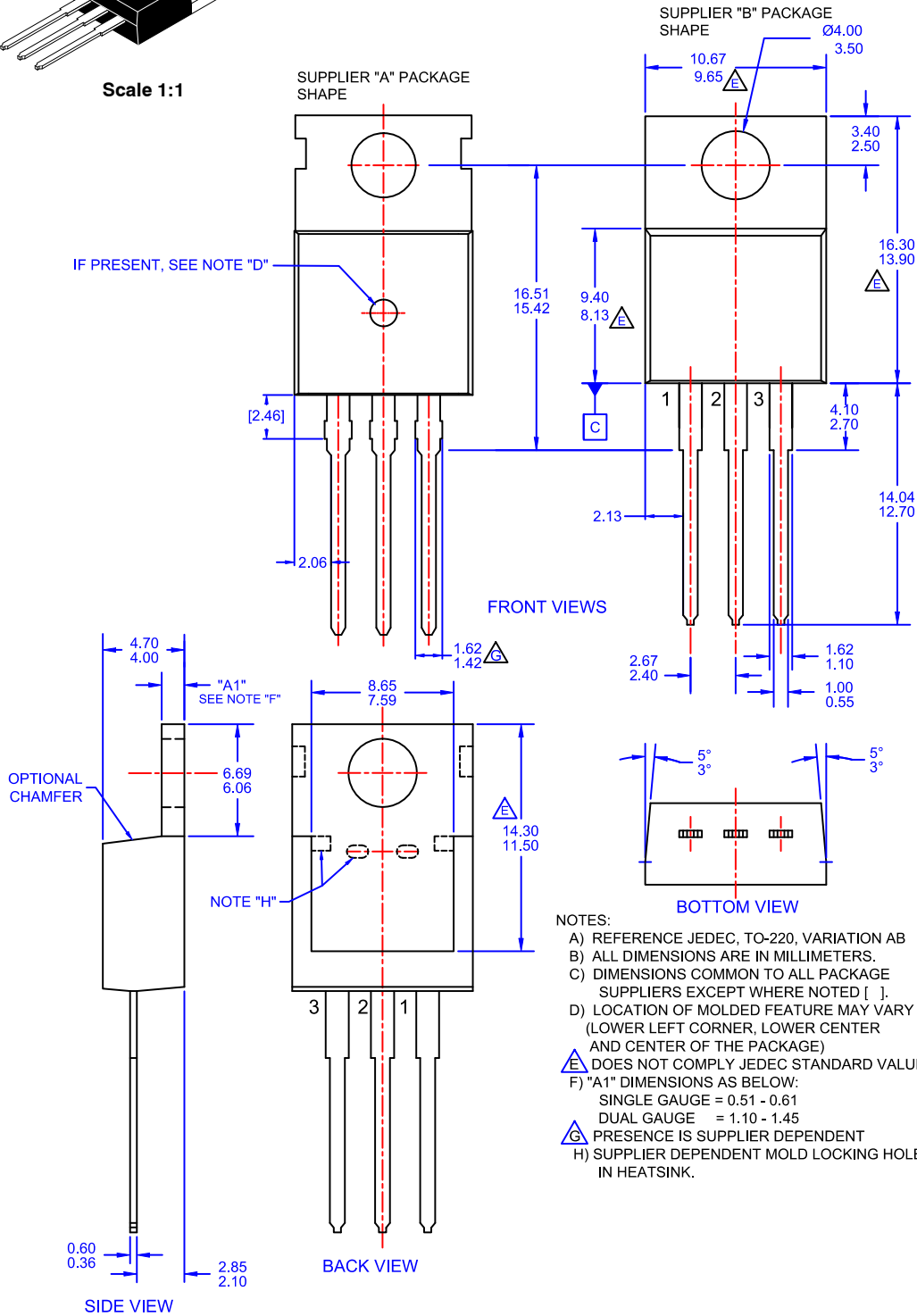
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Scale 1:1

TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E) DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
 SINGLE GAUGE = 0.51 - 0.61
 DUAL GAUGE = 1.10 - 1.45
- G) PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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