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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

November 2013

FDMC610P

P-Channel PowerTrench® MOSFET

-12 V, -80 A, 3.9 mΩ

Features

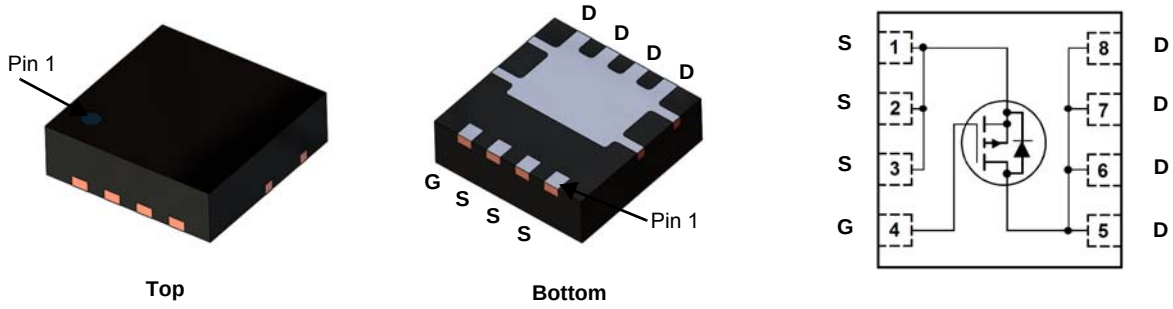
- Max $r_{DS(on)}$ = 3.9 mΩ at V_{GS} = -4.5 V, I_D = -22 A
- Max $r_{DS(on)}$ = 6.4 mΩ at V_{GS} = -2.5 V, I_D = -16 A
- State-of-the-art switching performance
- Lower output capacitance, gate resistance, and gate charge boost efficiency
- Shielded gate technology reduces switch node ringing and increases immunity to EMI and cross conduction
- RoHS Compliant

General Description

This P-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- High side switching for high end computing
- High power density DC-DC synchronous buck converter



Top Bottom

Power 33

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-12	V
V_{GS}	Gate to Source Voltage			±8	V
I_D	Drain Current - Continuous	T_C = 25 °C		-80	A
	- Continuous		(Note 1a)	-22	
	- Pulsed			-200	
P_D	Power Dissipation	T_C = 25 °C		48	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	T_C = 25 °C		2.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	T_A = 25 °C	(Note 1a)	53	

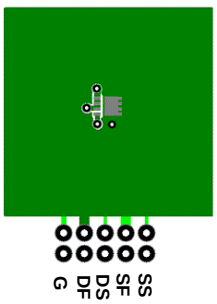
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
23AB	FDMC610P	Power 33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 µA , V_{GS} = 0 V	-12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 µA , referenced to 25 °C		-13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -9.6 V, V_{GS} = 0 V			-1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 µA	-0.4	-0.7	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 µA , referenced to 25 °C		3.1		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5 V, I_D = -22 A		2.8	3.9	mΩ
		V_{GS} = -2.5 V, I_D = -16 A		3.7	6.4	
		V_{GS} = -4.5 V, I_D = -22 A,T_J = 125 °C		3.6	5.4	
g_{FS}	Forward Transconductance	V_{DD} = -5 V, I_D = -22 A		16		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -6 V, V_{GS} = 0 V, f = 1 MHz		0.89	1.25	nF
C_{oss}	Output Capacitance			1620	2270	pF
C_{rss}	Reverse Transfer Capacitance			1440	2015	pF
R_g	Gate Resistance		0.1	3.6	7.2	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -6 V, I_D = -22 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		24	39	ns
t_r	Rise Time			37	60	ns
$t_{d(off)}$	Turn-Off Delay Time			193	309	ns
t_f	Fall Time			87	139	ns
Q_g	Total Gate Charge	V_{DD} = -6 V, I_D = -22 A, V_{GS} = -4.5 V		71	99	nC
Q_{gs}	Gate to Source Charge			13		nC
Q_{gd}	Gate to Drain “Miller” Charge			14		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2 A (Note 2)		-0.6	-1.2	V
		V_{GS} = 0 V, I_S = -22 A (Note 2)		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -22 A, di/dt = 100 A/µs		36	58	ns
Q_{rr}	Reverse Recovery Charge			19	33	nC

Note:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25 °C unless otherwise noted

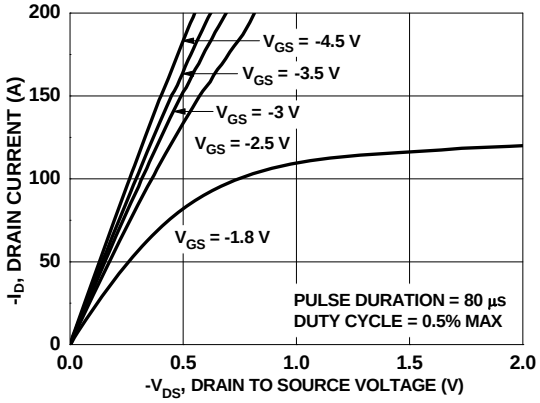


Figure 1. On Region Characteristics

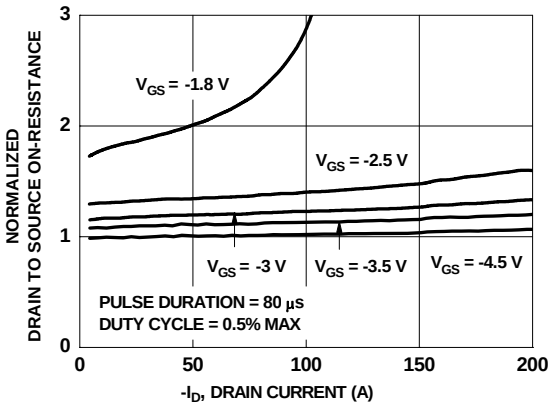


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

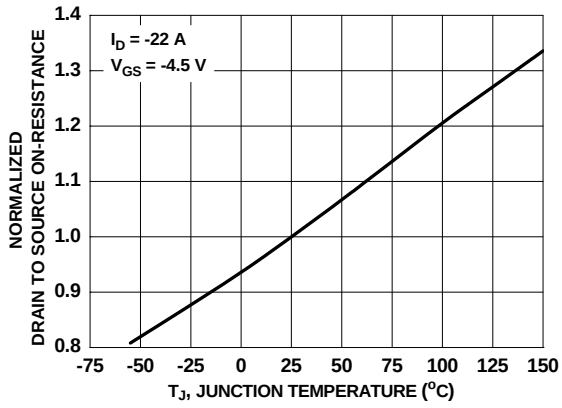


Figure 3. Normalized On Resistance vs Junction Temperature

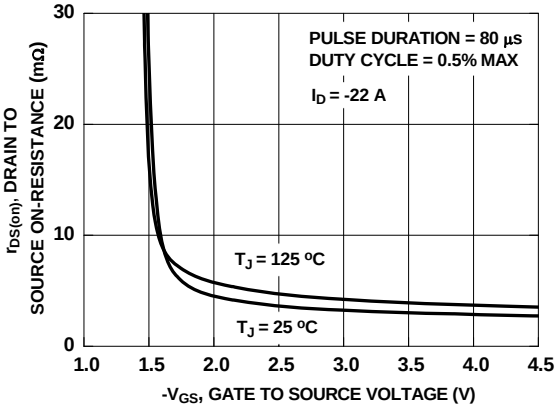


Figure 4. On-Resistance vs Gate to Source Voltage

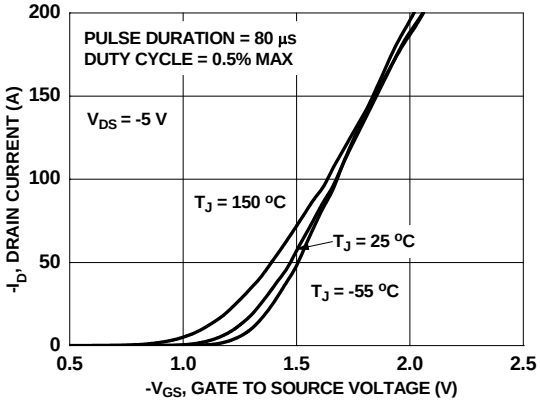


Figure 5. Transfer Characteristics

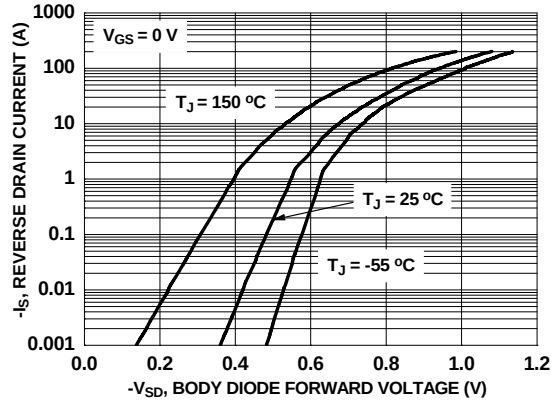


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

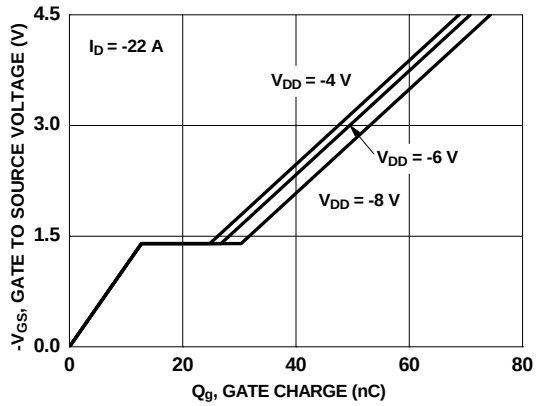


Figure 7. Gate Charge Characteristics

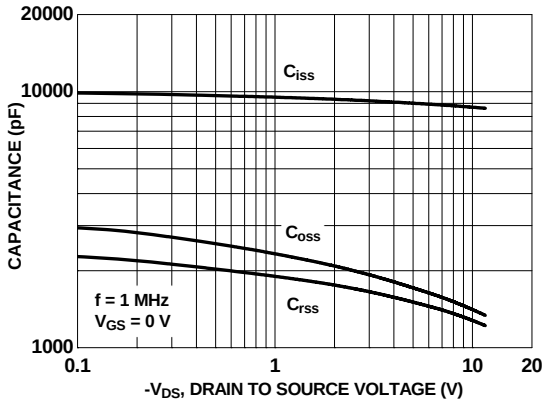


Figure 8. Capacitance vs Drain to Source Voltage

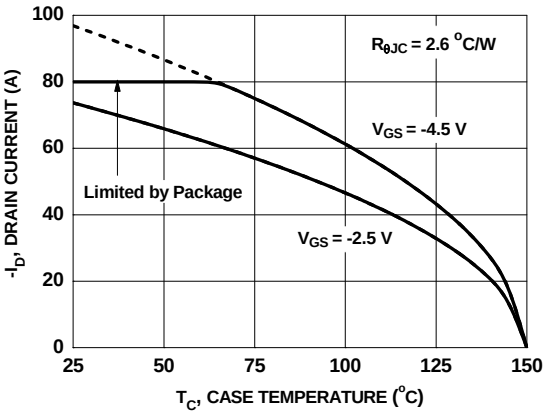


Figure 9. Maximum Continuous Drain Current vs Case Temperature

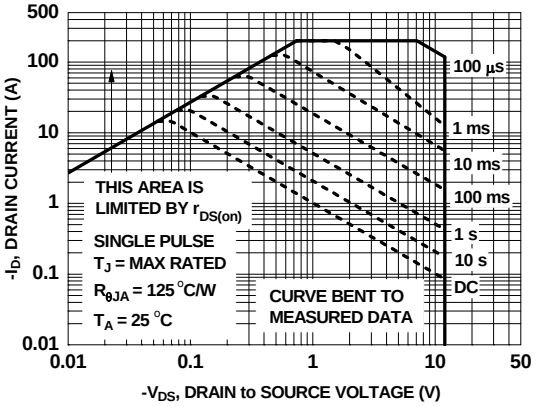


Figure 10. Forward Bias Safe Operating Area

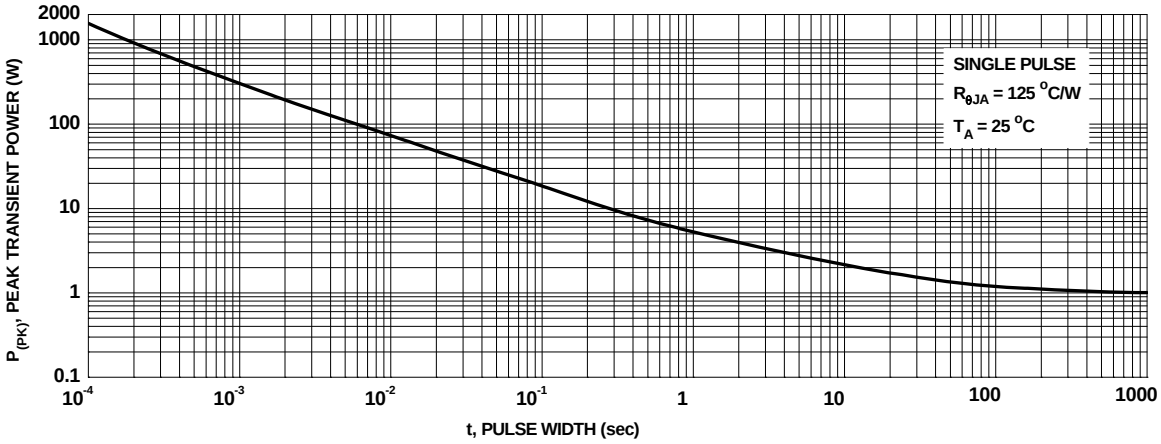


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

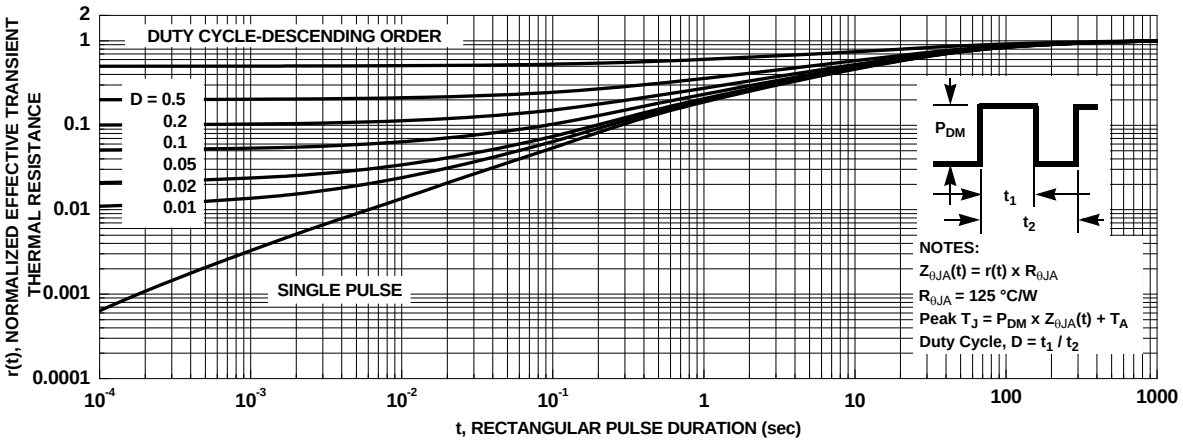
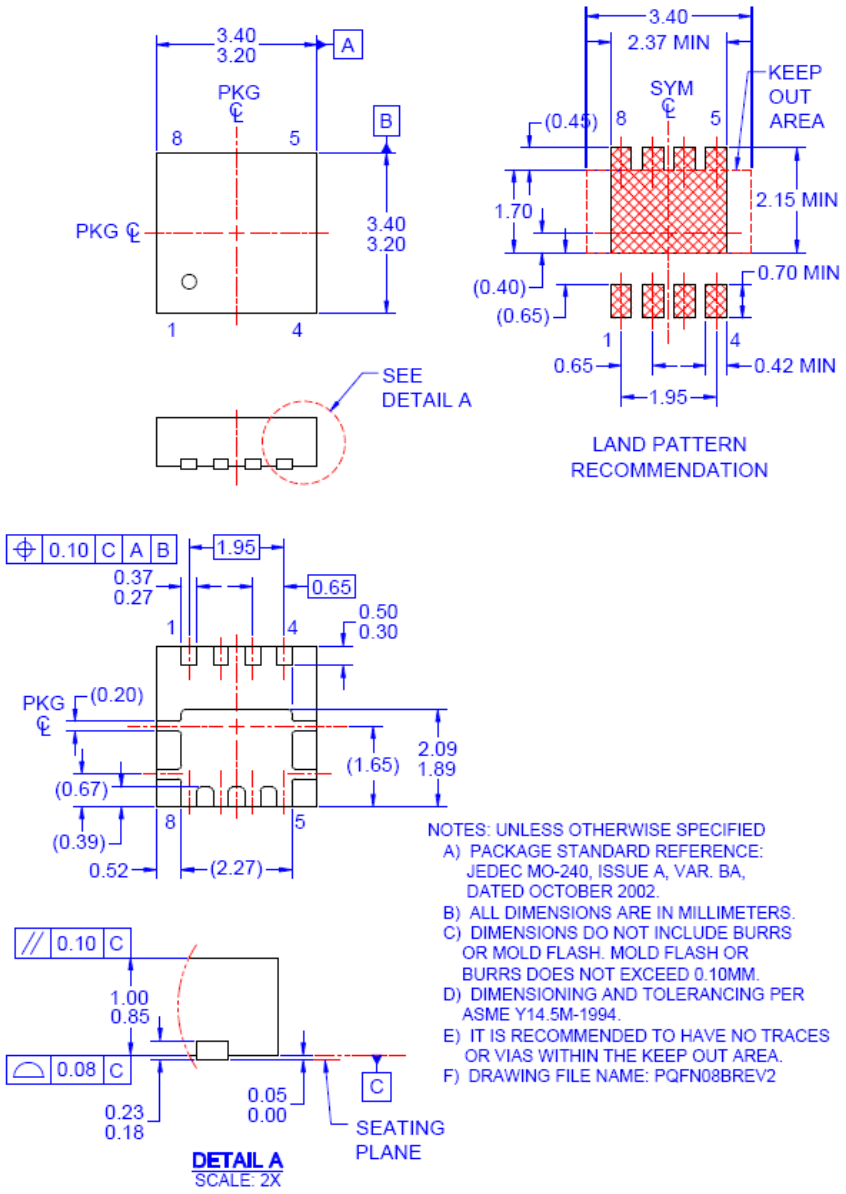


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



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A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: PQFN08BREV2

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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