Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

DATA SHEET

74ALVCH16843
18-bit bus-interface D-type latch (3-State)

Product specification

1998 Aug 04

IC24 Data Handbook

Philips
Semiconductors

PHILIPS

18-bit bus interface D-type latch (3-State) 74ALVCH16843

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

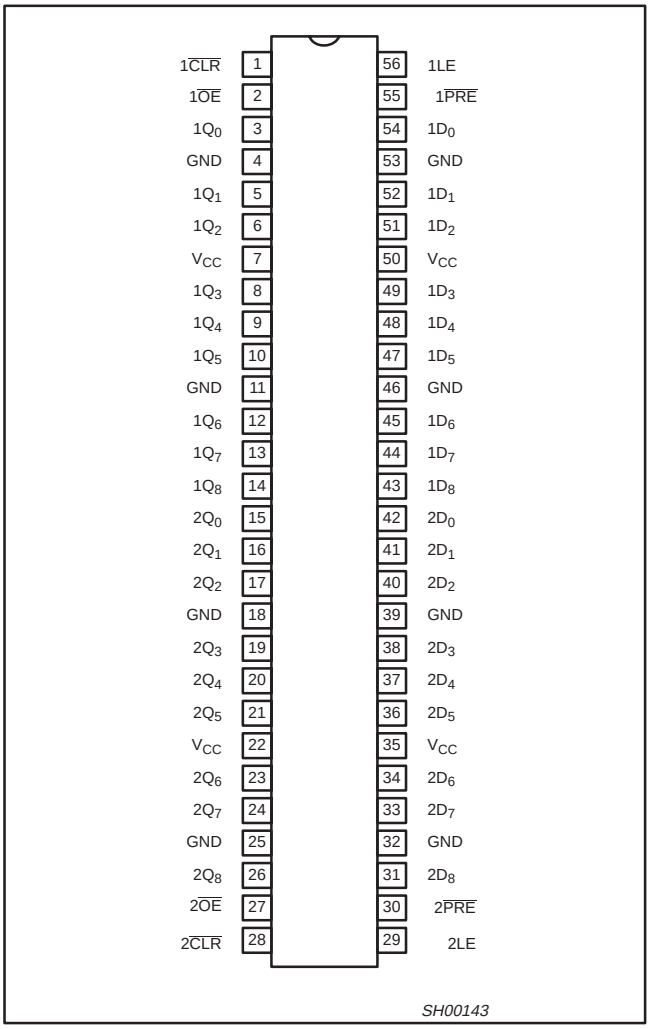
DESCRIPTION

The 74ALVCH16843 has two 9–bit D-type latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable (nLE), clear ($n\overline{CLR}$), preset ($n\overline{PRE}$) and output enable ($n\overline{OE}$) control gates.

When $n\overline{OE}$ is LOW, the data in the registers appear at the outputs. When $n\overline{OE}$ is HIGH, the outputs are in the high impedance OFF state. Operation of the $n\overline{OE}$ input does not affect the state of the flip-flops.

The 74ALVCH16843 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nDn to nQn	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.2 2.1	ns
	Propagation delay nLE to nQn	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.3 2.0	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	transparent mode Output enabled Output disabled	 17 3	pF
			Clocked mode Output enabled Output disabled	 19 9	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74ALVCH16843 DGG	ACH16843 DGG	SOT364-1

PIN DESCRIPTION

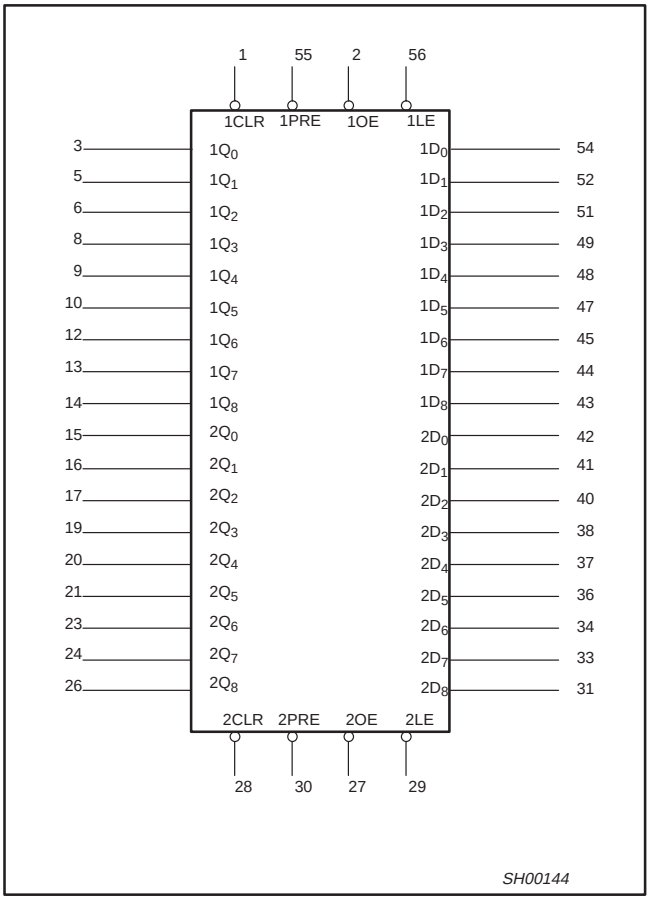
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{CLR}$	Clear input (active LOW)
2	$1\overline{OE}$	Output enable input (active LOW)
55	$1\overline{PRE}$	Preset input (active LOW)
56	1LE	Latch enable input (active HIGH)
54, 52, 51, 49, 48, 47, 45, 44, 43	1D0 to 1D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14	1Q0 to 1Q8	Data outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$2\overline{OE}$	Output enable input (active LOW)
28	$2\overline{CLR}$	Clear input (active LOW)
29	2LE	Latch enable input (active HIGH)
30	$2\overline{PRE}$	Preset input (active LOW)
42, 41, 40, 38, 37, 36, 34, 33, 31	2D0 to 2D8	Data inputs
15, 16, 17, 19, 20, 21, 23, 24, 26	2Q0 to 2Q8	Data outputs

FUNCTION TABLE

INPUTS					OUTPUT
$n\overline{PRE}$	$n\overline{CLR}$	$n\overline{OE}$	LE	D_X	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	H	X	Q_0
X	X	H	H	X	Z

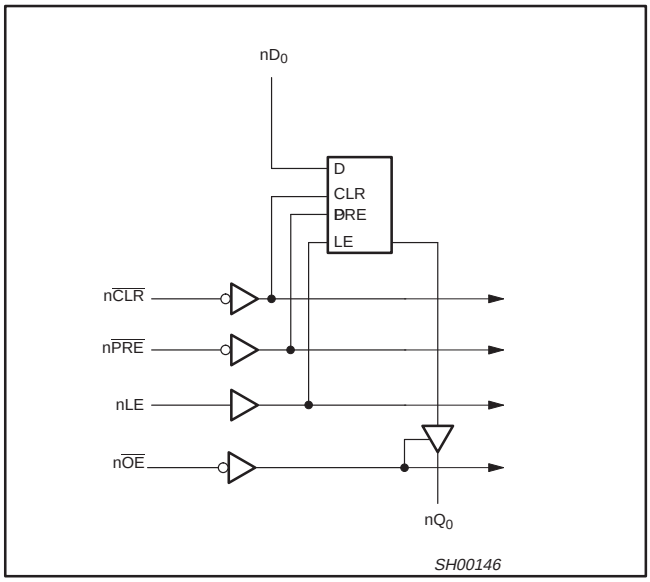
H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

LOGIC SYMBOL

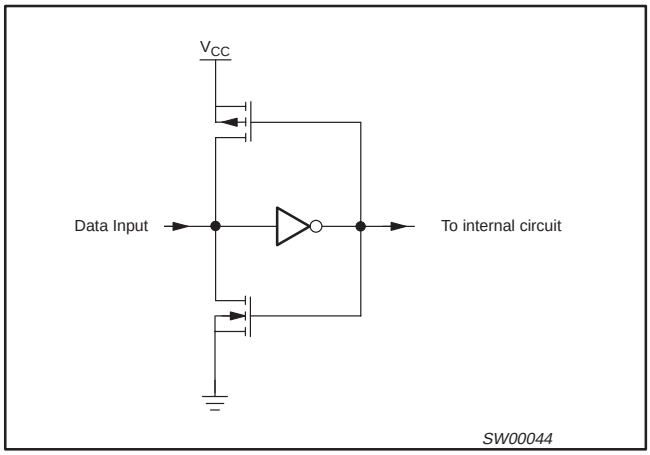


18-bit bus interface D-type latch (3-State) 74ALVCH16843

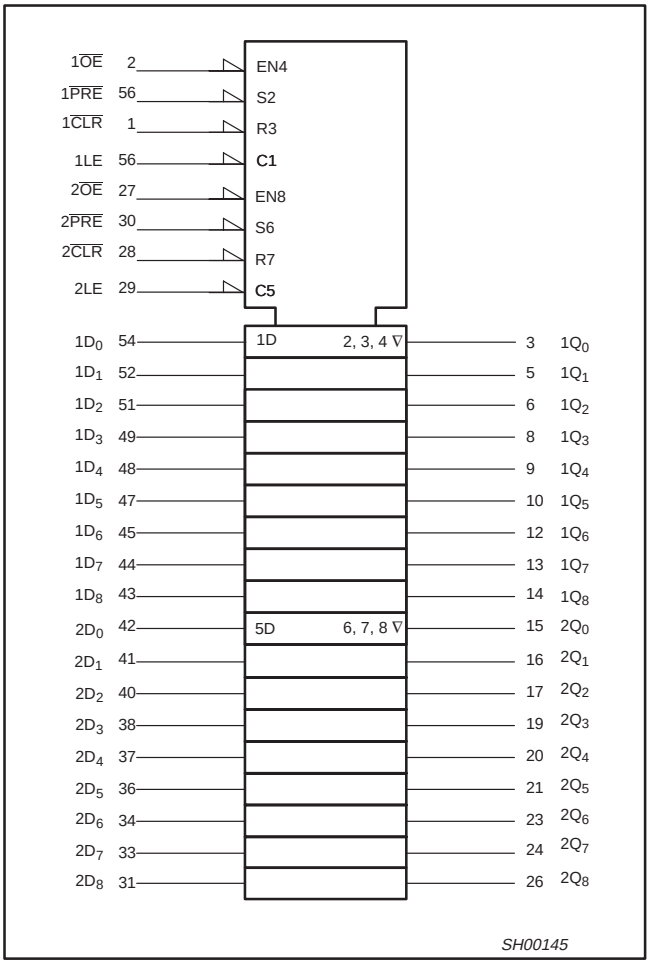
LOGIC DIAGRAM



BUS HOLD CIRCUIT



LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[2]	–0.5 to +4.6	V
		For data inputs[2]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; V_I = V_{CC} – 0.6V; I_O = 0		150	750	µA
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 3.6V	500			µA
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 3.6V	–500			µA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nDn to nQn	1, 6	1.0	2.2	4.3	ns
	Propagation delay nLE to nQn	2, 6	1.0	2.3	4.6	
	Propagation delay n$\overline{PRE}$ to nQn	1, 6	1.0	2.5	4.8	
	Propagation delay n$\overline{CLR}$ to nQn	1, 6	1.0	2.5	4.8	
t_{PZH}/t_{PZL}	3-State output enable time n$\overline{OE}$ to nQn	5, 6	1.0	2.8	5.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time n$\overline{OE}$ to nQn	5, 6	1.1	2.2	4.3	ns
t_{SU}	Set-up time nDn to nLE	3, 6	0.5	–0.1	–	ns
t_h	Hold time nDn to nLE	3, 6	0.9	0.5	–	ns
t_W	nLE pulse width HIGH	2, 6	1.5	0.5	–	ns
	n$\overline{PRE}$ pulse width LOW	4, 6	1.5	0.5	–	
	n$\overline{CLR}$ pulse width LOW	4, 6	1.5	0.5	–	
t_{REM}	Recovery time n$\overline{PRE}$ to nLE	4, 6	0.5	1.1	–	ns
	Recovery time n$\overline{CLR}$ to nLE	4, 6	0.5	1.0	–	

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nDn to nQn	1, 6	1.0	2.1	3.5	1.0	2.3	4.0	ns
	Propagation delay nLE to nQn	2, 6	1.0	2.0	3.5	1.0	2.1	3.9	
	Propagation delay n$\overline{PRE}$ to nQn	1, 6	1.0	2.2	3.8	1.0	2.6	4.5	
	Propagation delay n$\overline{CLR}$ to nQn	1, 6	1.0	2.3	3.9	1.0	2.5	4.3	
t_{PZH}/t_{PZL}	3-State output enable time n$\overline{OE}$ to nQn	5, 6	1.0	2.5	4.4	1.0	3.0	5.3	ns
t_{PHZ}/t_{PLZ}	3-State output disable time n$\overline{OE}$ to nQn	5, 6	1.3	2.6	4.0	1.3	2.8	4.4	ns
t_{SU}	Set-up time nDn to nLE	3, 6	0.5	0.0	–	0.5	–0.3	–	ns
t_h	Hold time nDn to nLE	3, 6	0.9	0.5	–	0.9	0.5	–	ns
t_W	nLE pulse width HIGH	2, 6	1.5	0.5	–	1.5	0.5	–	ns
	n$\overline{PRE}$ pulse width LOW	4, 6	1.5	0.5	–	1.5	0.6	–	
	n$\overline{CLR}$ pulse width LOW	4, 6	1.5	0.5	–	1.5	0.5	–	
t_{REM}	Recovery time n$\overline{PRE}$ to nLE	4, 6	1.0	0.4	–	0.8	–0.2	–	ns
	Recovery time n$\overline{CLR}$ to nLE	4, 6	0.8	0.2	–	0.6	–0.4	–	

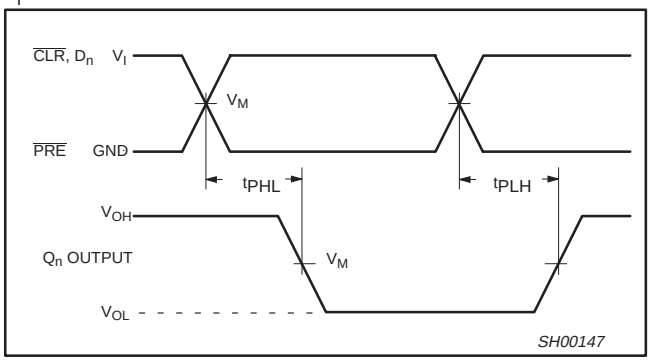
NOTES:
1. All typical values are measured T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

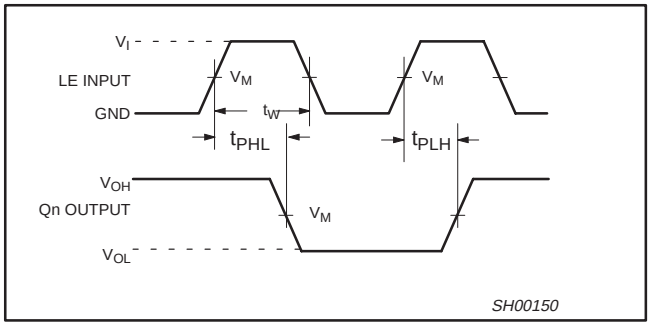
V_M = 0.5 V
$V_X = V_{OL}$ + 0.15V
$V_Y = V_{OH}$ –0.15V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

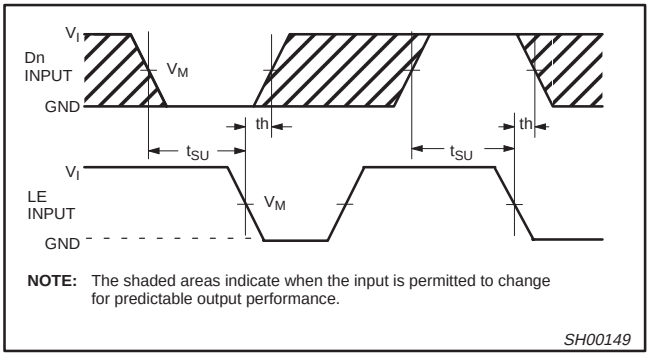
V_M = 1.5 V
$V_X = V_{OL}$ + 0.3V
$V_Y = V_{OH}$ –0.3V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7V



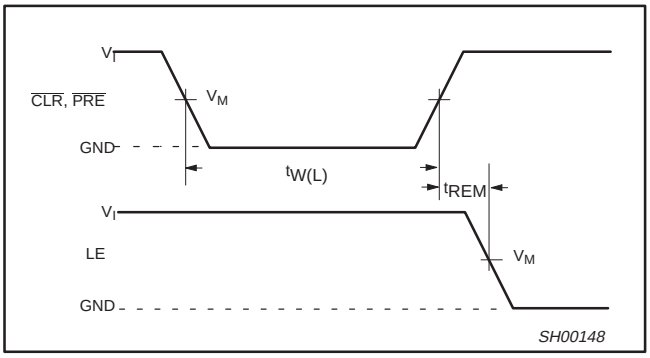
Waveform 1. Data input (Dn) to output (Qn), clear input ($\overline{CLR}$) to output (Qn) and preset input ($\overline{PRE}$) to output (Qn) propagation delay



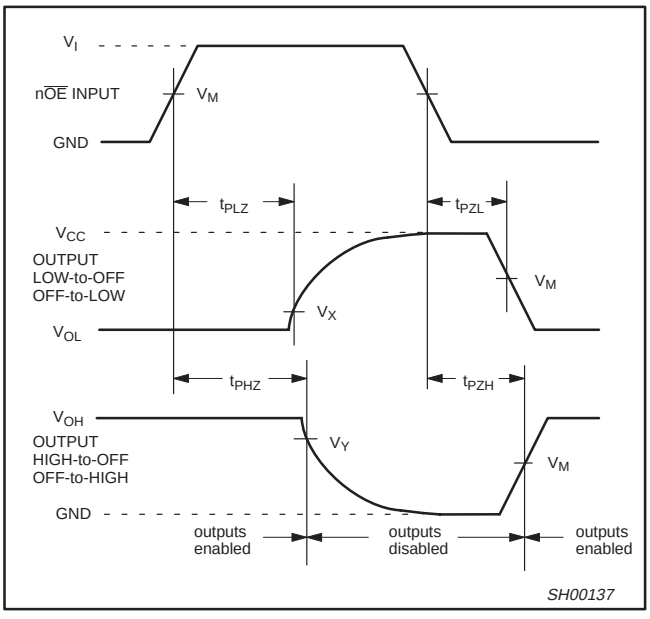
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delay



Waveform 3. Data set-up and hold times for the Dn input to the LE input

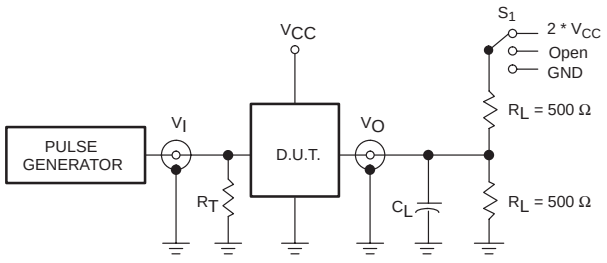


Waveform 4. Clear ($\overline{CLR}$) and preset ($\overline{PRE}$) pulse width, the clear ($\overline{CLR}$) and preset ($\overline{PRE}$) to latch (LE) removal time



Waveform 5. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

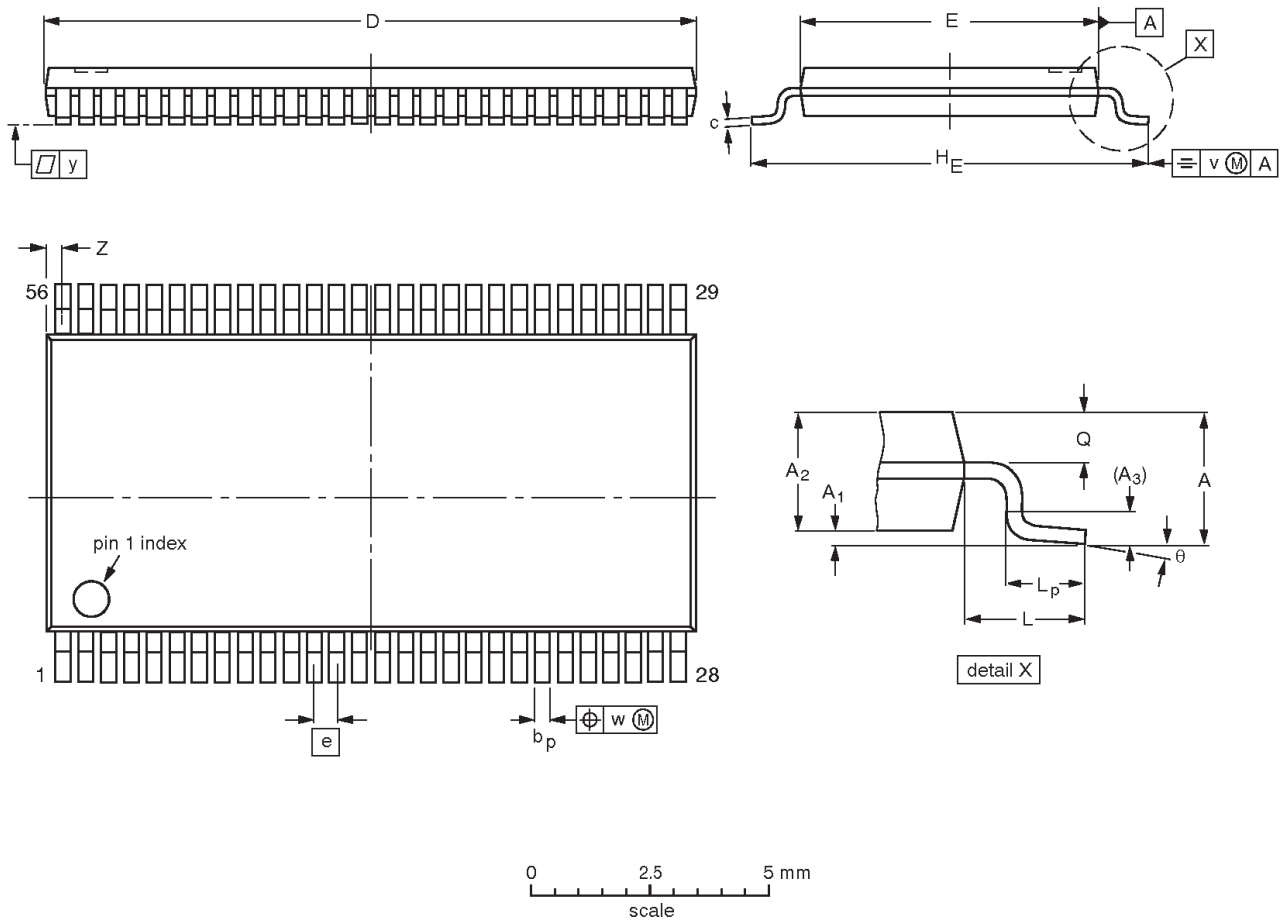
TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 6. Load circuitry for switching times

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153EE					~~93-02-03~~ 95-02-10

NOTES

18-bit bus interface D-type latch (3-State) 74ALVCH16843

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

print code Date of release: 07-98

Document order number: 9397-750-04562

Let's make things better.

Philips Semiconductors

PHILIPS