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NTE4094B & NTE4094BT
Integrated Circuit
CMOS, 8–Stage Shift/Storage Register

Description:

The NTE4094B (16–Lead DIP) and NTE4094BT (SOIC–16) are 8–stage shift registers with a data latch for each stage and a three–state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high–speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low–speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three–state buffers which are placed in the high–impedance state by a logic Low on Output Enable.

Features:

- Three–State Outputs
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial–to–Parallel Data Conversion
- Three–State Bus Compatible

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} + 0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55 to +125°C
Storage Temperature Range, T_{stg} . . . . . –65 to +150°C

Note 1. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation is is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	15	–	0.015	15	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on All Buffers Switching Note 3, Note 4)	I_T	5.0	I_T = (4.1µA/kHz) f + I_{DD}							µAdc
		10	I_T = (14µA/kHz) f + I_{DD}							µAdc
		15	I_T = (140µA/kHz) f + I_{DD}							µAdc
3−State Output Leakage Current	I_{TL}	18	–	±0.4	–	±0.00001	±0.4	–	±12	µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 1 \times 10^{-3}(C_L - 50)\, V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					
t_{TLH}, t_{THL} = (1.35ns/pf) C_L + 33ns		5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.6ns/pf) C_L + 20ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.4ns/pf) C_L + 20ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}					
Clock to Serial out QS						
t_{PHL}, t_{PLH} = (0.9ns/pf) C_L + 305ns		5.0	–	350	600	ns
t_{PHL}, t_{PLH} = (0.36ns/pf) C_L + 107ns		10	–	125	250	ns
t_{PHL}, t_{PLH} = (0.26ns/pf) C_L + 82ns		15	–	95	190	ns
Clock to Serial out Q'S						
t_{PHL}, t_{PLH} = (0.9ns/pf) C_L + 350ns		5.0	–	230	460	ns
t_{PHL}, t_{PLH} = (0.36ns/pf) C_L + 149ns		10	–	110	220	ns
t_{PHL}, t_{PLH} = (0.26ns/pf) C_L + 62ns		15	–	75	150	ns
Clock to Parallel out						
t_{PHL}, t_{PLH} = (0.9ns/pf) C_L + 375ns		5.0	–	420	840	ns
t_{PHL}, t_{PLH} = (0.36ns/pf) C_L + 177ns		10	–	195	390	ns
t_{PHL}, t_{PLH} = (0.26ns/pf) C_L + 122ns		15	–	135	270	ns
Strobe to Parallel out						
t_{PHL}, t_{PLH} = (0.9ns/pf) C_L + 245ns		5.0	–	290	580	ns
t_{PHL}, t_{PLH} = (0.36ns/pf) C_L + 127ns		10	–	145	290	ns
t_{PHL}, t_{PLH} = (0.26ns/pf) C_L + 87ns		15	–	100	200	ns
Output Enable to Output						
t_{PHZ}, t_{PZL} = (0.9ns/pf) C_L + 95ns		5.0	–	140	280	ns
t_{PHZ}, t_{PZL} = (0.36ns/pf) C_L + 57ns		10	–	75	150	ns
t_{PHZ}, t_{PZL} = (0.26ns/pf) C_L + 42ns		15	–	55	110	ns
t_{PLZ}, t_{PZH} = (0.9ns/pf) C_L + 180ns		5.0	–	225	450	ns
t_{PLZ}, t_{PZH} = (0.36ns/pf) C_L + 77ns		10	–	95	190	ns
t_{PLZ}, t_{PZH} = (0.26ns/pf) C_L + 57ns		15	–	70	140	ns
Setup Time, Data In to Clock	t_{su}	5.0	125	60	–	ns
		10	55	30	–	ns
		15	35	20	–	ns
Clock Pulse Width, High	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	ns
		15	83	40	–	ns
Clock Rise Time	$t_{r(cl)}$	5.0	15	–	–	µs
		10	5	–	–	µs
		15	5	–		µs
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.25	MHz
		10	–	5.0	2.5	MHz
		15	–	6.0	3.0	MHz
Strobe Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	80	40	–	ns
		15	70	35	–	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

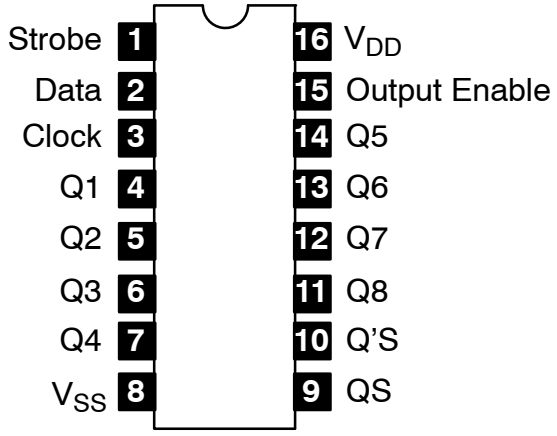
Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table:

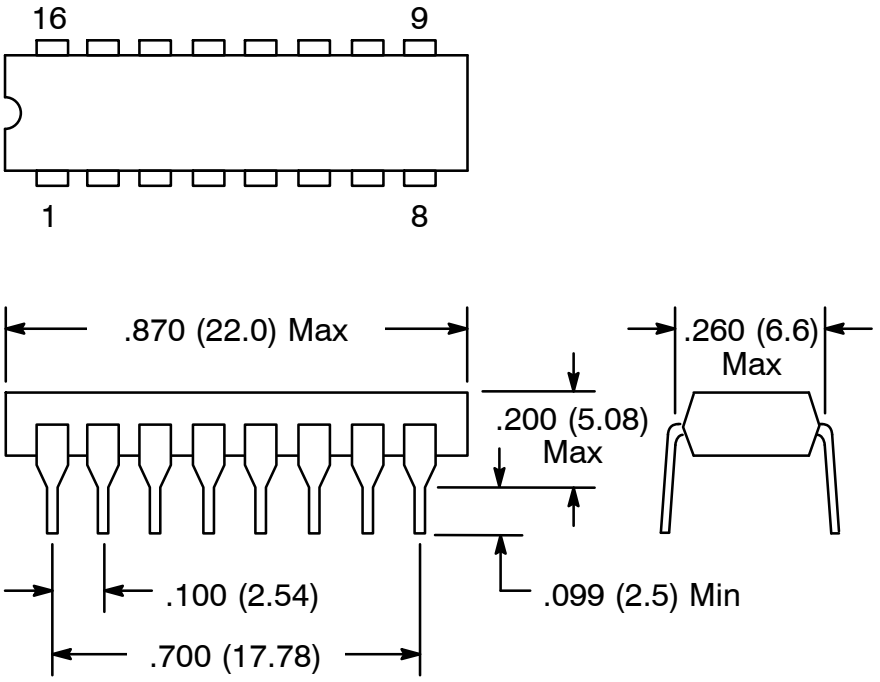
Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	QS *	Q'S
↗	0	X	X	Three–State	Three–State	Q7	No Change
↘	0	X	X	Three–State	Three–State	No Change	Q7
↗	1	0	X	No Change	No Change	Q7	No Change
↗	1	1	0	0	Q_N–1	Q7	No Change
↗	1	1	1	1	Q_N–1	Q7	No Change
↘	1	1	1	No Change	No Change	No Change	Q7

* At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and QS.
X = Don't Care

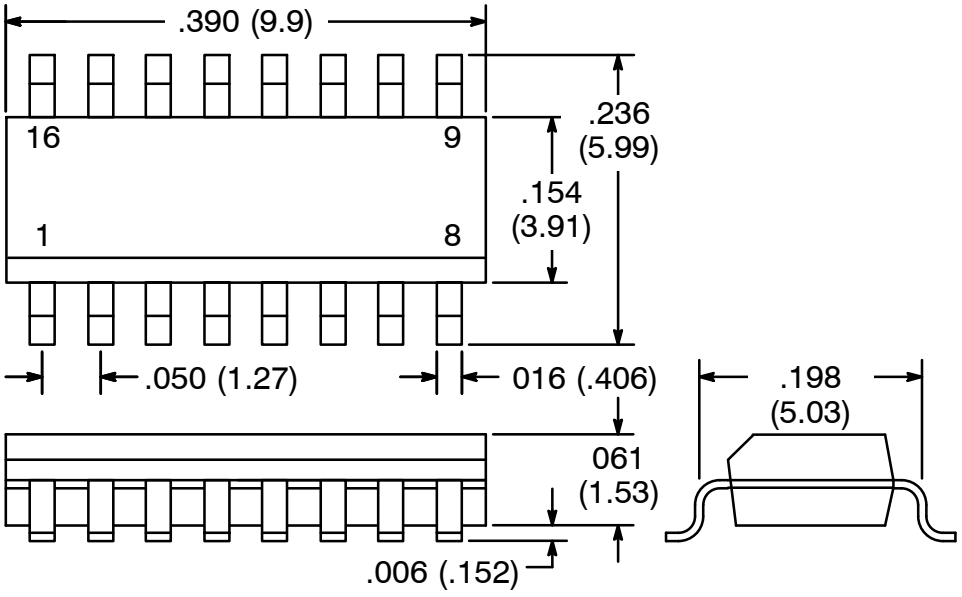
Pin Connection Diagram



NTE4094B



NTE4094BT



NOTE: Pin1 on Beveled Edge