# High Capacitance Piezo-sounder Driver with charge pump

## ■FEATURES

- ●Operating Voltage +2.0 to +5.5V
- ●Consumption Current (Active)
  $I_{DD11}$=3.5mA typ. (VDD=3V , $F_{IN}$=4kHz)
- ●Consumption Current (Shutdown)
  $I_{SD1}$=0.5µA max. (VDD=3V , IN=0V)
- ●High Capacitance Driving 30nF typ.
- ●Differential Output 30$V_{PP}$ max. (VDD=5V)
- ●Charge pump Circuit 3times
- ●Input Signal Detector & Auto Shutdown Control
- ●Operating Temperature -40 to +105°C
- ●Bi-CMOS Technology
- ●Package Outline EQFN16-G2, MSOP10(TVSP10)

## ■GENERAL DESCRIPTION

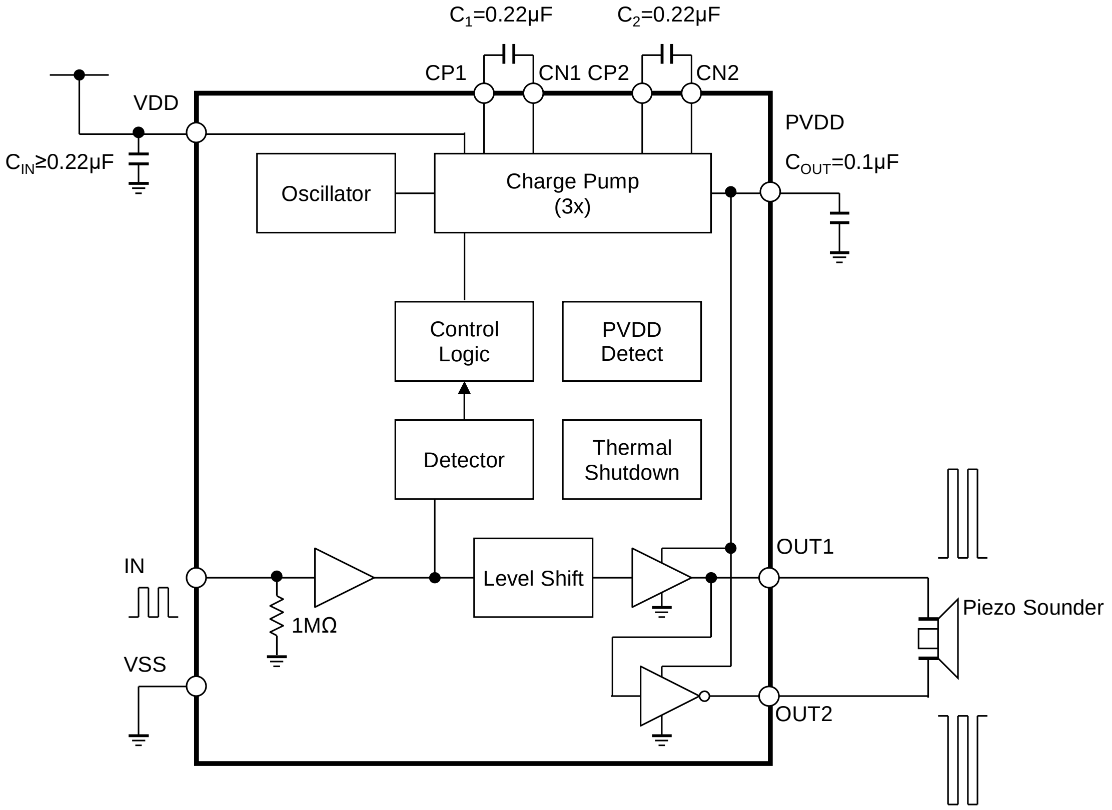
The NJW1280 is a switching driver with charge pump for high capacitance piezo-sounder. It can drive outputs up to 30$V_{PP}$ from 5V supply.

Because the NJW1280 has the shutdown function, it is suitable for the battery application.

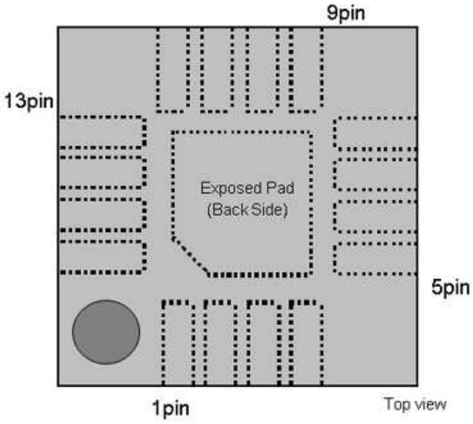
## ■APPLICATION

- ●Fire Alarm
- ●Smoke Detector
- ●Security Alarm

## ■APPLICATION CIRCUIT



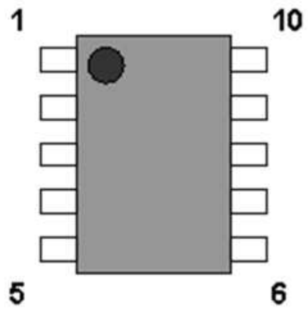
■PIN CONFIGURATION (EQFN16-G2)




| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | N.C. | - |
| 2 | IN | Input Terminal |
| 3 | N.C. | - |
| 4 | N.C. | - |
| 5 | OUT1 | Output Terminal 1 |
| 6 | OUT2 | Output Terminal 2 |
| 7 | VSS | VSS Terminal |
| 8 | CN1 | Capacitor Connection Terminal |
| 9 | N.C. | - |
| 10 | CN2 | Capacitor Connection Terminal |
| 11 | N.C. | - |
| 12 | CP1 | Capacitor Connection Terminal |
| 13 | PVDD | Charge Pump Output Terminal |
| 14 | CP2 | Capacitor Connection Terminal |
| 15 | VDD | Power Supply Terminal(Connect to 16pin) |
| 16 | VDD | Power Supply Terminal |

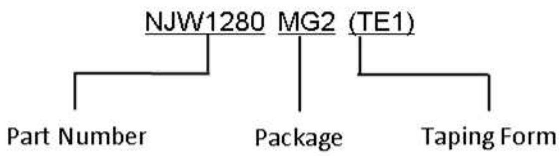
Exposed Pad:
Connect the Exposed Pad on land of float, or GND.

■PIN CONFIGURATION (MSOP10(TVSP10))




| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | CP1 | Capacitor Connection Terminal |
| 2 | PVDD | Charge Pump Output Terminal |
| 3 | CP2 | Capacitor Connection Terminal |
| 4 | VDD | Power Supply Terminal |
| 5 | IN | Input Terminal |
| 6 | OUT1 | Output Terminal 1 |
| 7 | OUT2 | Output Terminal 2 |
| 8 | VSS | VSS Terminal |
| 9 | CN1 | Capacitor Connection Terminal |
| 10 | CN2 | Capacitor Connection Terminal |

■MARK INFORMATION




■ORDERING INFORMATION

| PART NUMBER | PACKAGE OUTLINE | RoHS | HALOGEN-FREE | TERMINAL FINISH | MARKING | WEIGHT (mg) | MOQ(pcs) |
|---|---|---|---|---|---|---|---|
| NJW1280MG2 | EQFN16-G2 | Yes | Yes | Sn-2Bi | 1280 | 6.5 | 3,000 |
| NJW1280RB2 | MSOP10(TVSP10) | Yes | Yes | Sn-2Bi | 1280 | 19 | 2,000 |

## ■ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 6.0 | V |
| Maximum Input Voltage | $V_{IN}$ | -0.3 to $V_{DD}$ + 0.3 | V |
| Power Dissipation (Ta=25˚C)<br>EQFN16-G2<br>MSOP10(TVSP10) | $P_D$ | 2layer/4layer<br>520(1)/1400(2)<br>520(3)/730(4) | mW |
| Storage Temperature Range | $T_{stg}$ | -40 to +150 | °C |

## ■THERMAL CHARACTERISTICS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Junction-to-ambient thermal resistance<br>EQFN16-G2<br>MSOP10(TVSP10) | θja | 2layer/4layer<br>239.4(1)/89.8(2)<br>240.3(3)/171.6(4) | °C /W |

(1) Mounted on glass epoxy board(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(2) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

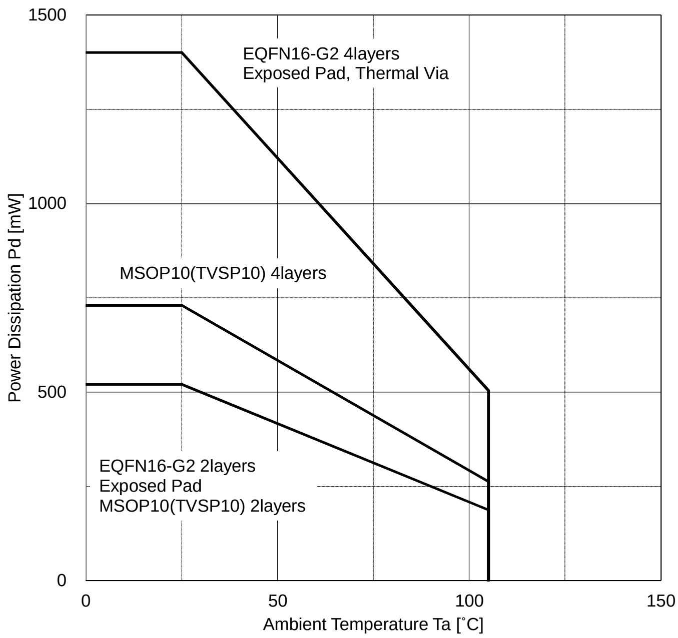
(3) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(4) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers), internal Cu area: 74.2x74.2mm

## ■RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Operating Voltage Range | $V_{DD}$ | +2.0 to +5.5 | V |
| Operating Temperature Range | $T_{opr}$ | -40 to +105 | °C |

## ■POWER DISSIPATION vs. AMBIENT TEMPERATURE



## ■ELECTRICAL CHARACTERISTICS

($Ta=25^{o}C$, VDD=3V, $C_1=C_2$=220nF, $C_{OUT}$=100nF, $C_{PIEZO}$=30nF, $F_{IN}$=4kHz unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Charge Pump Output Voltage 1 | $V_{PVDD1}$ | PVDD terminal ($C_{PIEZO}$=No Load $I_{MPVDD}$=-9mA) *1) | 8 | - | 9 | V |
| Charge Pump Output Voltage 2 | $V_{PVDD2}$ | PVDD terminal VDD=5V ($C_{PIEZO}$=No Load $I_{MPVDD}$=-15mA) *1) | 13.5 | - | 15 | V |
| Piezo Driver Output Voltage 1 | $V_{OUT1}$ | Differential Output (OUT1,OUT2) | 16.2 | 18 | - | $V_{PP}$ |
| Piezo Driver Output Voltage 2 | $V_{OUT2}$ | Differential Output(OUT1,OUT2) VDD=5V | 27 | 30 | - | $V_{PP}$ |
| Operating Current 11 | $I_{DD11}$ | $C_{PIEZO}$=No Load | - | 3.5 | 7 | mA |
| Operating Current 12 | $I_{DD12}$ | $C_{PIEZO}$=No Load, VDD=5V | - | 4.5 | 9 | mA |
| Operating Current 21 | $I_{DD21}$ | Differential application | - | 16.5 | - | mA |
| Operating Current 22 | $I_{DD22}$ | Differential application, VDD=5V | - | 27.5 | - | mA |
| Shutdown Current1 | $I_{SD1}$ | IN=0V*2) | - | - | 0.5 | µA |
| Shutdown Current2 | $I_{SD2}$ | IN=0V,VDD=5V | - | - | 1.0 | µA |
| Input Signal Frequency Range | $F_{IN}$ | Waveform=Rectangular Pulse | 0.2 | 4 | 6 | kHz |
| Internal Switching Frequency | $F_{OSC}$ | | 0.3 | 0.6 | 1.2 | MHz |
| Turn-On Time | $T_{ON}$ | From IN signal High to the OUT1 signal high | - | 2 | 4 | ms |
| Shutdown Delay Time | $T_{OFF}$ | DIN=H->L to PVDD OFF | 6 | 15 | 30 | ms |
| Output Wave Rise Time | $T_R$ | OUT1, OUT2, 10% to 90% | - | 16 | - | µs |
| Output Wave Fall Time | $T_F$ | OUT1, OUT2, 90% to 10% | - | 10 | - | µs |

*1) It does not guarantee the use of any method other than the use of the application circuit.

*2) IN has been low at least $T_{OFF(max.)}$.

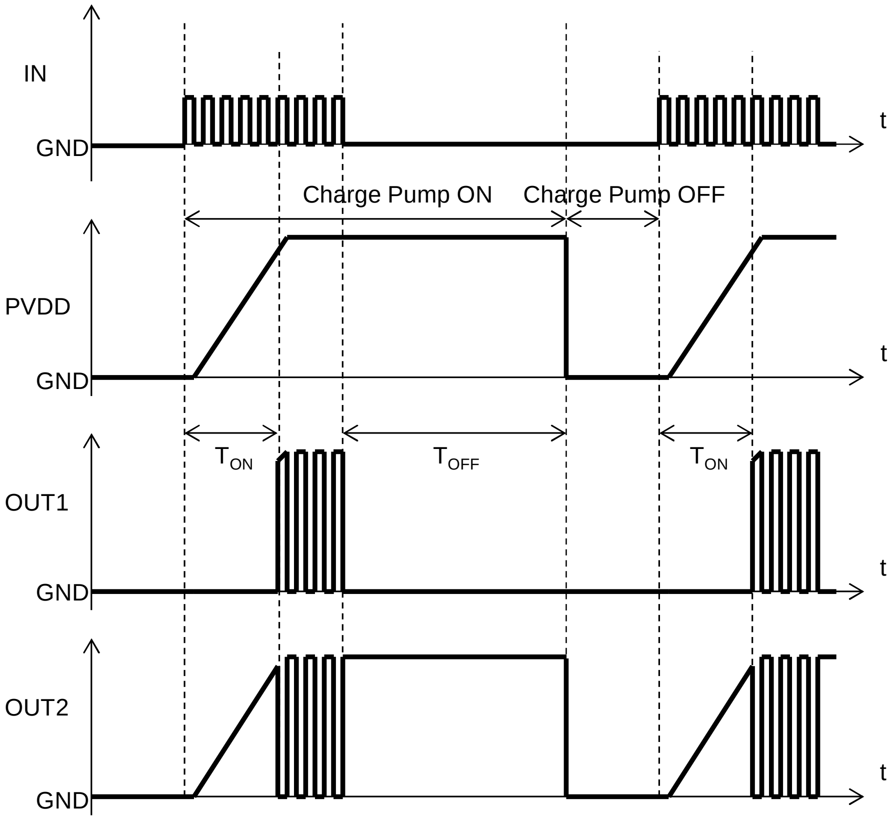
## ■INPUT TERMINAL CHARACTERISTICS

(Ta=25°C, VDD=3V, unless otherwise specified)

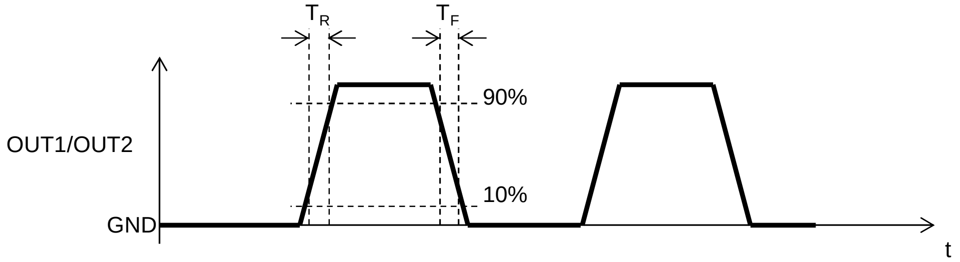
| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| High Level Input Voltage 1 | $V_{IH1}$ | IN terminal | 1.6 | - | VDD | V |
| Low Level Input Voltage 1 | $V_{IL1}$ | IN terminal | 0 | - | 0.4 | V |
| High Level Input Current | $I_{IH}$ | IN terminal IN=3V | - | 3 | 4 | μA |
| Low Level Input Current | $I_{IL}$ | IN terminal IN=0V | - | - | 1 | μA |

■**Timing Chart**

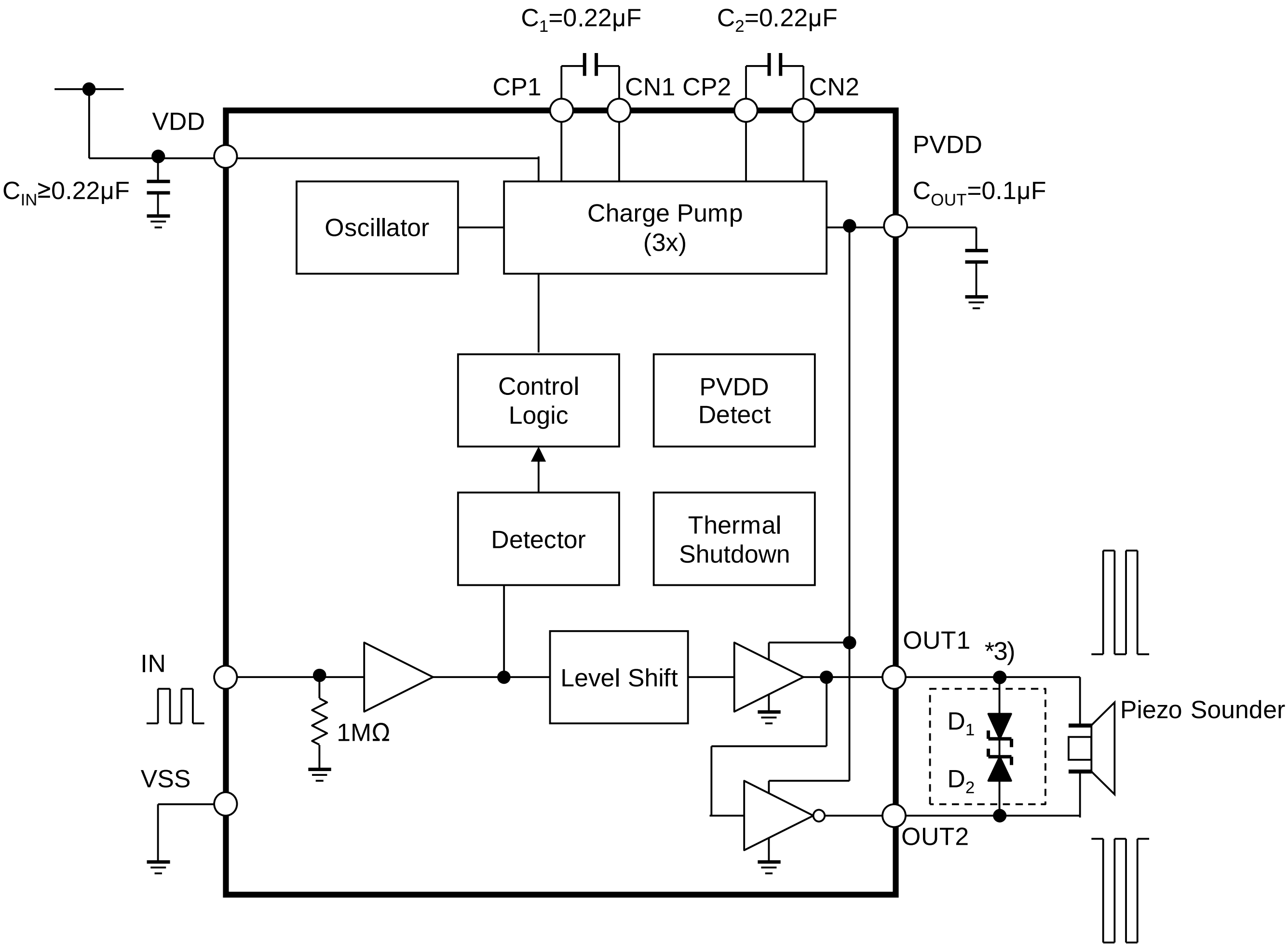
$T_{ON}/T_{OFF}$




$T_R/T_F$



■**Application Circuit**

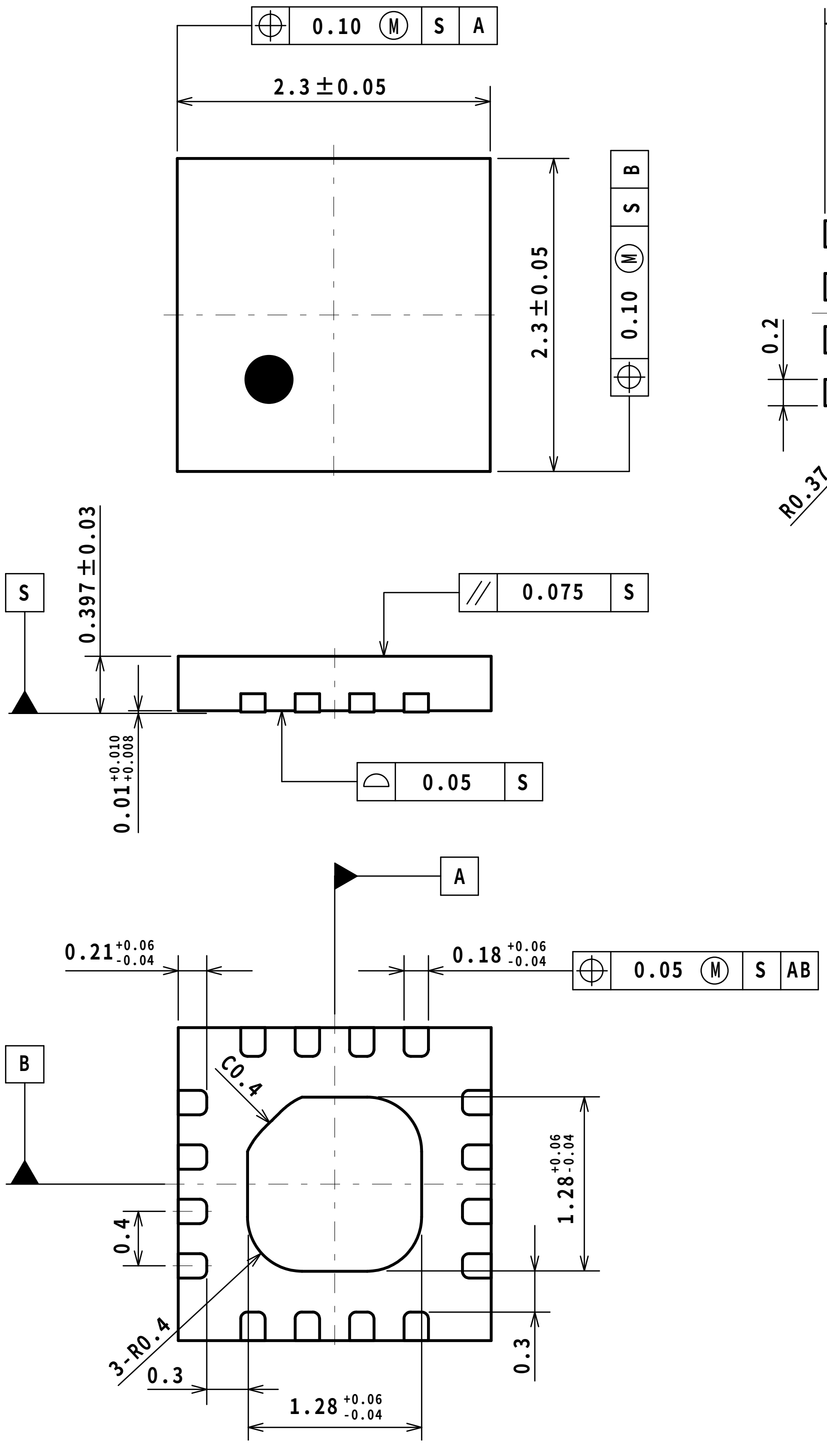



*3) Please do not drop the product or apply shock or temperature change to it. If so, the LSI might be destroyed by the charge (surge voltage) generated. Above figure shows an example driving circuit using Zener diode.
The guideline for Zener voltage is VDD x3 <$V_Z$<20V.

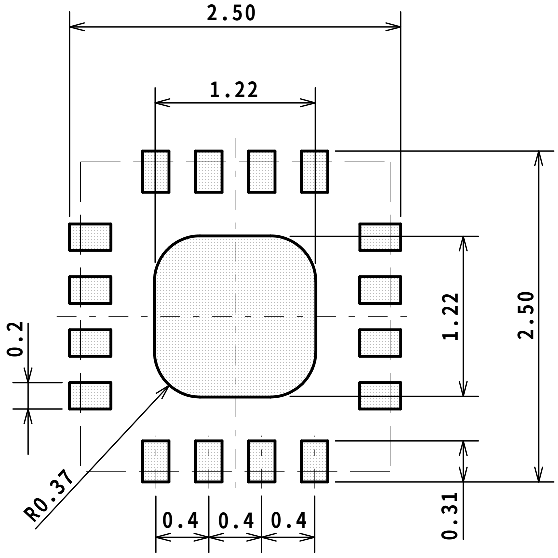
## EQFN16-G2

Unit: mm

■PACKAGE DIMENSIONS



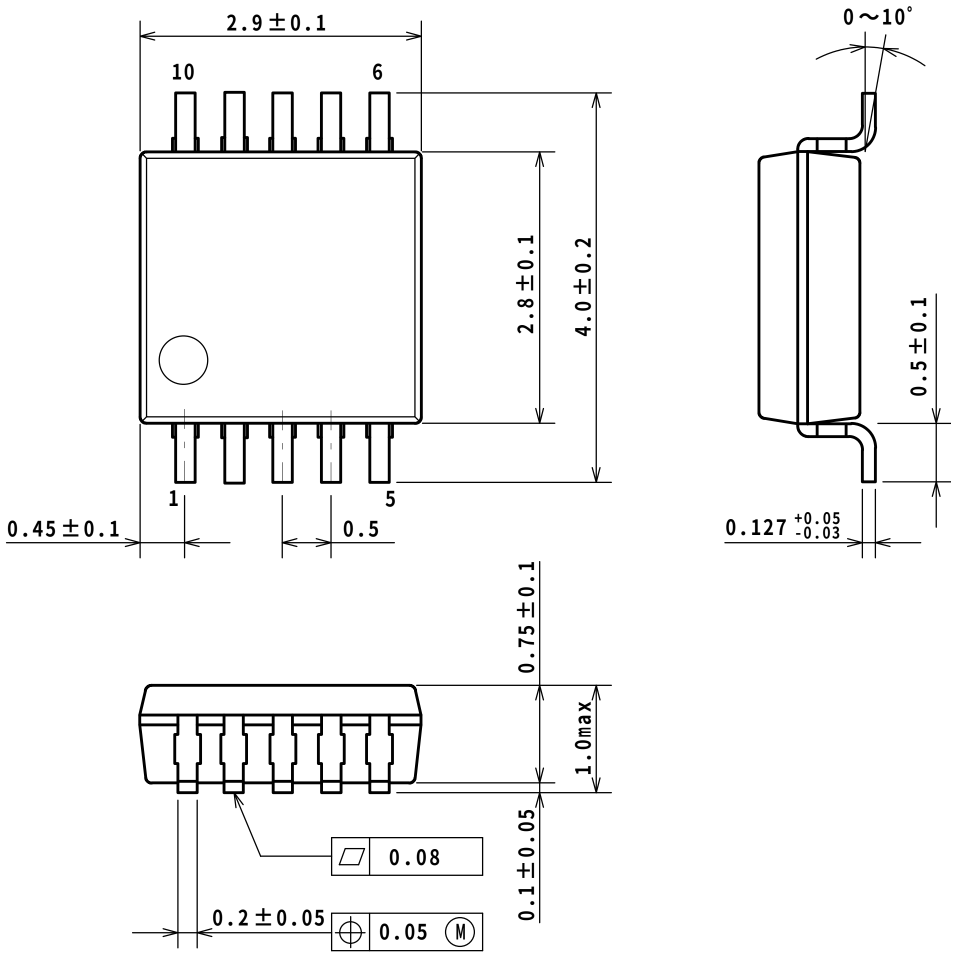

■EXAMPLE OF SOLDER PADS DIMENSIONS



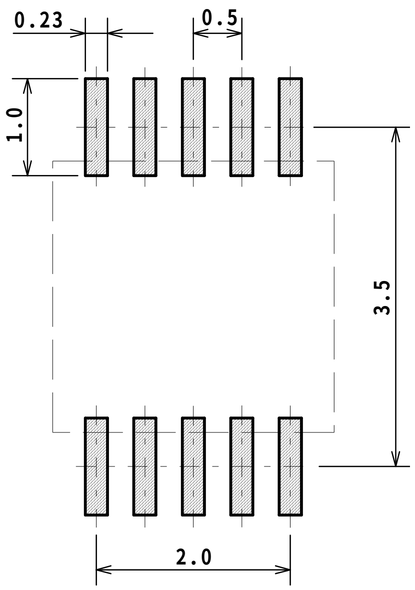
# MSOP10 JEDEC MO-187-DA/THIN TYPE

Unit: mm

## ■PACKAGE DIMENSIONS




## ■EXAMPLE OF SOLDER PADS DIMENSIONS

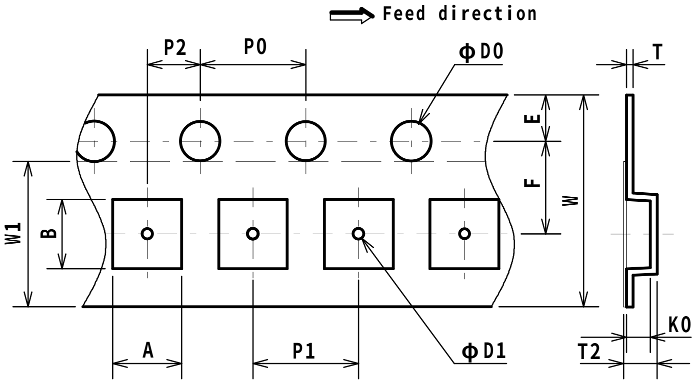


## EQFN16-G2

Unit: mm

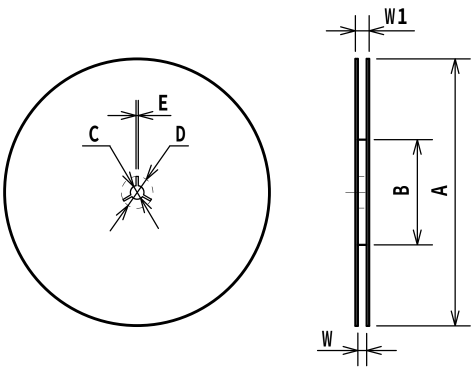
## ■PACKING SPEC

### TAPING DIMENSIONS



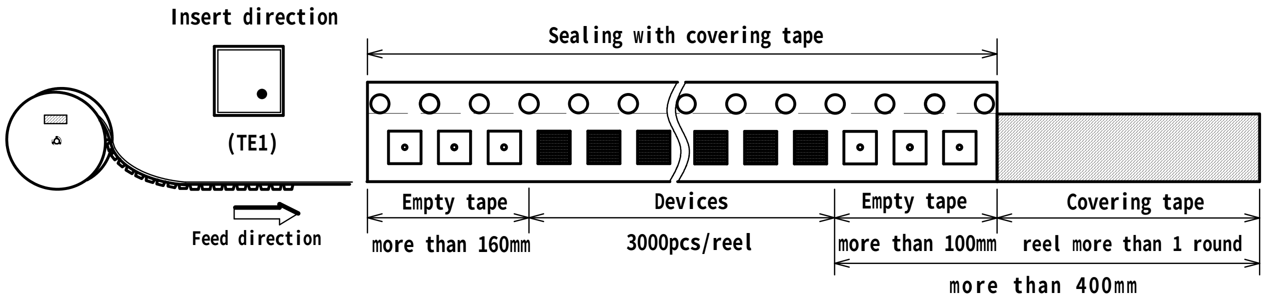

| SYMBOL | DIMENSION | REMARKS |
|---|---|---|
| A | 2.55±0.05 | BOTTOM DIMENSION |
| B | 2.55±0.05 | BOTTOM DIMENSION |
| D0 | $1.5^{+0.1}_{0}$ | |
| D1 | 0.5±0.1 | |
| E | 1.75±0.1 | |
| F | 3.5±0.05 | |
| P0 | 4.0±0.1 | |
| P1 | 4.0±0.1 | |
| P2 | 2.0±0.05 | |
| T | 0.25±0.05 | |
| T2 | 1.00±0.07 | |
| K0 | 0.65±0.05 | |
| W | 8.0±0.2 | |
| W1 | 5.5 | THICKNESS 0.1max |

### REEL DIMENSIONS

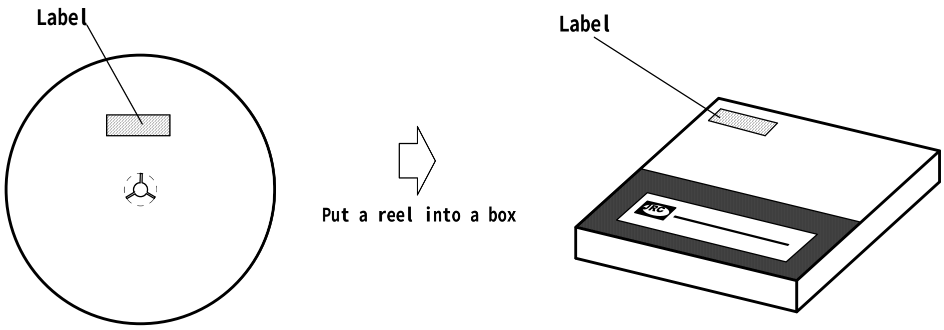



| SYMBOL | DIMENSION |
|---|---|
| A | $\phi 180^{0}_{-1.5}$ |
| B | $\phi 60^{+1}_{0}$ |
| C | φ 13±0.2 |
| D | φ 21±0.8 |
| E | 2±0.5 |
| W | $9^{+0.3}_{0}$ |
| W1 | 1.2 |

### TAPING STATE




### PACKING STATE



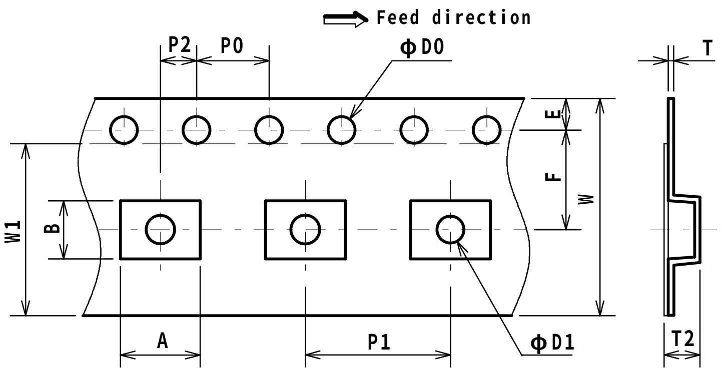

UNIT : mm

## MSOP10 MEET JEDEC MO-187-DA/THIN TYPE

■PACKING SPEC

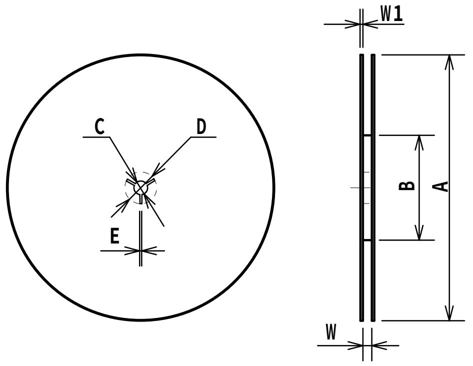
Unit: mm

### TAPING DIMENSIONS



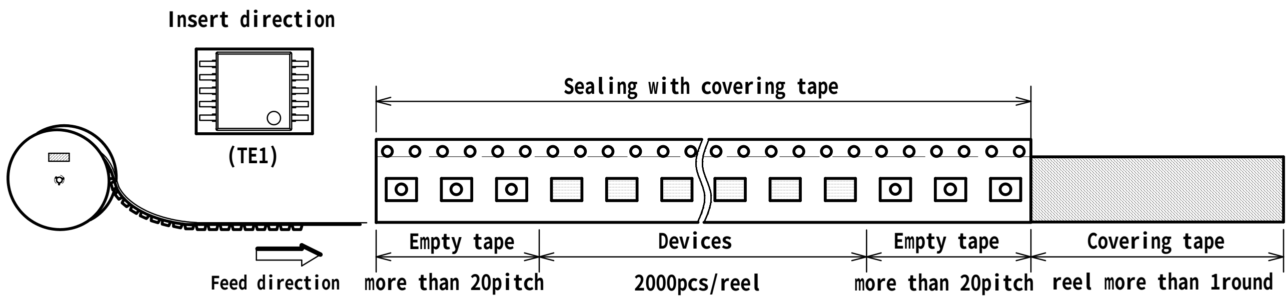

| SYMBOL | DIMENSION | REMARKS |
|---|---|---|
| A | 4.4 | BOTTOM DIMENSION |
| B | 3.2 | BOTTOM DIMENSION |
| D0 | $1.5^{+0.1}_{0}$ | |
| D1 | $1.5^{+0.1}_{0}$ | |
| E | 1.75±0.1 | |
| F | 5.5±0.05 | |
| P0 | 4.0±0.1 | |
| P1 | 8.0±0.1 | |
| P2 | 2.0±0.05 | |
| T | 0.3±0.05 | |
| T2 | 1.75 (MAX.) | |
| W | 12.0±0.3 | |
| W1 | 9.5 | THICKNESS 0.1max |

### REEL DIMENSIONS

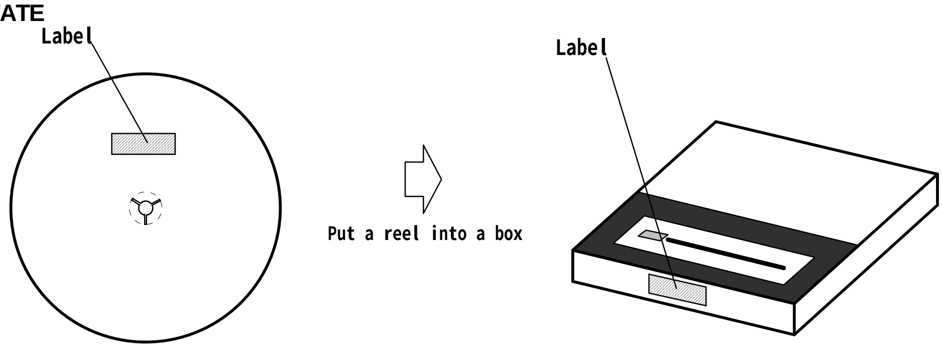



| SYMBOL | DIMENSION |
|---|---|
| A | φ254±2 |
| B | φ100±1 |
| C | φ 13±0.2 |
| D | φ 21±0.8 |
| E | 2±0.5 |
| W | 13.5±0.5 |
| W1 | 2.0±0.2 |

### TAPING STATE

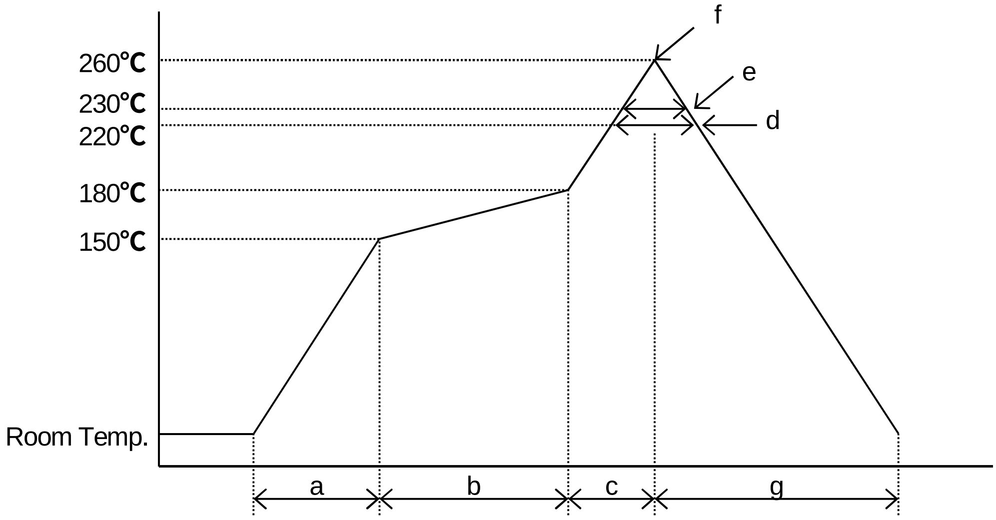



### PACKING STATE



**■RECOMMENDED MOUNTING METHOD**

∗Recommended reflow soldering procedure




| | |
|---|---|
| a: Temperature ramping rate | : 1 to 4°C/s |
| b: Pre-heating temperature | : 150 to 180°C |
| time | : 60 to 120s |
| c: Temperature ramp rate | : 1 to 4°C/s |
| d: 220°C or higher time | : Shorter than 60s |
| e: 230°C or higher time | : Shorter than 40s |
| f: Peak temperature | : Lower than 260°C |
| g: Temperature ramping rate | : 1 to 6°C/s |

The temperature indicates at the surface of mold package.

## ■PRECAUTIONS FOR USE OF PIEZO SOUNDER DRIVER IC

1. Power Supply

Use a stable power supply to operate the IC stably. Furthermore, please design so that unexpected abnormal overcurrent does not flow more than necessary to prevent the IC breakdown and the spread of the effects.

2. Inductive Load

If your design includes an inductive load, the IC malfunction or breakdown caused by the current resulting from the inrush current at ON or the current resulting from the back electromotive force at OFF. Incorporate a protection circuit into the design to prevent these. The IC breakdown may cause smoke or ignition.

3. External parts

Carefully select external parts (such as power supply decoupling capacitor, charge pimp flying capacitor and charge pump store capacitor), load components (such as a piezo-sounder) taking into consideration absolute maximum ratings, characteristics variation by temperature and leakage current characteristics.

4. Auxiliary functions

The Piezo-sounder Driver IC have the auxiliary functions which suppress breaking themselves under unexpected abnormal conditions. These auxiliary functions are not guarantee as they operate over absolute maximum ratings. It is essential to design as the auxiliary functions do not operate. Do not design depending on the auxiliary functions.

4.1 Thermal shutdown circuit

The thermal shutdown circuit is a suspension circuit of IC's operation to prevent the junction temperature endlessly increase under unexpected abnormal conditions. The IC will return to operate under normal junction temperature.

The thermal shutdown function is not guarantee as it operates over temperature of absolute maximum ratings. Depending on the method of use and usage conditions may cause the thermal shutdown circuit to not operate properly or the IC breakdown before operation.

4.2 Current Limit Circuit

The current limit circuit limits output current to below a constant value to prevent output current endlessly increase under unexpected abnormal conditions.

Depending on the method of use and usage conditions such as exceeding absolute maximum ratings may cause the current limit circuit to not operate properly or the IC breakdown before operation.

## ■APPLICATION NOTE

The NJW1280 is a switching driver with 3times charge pump for piezo-sounder. It can drive outputs up to $30V_{PP}$ from 5V supply. The NJW1280 has the shutdown function, it is suitable for the battery application.

### 1. Operating Principle

The NJW1280 has the built-in Oscillator, Charge Pump, Control Logic, Detector, Level Shift, Low PVDD Detect, and Thermal Shut Down.(Fig.1)

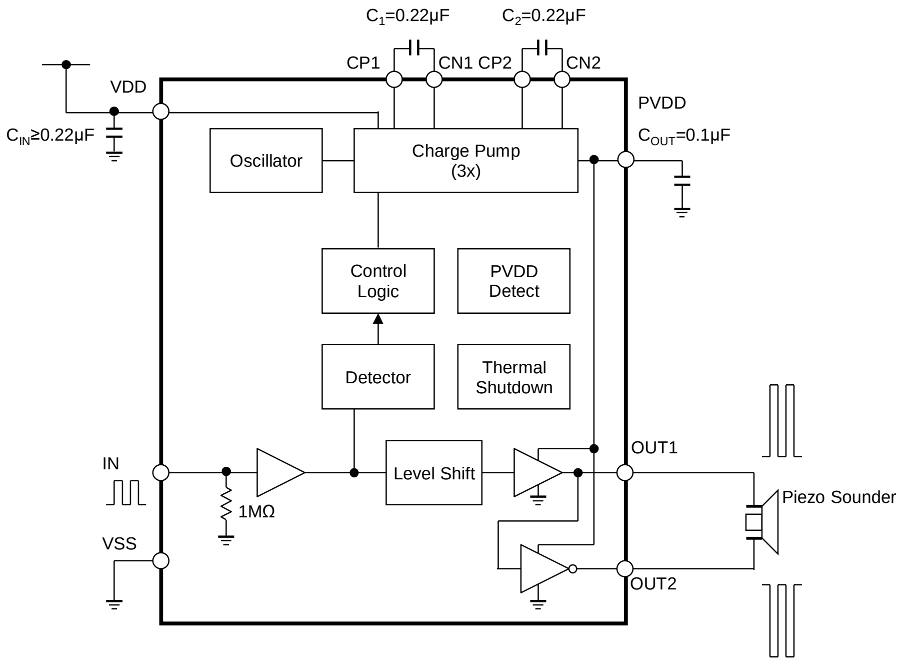



**Fig.1 NJW1280 Function Block Diagram and application circuit**

### 2. External Parts

#### 2-1. Parts List

Table 1 is external parts list of application circuit.

**Table 1 List of External Parts**

| Part No. | Quantity | Value | Description | Use in application |
|---|---|---|---|---|
| $C_1$,$C_2$ | 2 | 0.22μF | X7R ceramic capacitor | Charge pump flying capacitor |
| $C_{OUT}$ | 1 | 0.1μF | X7R ceramic capacitor | Charge pump store capacitor |
| $C_{IN}$ | 1 | ≥0.22μF* | X7R ceramic capacitor | Power supply decoupling |

*Please decide after evaluation by application.

#### 2-2. Flying capacitor(C1, C2)

C1, C2 are flying capacitors that carry charges in the charge pump circuit. Use capacitors with a low-ESR(ex. ceramic capacitors) and good temperature characteristics, and place them as closed to the IC as possible to minimize wring resistance, capacitance, and inductance(Fig. 2)


**Fig 2 Flying Capacitor**

### 2-3. Store capacitor($C_{OUT}$)

Use capacitors with a low-ESR(ex. ceramic capacitors) and good temperature characteristics, and place them as closed to the IC as possible to minimize wring resistance, capacitance, and inductance(Fig. 3)

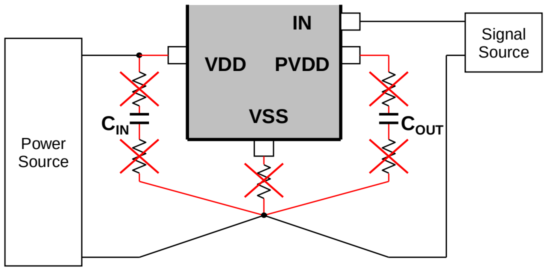



**Fig 3 Store capacitor, Coupling Capacitor**

### 2-4. Coupling capacitor of power supply

It stabilizes the VDD line. Please decide the capacity according to your system. Use capacitors with low ESR(ex. ceramic capacitors) and good temperature characteristics, and place them as close to the IC as possible to minimize wiring resistance, capacitance, and inductance. (Fig. 3) Also, connecting an electrolytic capacitor with large capacitance in parallel will make the operation of the NJW 1280 more stable.

## 3. Operation

By inputting the signal to the IN terminal, the NJW 1280 starts its operation and enters the active state. When it detects that no signal is being input, it stops and enters the shutdown state.

### 3-1. Operation sequence

NJW 1280 detects the presence or absence of an input signal and starts and stops it.

### 3-2. Stop condition

Fig. 4 shows the sequence from operation start to stop. When the NJW 1280 detects the rise of the input voltage, it starts up in the soft start state (a). No signal is output during the soft start period. When the NJW 1280 detects the rising edge of the input signal after the $T_{ON}$ period, the soft start ends and a signal is output (b). After the $T_{OFF}$ period has elapsed while the input signal is low, the IC enters the shutdown state.

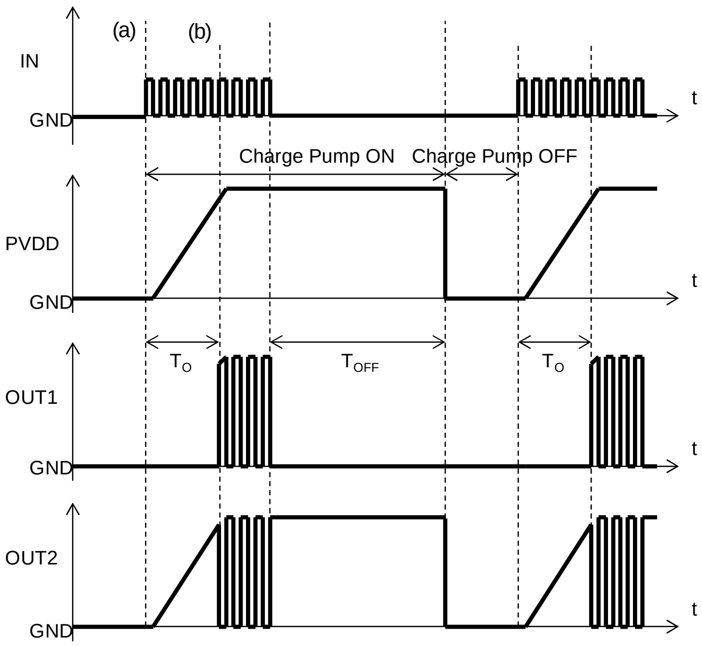



**Fig4 Sequence from operation to stop**

When inputting an intermittent signal, the period of no signal may exceed $T_{OFF}$. When the IC enters the shutdown state, no signal is output during the $T_{ON}$ period when the signal is input again, so the head of the output signal will be missing. In this case, as shown in Fig. 5, if the input signal is held at the H level in the no signal period, the NJW 1280 does not count the $T_{OFF}$ period and does not enter the shutdown state.

However, when supplying DC voltage to the piezoelectric sounder, there is a possibility that it will have some effect on the piezoelectric sounder. Therefore, if you can think of a way of supplying DC voltage, please check with the piezoelectric sounder manufacturer you use.

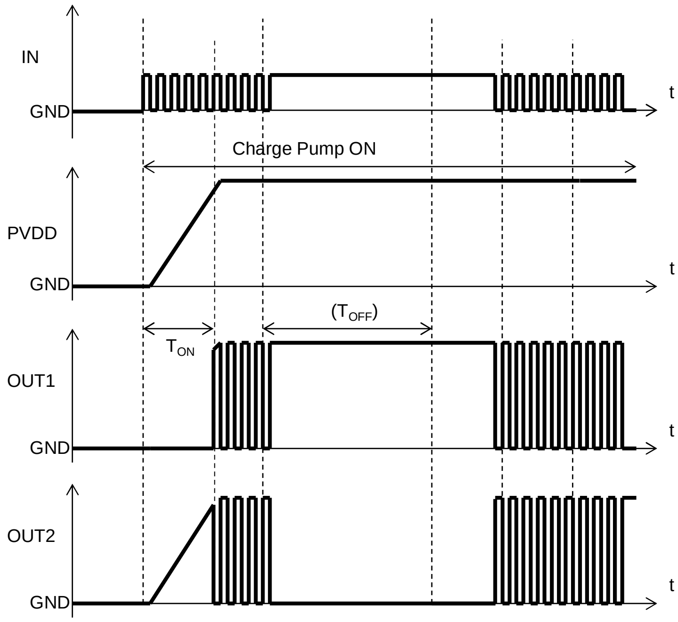



**Fig 5 Output countermeasure sequence**

### 3-3. TSD function

The thermal shutdown function stops the charge pump circuit and output circuit when the junction temperature $T_J$ of the NJW 1280 exceeds Tstg and becomes the certain temperature $T_{TSD1}$ as shown in Fig. 6. When $T_J$ drops the certain temperature $T_{TSD2}$ below, the NJW1280 starts operation from the soft sequence state again. Fig. 6 (a) shows the case where the TSD function is ON while inputting the signal, and (b) show the case where the input signal stops while the TSD function is ON and it goes L level. In the latter case, the NJW1280 enters the shutdown state after the $T_{OFF}$ period after the start in the soft start state after the TSD function turns off.

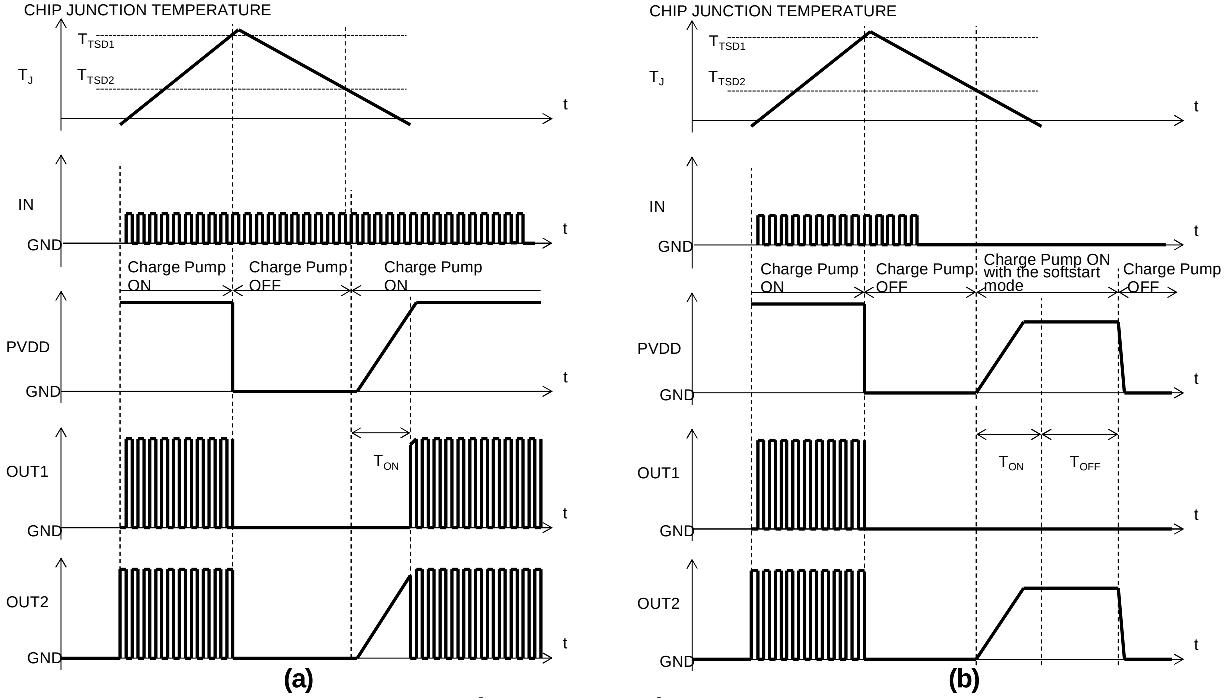



**Fig 6 TSD operation sequence**

The TSD function is not guaranteed because it exceeds the maximum rating. It is an auxiliary function to the last. Please make a redundant design that the TSD does not work. Do not perform set design using this function.

### 3-4. PVDDdet operation sequence

The PVDDdet function resets the IC when the PVDD pin voltage falls below the voltage $V_{DET} \approx 1.5 \times V_{DD}$ for some reason. This function does not function during the soft start period. Detection voltage depends on $V_{DD}$ voltage.

The operation is shown in Fig. 7. If the PVDD voltage falls below $V_{DET}$ while the NJW1280 is operating, the NJW1280 is reset and the shutdown state is entered and the charge pump circuit and output circuit stop (a). When the input signal rises in this state, the IC starts operation (b), but when the PVDDdet function starts to function after the soft start period $T_{ON}$, it will be shut down again (c).
This situation continues until the cause of lowering the voltage of the PVDD terminal is eliminated.

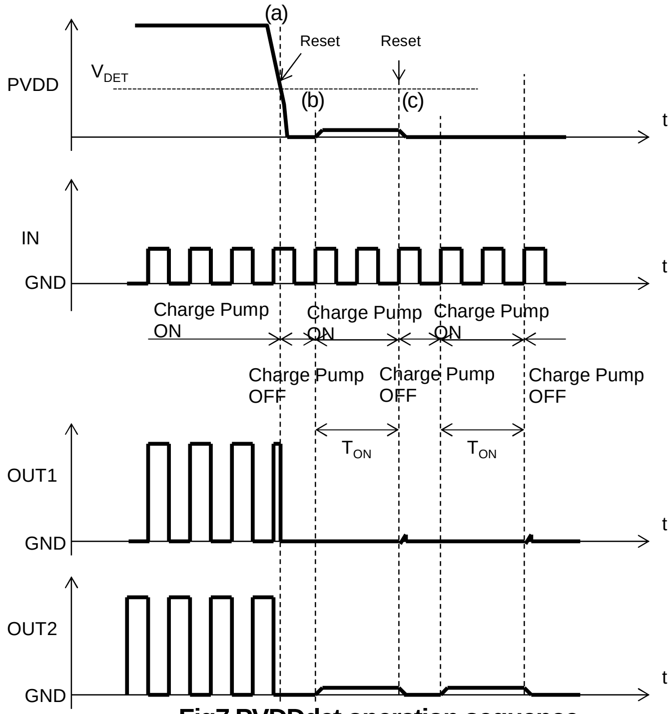



**Fig7 PVDDdet operation sequence**

This function is an auxiliary function. Please make safety design so that this function does not work.
Also, do not do set design using this function.

**4. Surge voltage from piezo-souder**

Please do not drop the product or apply shock or temperature change to it. If so, the LSI might be destroyed by the charge (surge voltage) generated. Above Fig. 8 shows an example driving circuit using zener diode.
The guideline for Zener voltage is VDD x3 <$V_Z$<20V.

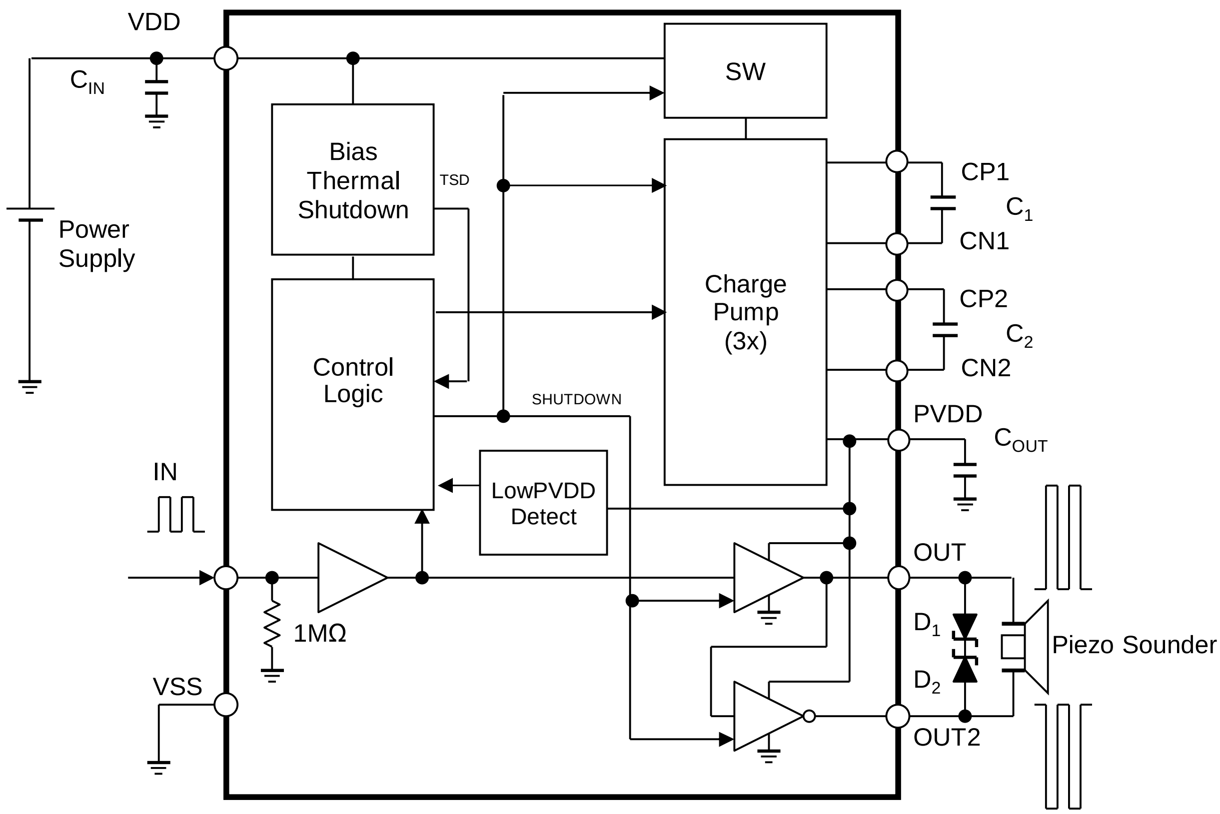
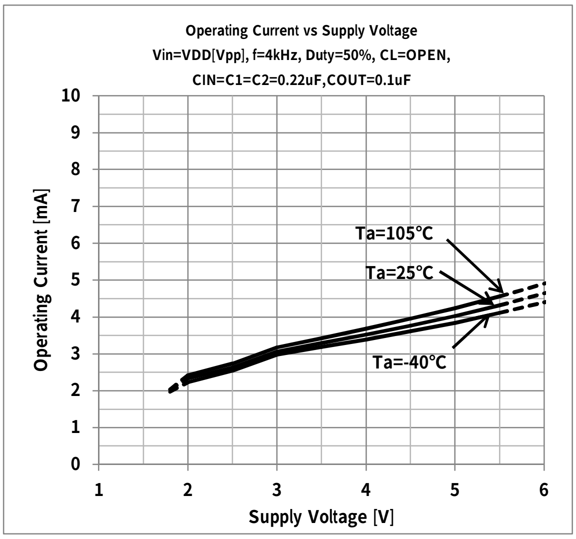
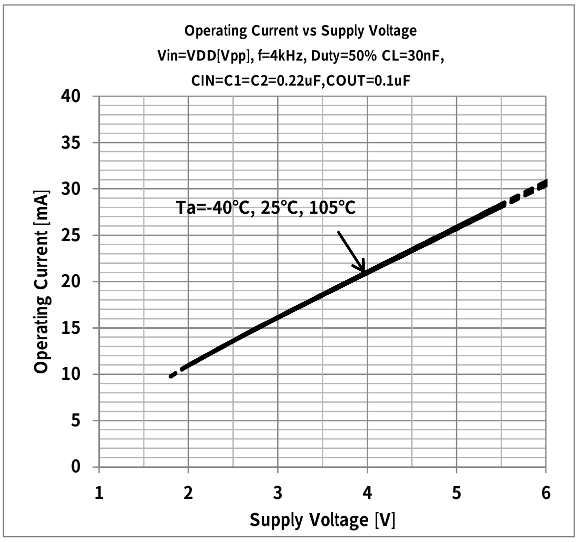
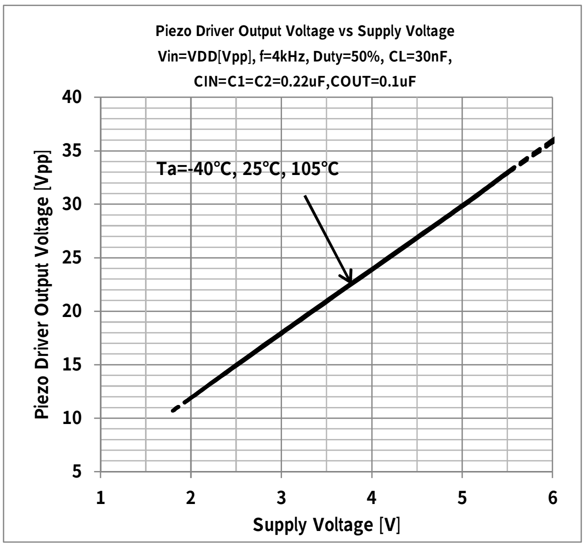


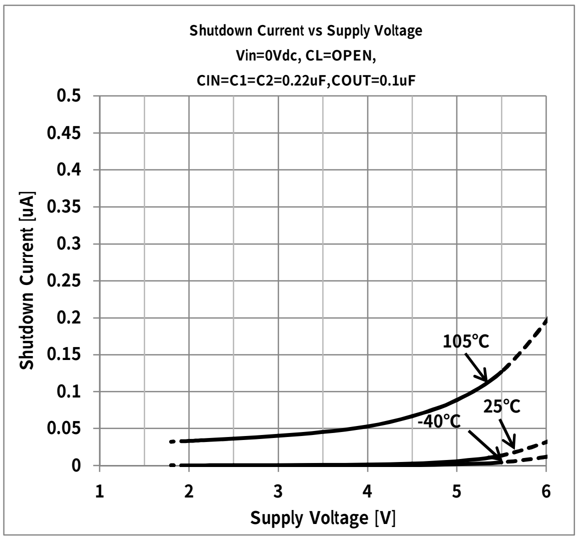

**Fig. 8 Example of application circuit**

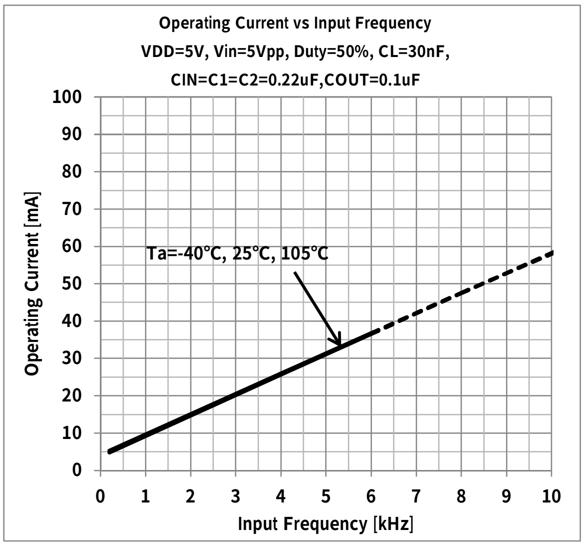
## 5. Typical Characteristics

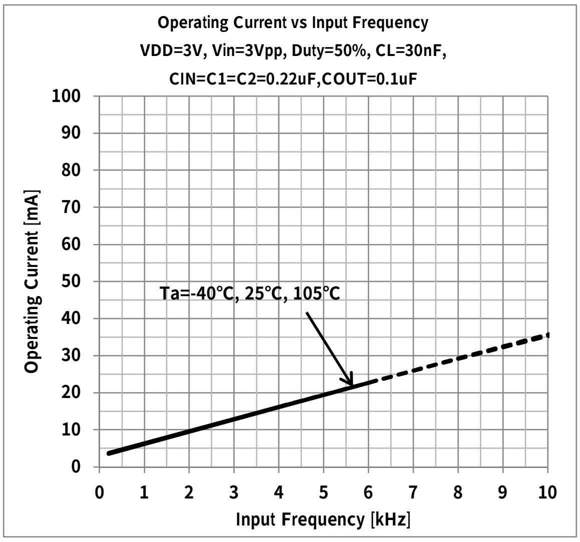


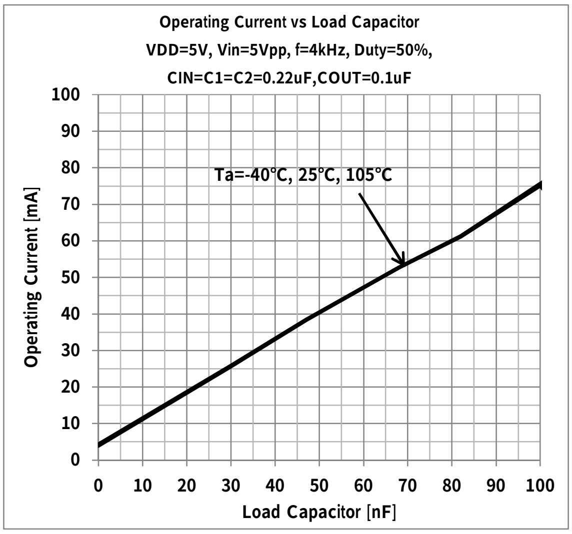



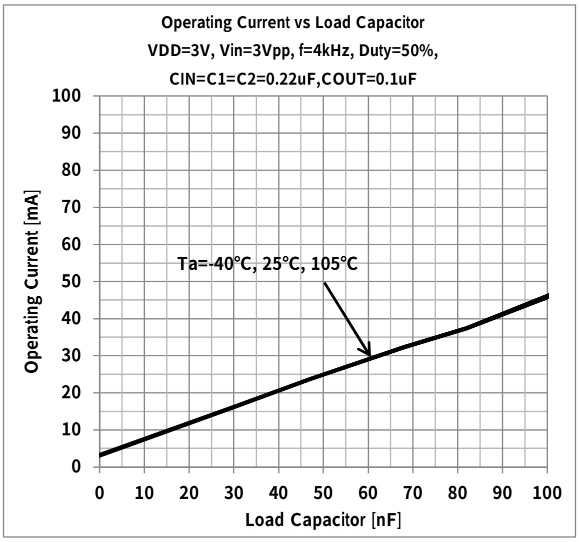



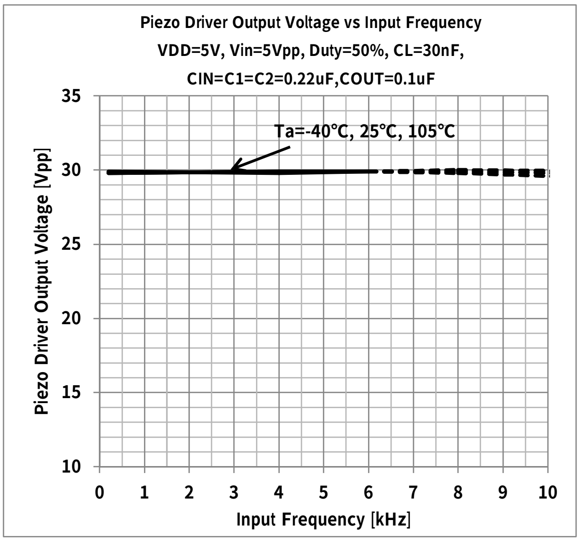



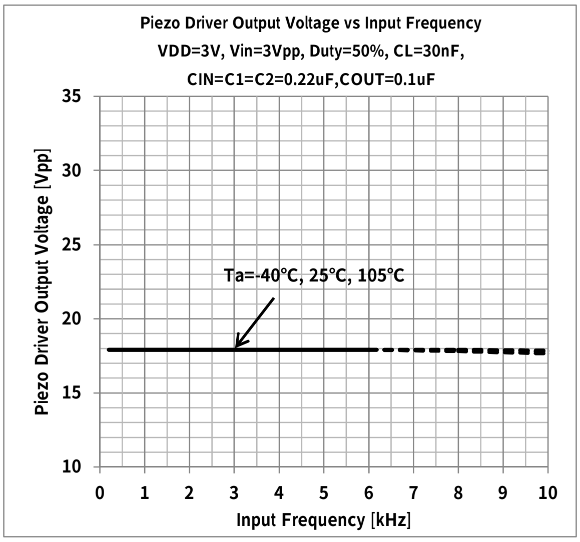



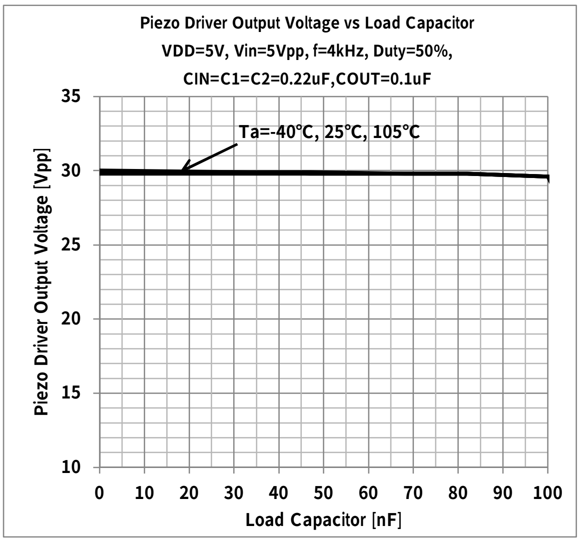



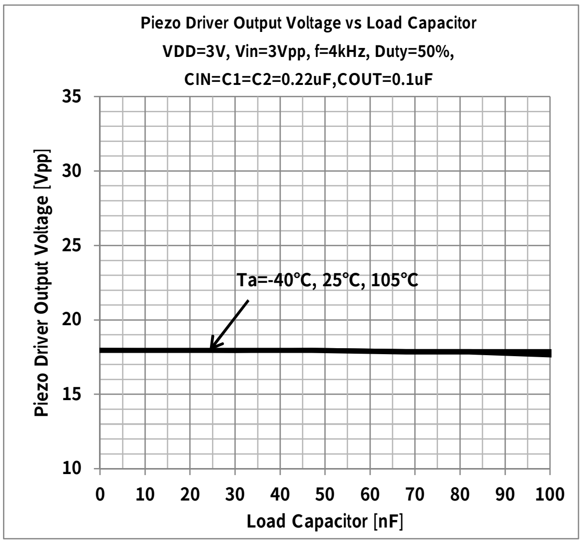

Operating Current vs Load Capacitor
VDD=5V, Vin=5Vpp, f=4kHz, Duty=50%,
CIN=C1=C2=0.22uF,COUT=0.1uF
Ta=-40°C, 25°C, 105°C
Operating Current [mA]
Load Capacitor [nF]
0 10 20 30 40 50 60 70 80 90 100


Operating Current vs Load Capacitor
VDD=3V, Vin=3Vpp, f=4kHz, Duty=50%,
CIN=C1=C2=0.22uF,COUT=0.1uF
Ta=-40°C, 25°C, 105°C
Operating Current [mA]
Load Capacitor [nF]
0 10 20 30 40 50 60 70 80 90 100


Piezo Driver Output Voltage vs Input Frequency
VDD=5V, Vin=5Vpp, Duty=50%, CL=30nF,
CIN=C1=C2=0.22uF,COUT=0.1uF
Ta=-40°C, 25°C, 105°C
Piezo Driver Output Voltage [Vpp]
Input Frequency [kHz]
10 15 20 25 30 35
0 1 2 3 4 5 6 7 8 9 10


Piezo Driver Output Voltage vs Input Frequency
VDD=3V, Vin=3Vpp, Duty=50%, CL=30nF,
CIN=C1=C2=0.22uF,COUT=0.1uF
Ta=-40°C, 25°C, 105°C
Piezo Driver Output Voltage [Vpp]
Input Frequency [kHz]
10 15 20 25 30 35
0 1 2 3 4 5 6 7 8 9 10


Piezo Driver Output Voltage vs Load Capacitor
VDD=5V, Vin=5Vpp, f=4kHz, Duty=50%,
CIN=C1=C2=0.22uF,COUT=0.1uF
Ta=-40°C, 25°C, 105°C
Piezo Driver Output Voltage [Vpp]
Load Capacitor [nF]
10 15 20 25 30 35
0 10 20 30 40 50 60 70 80 90 100


Piezo Driver Output Voltage vs Load Capacitor
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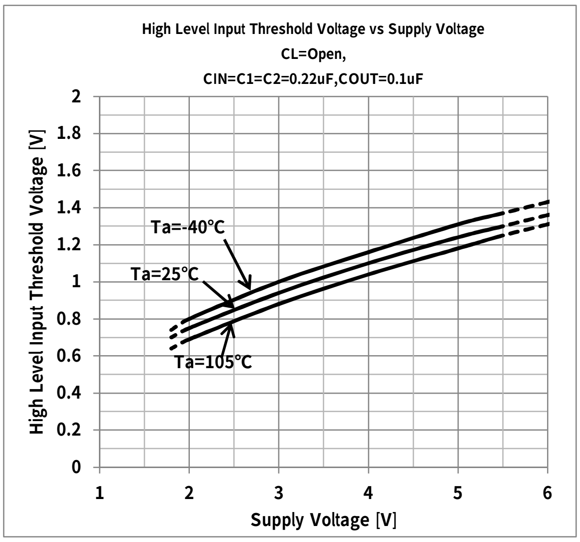
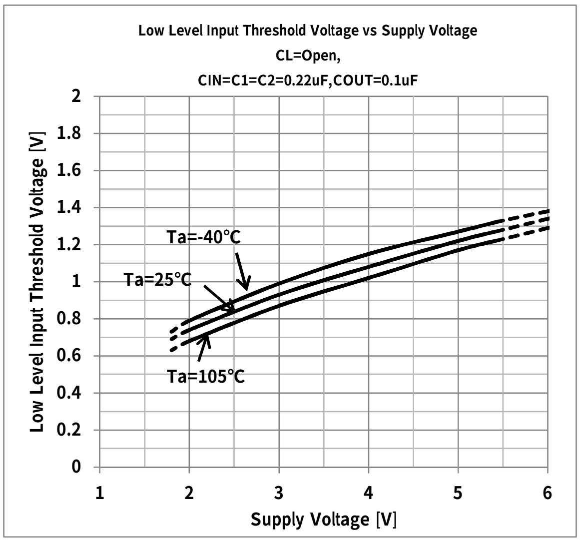
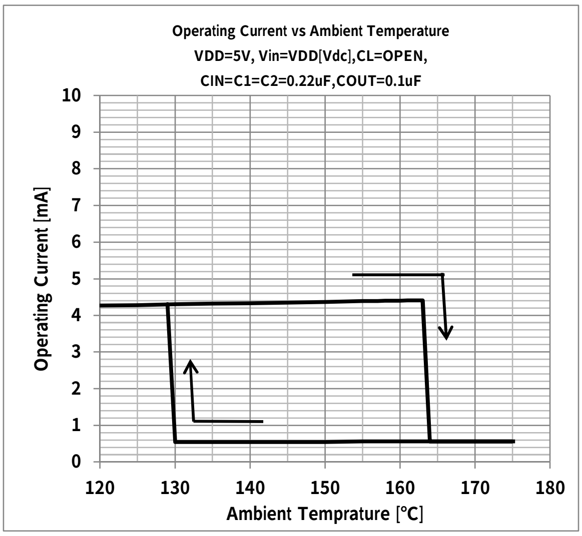
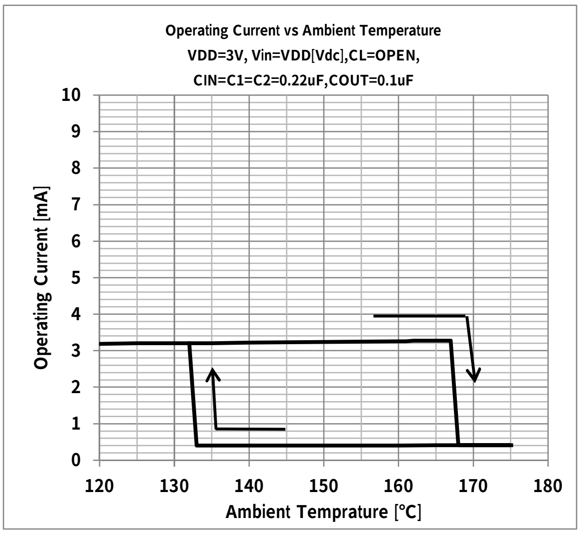
CIN=C1=C2=0.22uF,COUT=0.1uF
Ta=-40°C, 25°C, 105°C
Piezo Driver Output Voltage [Vpp]
Load Capacitor [nF]
10 15 20 25 30 35
0 10 20 30 40 50 60 70 80 90 100

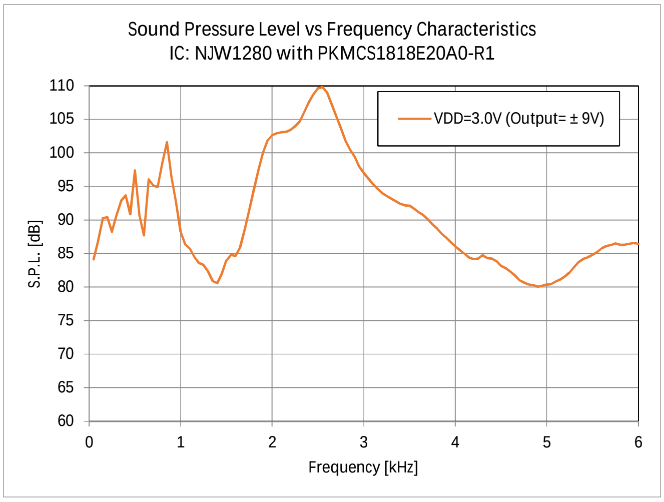

High Level Input Threshold Voltage vs Supply Voltage
CL=Open,
CIN=C1=C2=0.22uF,COUT=0.1uF
High Level Input Threshold Voltage [V]
Supply Voltage [V]
Ta=-40°C
Ta=25°C
Ta=105°C
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
1
2
3
4
5
6

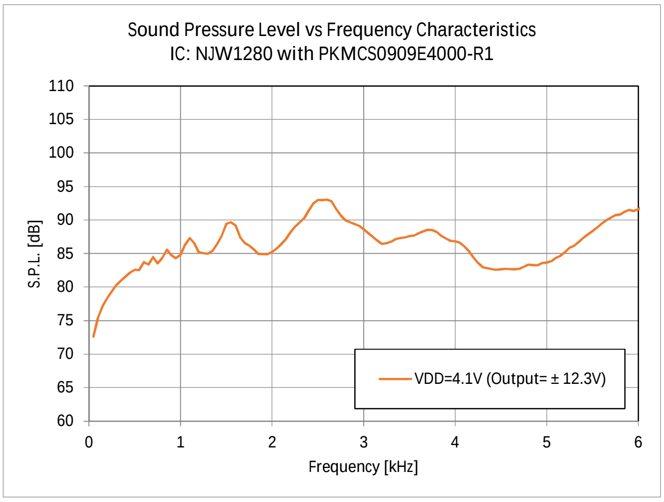

Low Level Input Threshold Voltage vs Supply Voltage
CL=Open,
CIN=C1=C2=0.22uF,COUT=0.1uF
Low Level Input Threshold Voltage [V]
Supply Voltage [V]
Ta=-40°C
Ta=25°C
Ta=105°C
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
1
2
3
4
5
6

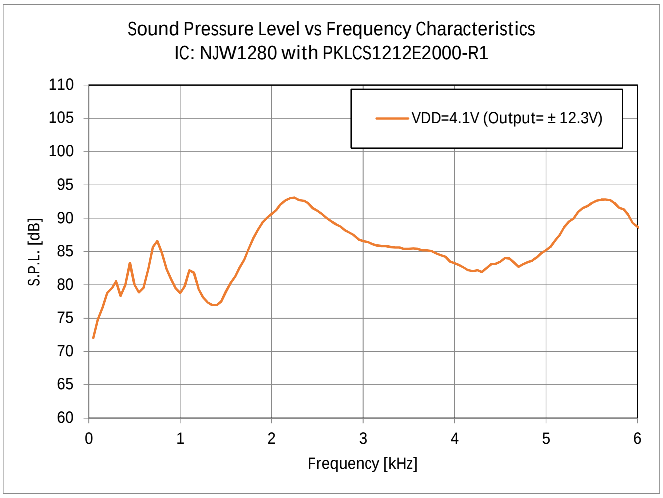

Operating Current vs Ambient Temperature
VDD=5V, Vin=VDD[Vdc],CL=OPEN,
CIN=C1=C2=0.22uF,COUT=0.1uF
Operating Current [mA]
Ambient Temprature [°C]
0
1
2
3
4
5
6
7
8
9
10
120
130
140
150
160
170
180

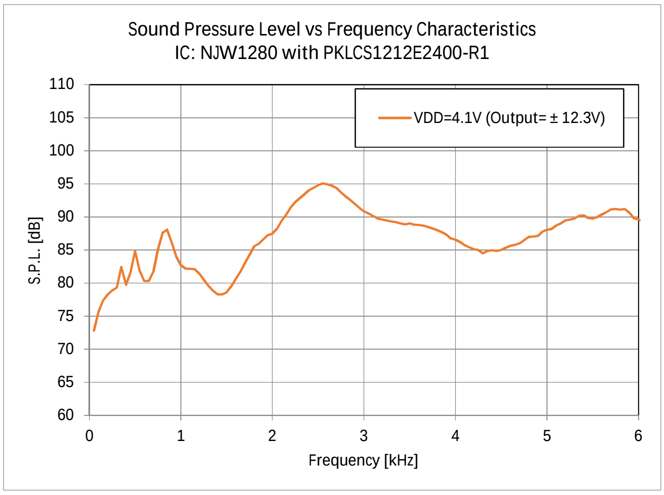

Operating Current vs Ambient Temperature
VDD=3V, Vin=VDD[Vdc],CL=OPEN,
CIN=C1=C2=0.22uF,COUT=0.1uF
Operating Current [mA]
Ambient Temprature [°C]
0
1
2
3
4
5
6
7
8
9
10
120
130
140
150
160
170
180

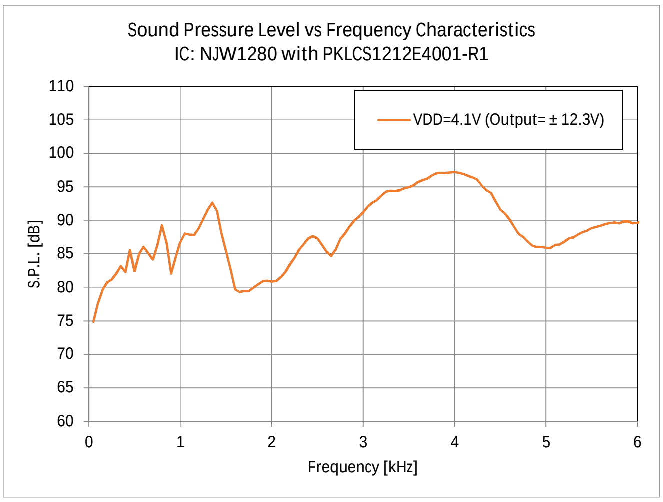
## 6. muRata Piezo sounder/buzzer recommended parts evaluation result

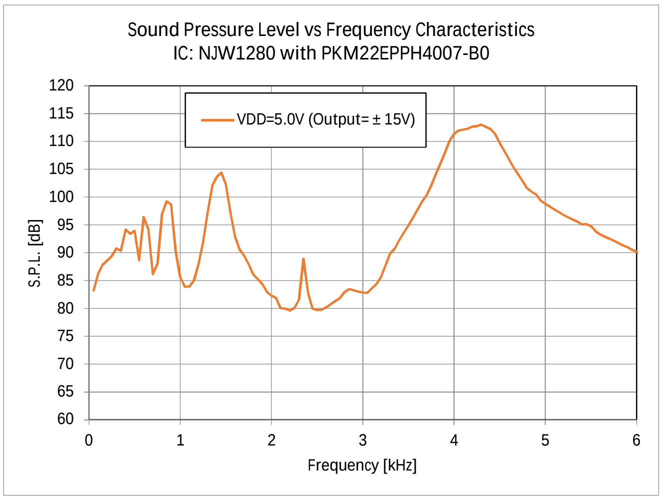


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