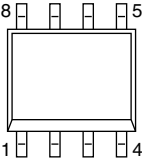
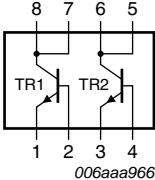




## 2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		
2	base TR1		
3	emitter TR2		
4	base TR2		
5	collector TR2		
6	collector TR2		
7	collector TR1		
8	collector TR1		

## 3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4021SN	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

## 4. Marking

Table 5. Marking codes

Type number	Marking code
PBSS4021SN	4021SN

## 5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

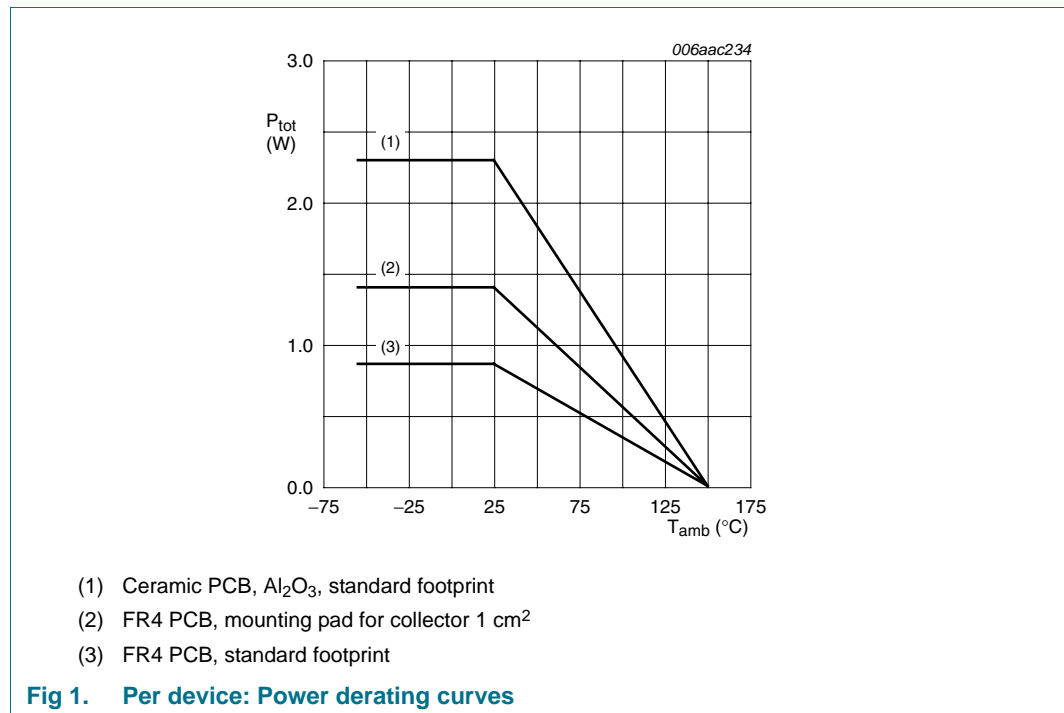
Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
$V_{CBO}$	collector-base voltage	open emitter	-	20	V	
$V_{CEO}$	collector-emitter voltage	open base	-	20	V	
$V_{EBO}$	emitter-base voltage	open collector	-	5	V	
$I_C$	collector current		-	7.5	A	
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	15	A	
$I_B$	base current		-	1	A	
$P_{tot}$	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	0.73	W
			[2]	-	1	W
			[3]	-	1.7	W

**Table 6. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per device</b>					
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	0.86	W
			[2]	1.4	W
			[3]	2.3	W
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-55	+150	°C
$T_{stg}$	storage temperature		-65	+150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

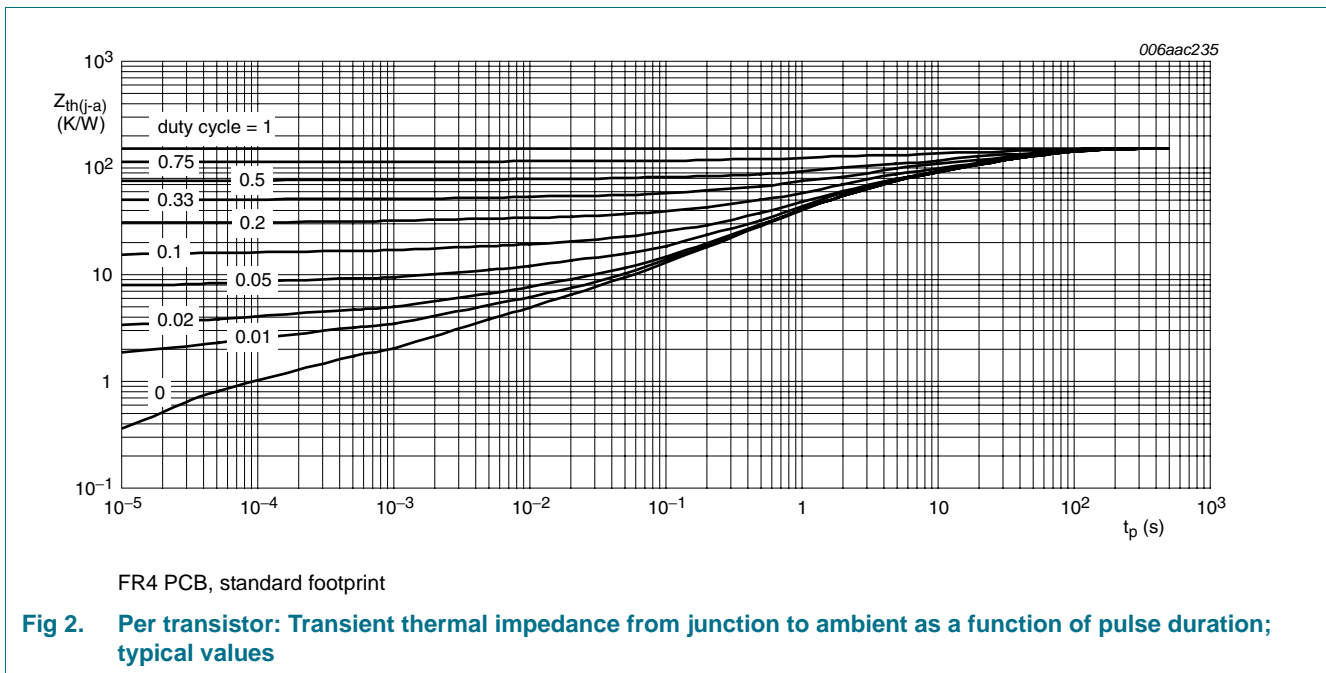


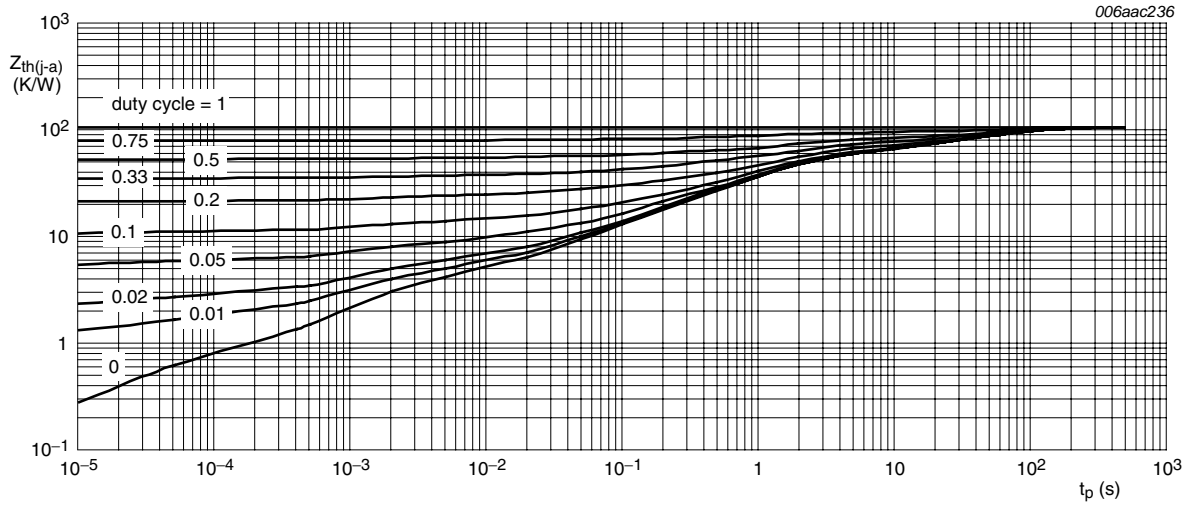
## 6. Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	170	K/W
			[2]	-	-	125	K/W
			[3]	-	-	75	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W	
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	145	K/W
			[2]	-	-	90	K/W
			[3]	-	-	55	K/W

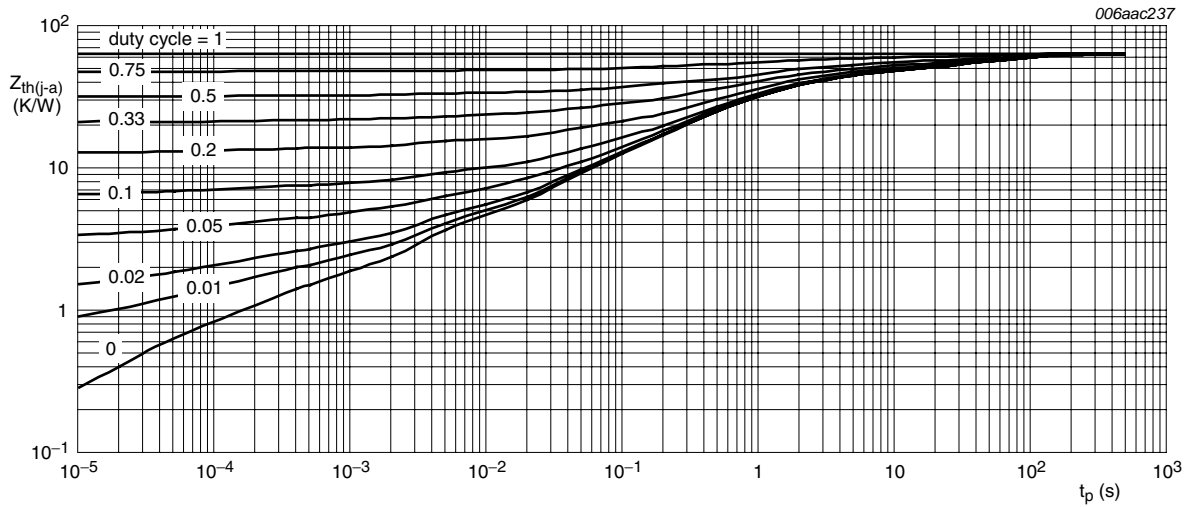
- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.





FR4 PCB, mounting pad for collector 1 cm<sup>2</sup>

**Fig 3.** Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

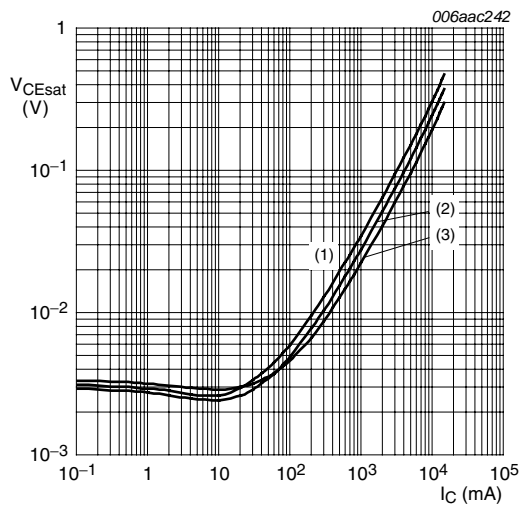


Ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint

**Fig 4.** Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

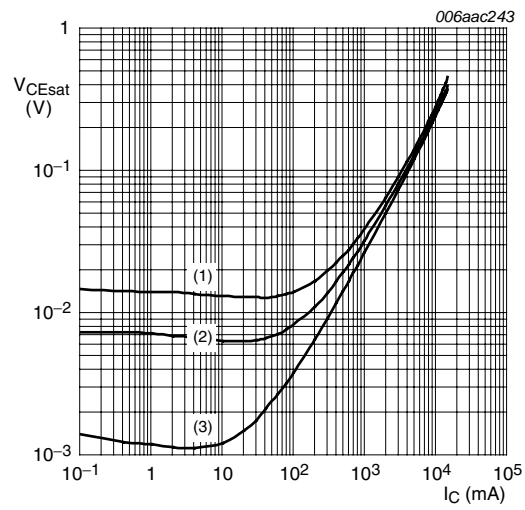






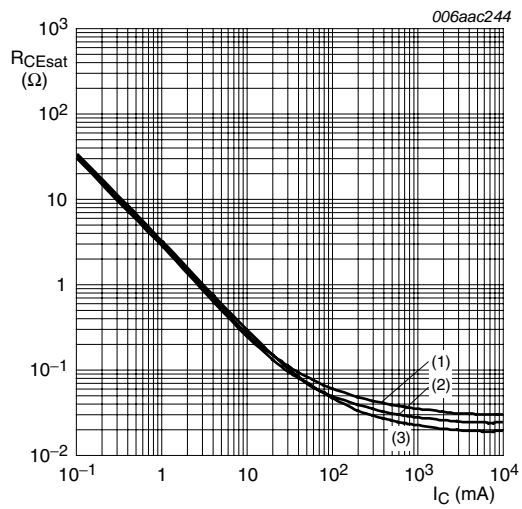
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values**



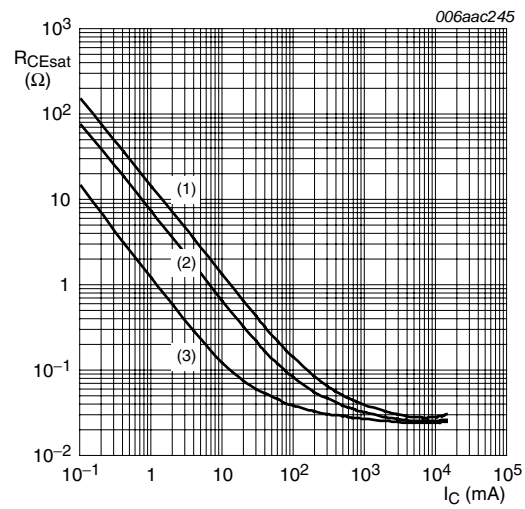
$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values**

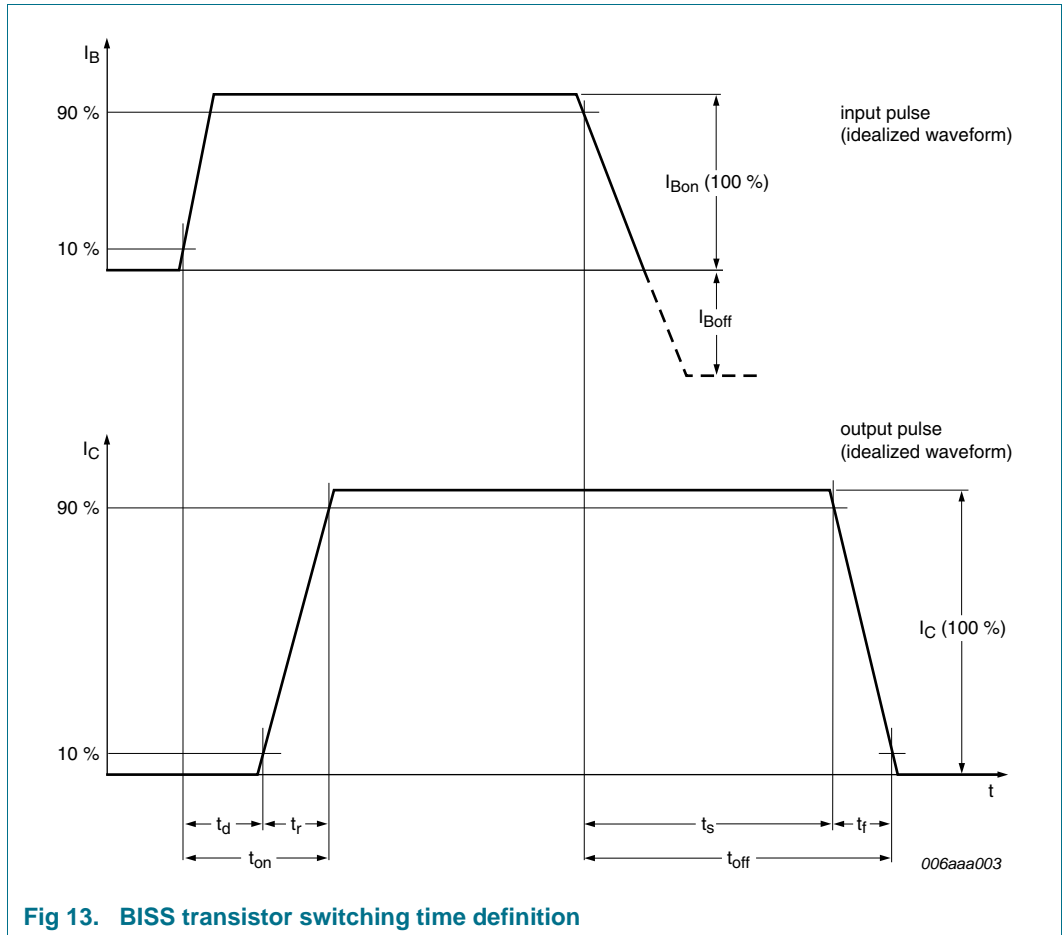


$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

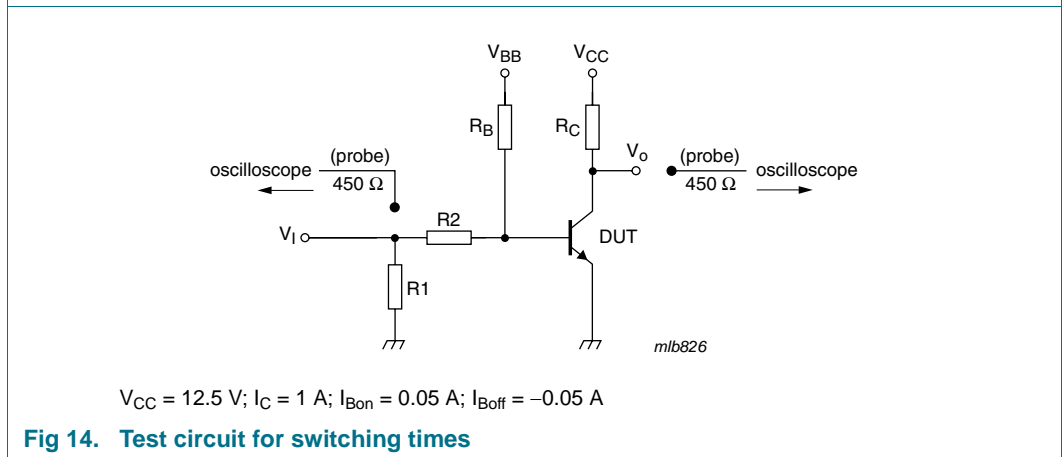
**Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values**



**8. Test information**

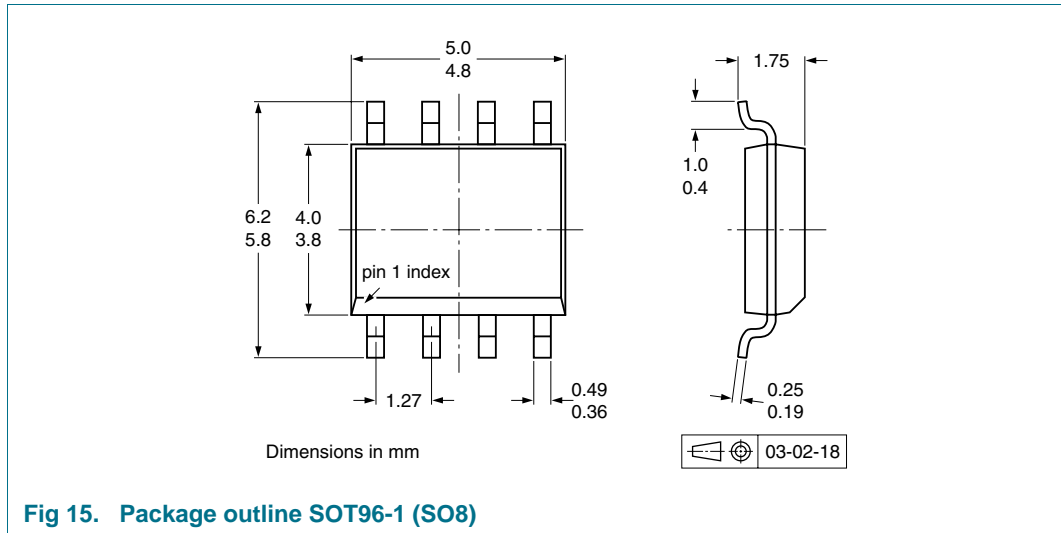


**Fig 13. BISS transistor switching time definition**



**Fig 14. Test circuit for switching times**

## 9. Package outline



## 10. Packing information

**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity	
			1000	2500
PBSS4021SN	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see [Section 14](#).









## 15. Contents

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