

LSF0204

4-bit bidirectional multi-voltage level translator; open-drain; push-pull

Rev. 1 — 18 May 2020

Product data sheet

1. General description

The LSF0204 is an 4 channel bidirectional multi-voltage level translator for open-drain and push-pull applications. It supports up to 100 MHz up translation and ≥ 100 MHz down translation at ≤ 30 pF capacitive load. There is no need for a direction pin which minimizes system effort. The LSF0204 supports 5 V tolerant I/O pins for compatibility with TTL levels in a variety of applications. The ability to set up different voltage translation levels on each channel makes the device very flexible and suitable for a lot of different applications.

2. Features and benefits

- Bidirectional voltage translation with no direction pin
- Up translation
 - ≥ 100 MHz; $C_L = 15$ pF, 30 pF
 - ≥ 50 MHz; $C_L = 50$ pF
- Down translation
 - ≥ 100 MHz; $C_L = 15$ pF, 30 pF
 - ≥ 50 MHz; $C_L = 50$ pF
- Hot insertion
- Bidirectional voltage level translation between:
 - 0.8 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
 - 1.2 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
 - 1.8 V and 2.5 V, 3.3 V and 5.0 V
 - 2.5 V and 3.3 V and 5.0 V
 - 3.3 V and 5.0 V
- Low standby current
- 5 V tolerant I/O pins to support TTL
- Low R_{ON} provides less signal distortion
- Latch-up performance exceeds 100 mA per JESD78 class II level A
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
 - CDM ANSI/ESDA/JEDEC JS-002 exceeds 1000 V
- Specified from -40 °C to $+125$ °C

3. Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I²C, and other interfaces in Telecom infrastructure
- Industrial
- Personal computing

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
LSF0204PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
LSF0204GU12	-40 °C to +125 °C	XQFN12	plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 × 2.0 × 0.50 mm	SOT1174-1

5. Functional diagram

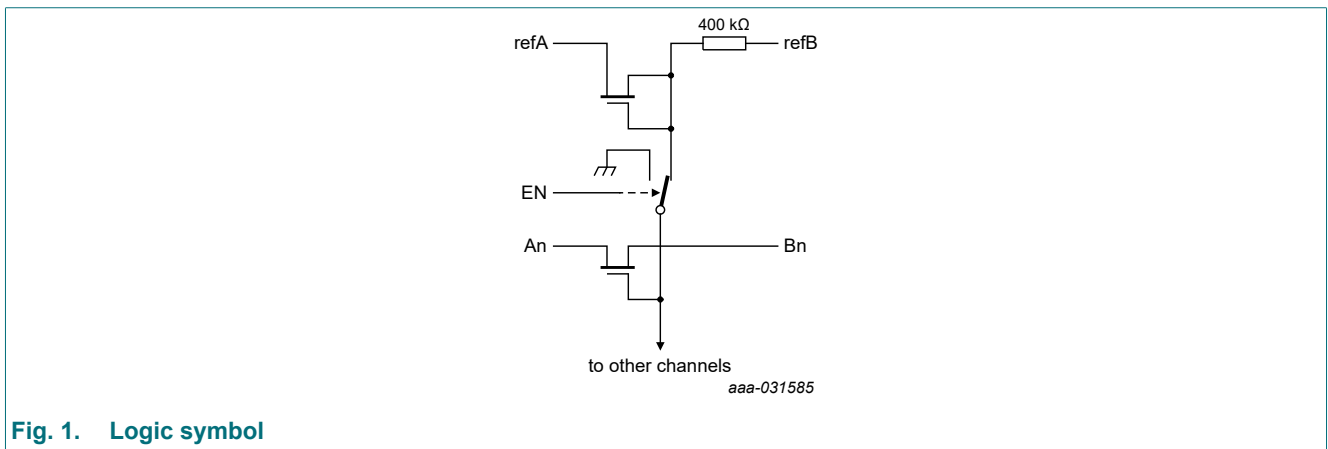


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning

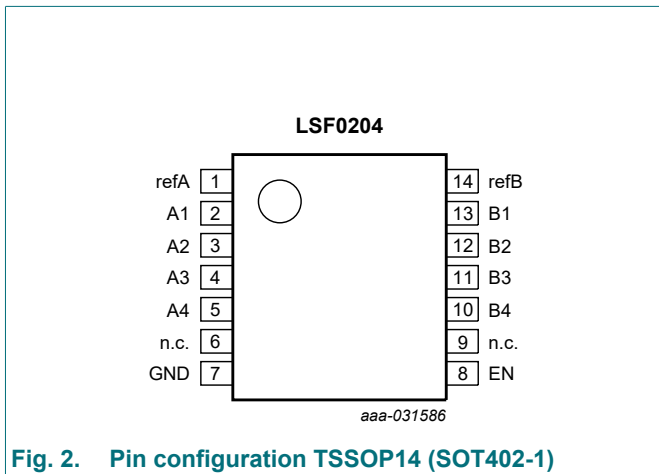


Fig. 2. Pin configuration TSSOP14 (SOT402-1)

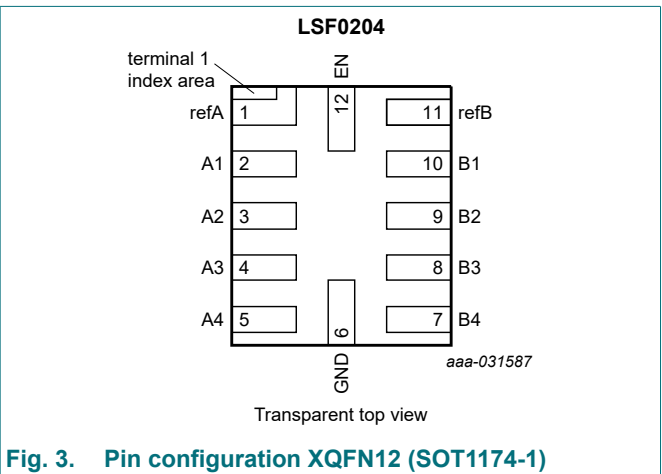


Fig. 3. Pin configuration XQFN12 (SOT1174-1)

6.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	TSSOP14	XQFN12	
refA	1	1	reference voltage A (EN input circuit is referenced to refA)
A1, A2, A3, A4	2, 3, 4, 5	2, 3, 4, 5	data input/output A
n.c.	6, 9	-	not connected
GND	7	6	ground (0 V)
EN	8	12	enable input (active HIGH)
B1, B2, B3, B4	13, 12, 11, 10	10, 9, 8, 7	data input/output B
refB	14	11	reference voltage B

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	input/output
EN[1]	An, Bn channel
H	An = Bn
L	Z

[1] EN input circuit is referenced to refA

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pins refA, refB, An, Bn and EN [1]	-0.5	+7.0	V
$I_{I/O}$	input/output current	pins refA, refB, An and Bn; continuous channel current	-	+128	mA
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	TSSOP14 package [2]	-	500	mW
		XQFN12 package	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pins refA, refB, An, Bn and EN	0.0	5.0	V
$I_{I/O}$	input/output current	pins refA, refB, An and Bn; continuous channel current	-	+64	mA
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	EN input	-	10	ns/V

10. Static characteristics

Table 6. Static characteristics

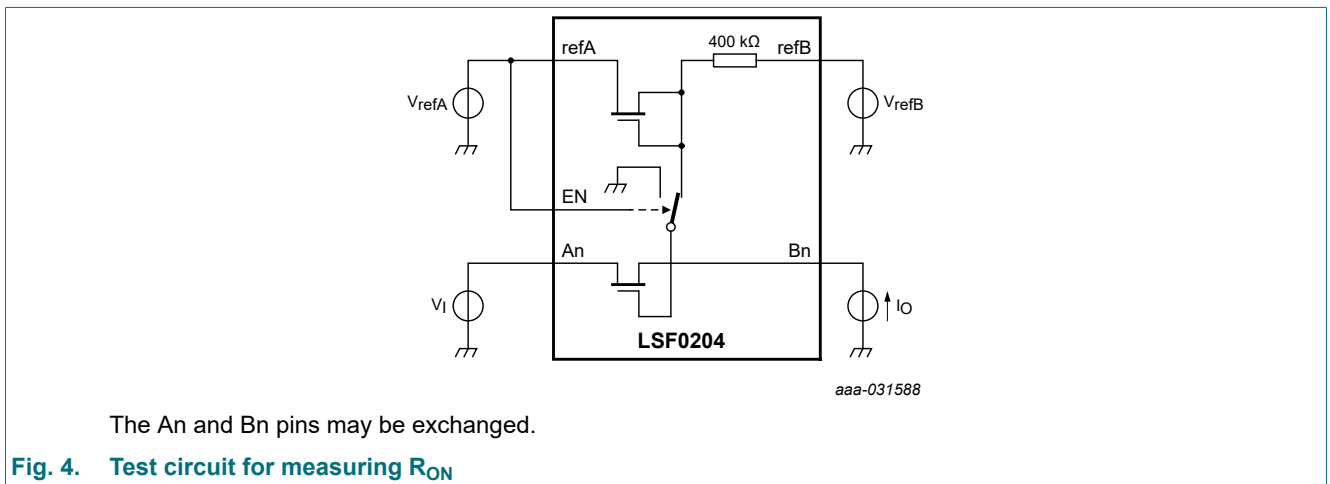
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+125\text{ °C}$			Unit
			Min	Typ [1]	Max	
V_{IK}	input clamping voltage	$V_{I(EN)} = 0\text{ V}$; $I_I = -18\text{ mA}$	-1.2	-	-	V
I_{IH}	HIGH-level input current	$V_I = 5\text{ V}$; $V_{I(EN)} = 0\text{ V}$	-	-	5	μA
I_I	input current	EN input; $V_{refA} = 4.5\text{ V}$; $V_{refB} = 5.5\text{ V}$; $V_{I(EN)} = 0\text{ V to }V_{refA}$; $I_O = 0\text{ A}$	-	-	± 1	μA
V_{IH}	HIGH-level input voltage	EN input				
		$V_{refA} = 1.5\text{ V to }4.5\text{ V}$	$0.7V_{refA}$	-	-	V
		$V_{refA} = 1.0\text{ V to }1.5\text{ V}$	$0.8V_{refA}$	-	-	V
V_{IL}	LOW-level input voltage	EN input				
		$V_{refA} = 1.5\text{ V to }4.5\text{ V}$	-	-	$0.3V_{refA}$	V
		$V_{refA} = 1.0\text{ V to }1.5\text{ V}$	-	-	$0.3V_{refA}$	V
I_{refB-A}	leakage current refB to refA	$V_{refA} = V_{I(EN)} = 1.8\text{ V}$; $V_{refB} = 3.3\text{ V}$; $I_O = 0\text{ A}$; $V_I = 3.3\text{ V or GND}$	-	-	3.5	μA
I_{GND}	ground current	$V_{refA} = V_{I(EN)} = 1.8\text{ V}$; $V_{refB} = 3.3\text{ V}$; $I_O = 0\text{ A}$; $V_I = 3.3\text{ V or GND}$	-	0.2	-	μA
I_{OFF}	power-off leakage current	$V_{refA} = V_{refB} = V_{I(EN)} = 0\text{ V}$; $I_O = 0\text{ A}$; $V_I = 5\text{ V or GND}$	-	-	± 1	μA
C_I	input capacitance	pins refA, refB and EN; $V_I = 3\text{ V or }0\text{ V}$	-	7	-	pF
$C_{io(off)}$	OFF-state input/output capacitance	pins An, Bn; $V_O = 0\text{ V or }3\text{ V}$; $V_{I(EN)} = 0\text{ V}$	-	3	6	pF
$C_{io(on)}$	ON-state input/output capacitance	pins An, Bn; $V_O = 0\text{ V or }3\text{ V}$; $V_{I(EN)} = 3.0\text{ V}$	-	8	13	pF

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Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ [1]	Max	
R _{ON}	ON resistance	see Fig. 4 [2]				
		V _I = 0 V; I _O = 64 mA;				
		V _{refA} = V _{I(EN)} = 3.3 V; V _{refB} = 5 V	-	3	-	Ω
		V _{refA} = V _{I(EN)} = 1.8 V; V _{refB} = 5 V	-	4	-	Ω
		V _I = 0 V; I _O = 32 mA;				
		V _{refA} = V _{I(EN)} = 1.0 V; V _{refB} = 5 V	-	7	-	Ω
		V _{refA} = V _{I(EN)} = 1.8 V; V _{refB} = 5 V	-	4	-	Ω
		V _{refA} = V _{I(EN)} = 2.5 V; V _{refB} = 5 V	-	3.5	-	Ω
		V _I = 1.8 V; I _O = 15 mA; V _{refA} = V _{I(EN)} = 3.3 V; V _{refB} = 5 V	-	5	-	Ω
		V _I = 1 V; I _O = 10 mA; V _{refA} = V _{I(EN)} = 1.8 V; V _{refB} = 3.3 V	-	8	-	Ω
		V _I = 0 V; I _O = 10 mA; V _{refA} = V _{I(EN)} = 1 V; V _{refB} = 3.3 V	-	6	-	Ω
		V _I = 0 V; I _O = 10 mA; V _{refA} = V _{I(EN)} = 1 V; V _{refB} = 1.8 V	-	6	-	Ω

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] Measured by the voltage drop between the An and Bn pins at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) pins.



11. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; for waveforms see Fig. 5 and Fig. 6; for test circuit see Fig. 7

Symbol	Parameter	Conditions	$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$			Unit
			Min	Typ[1]	Max	
Translating down (3.3 V to 1.8 V)						
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An				
		$V_{\text{refA}} = V_{\text{I(EN)}} = 1.8\text{ V}$; $V_{\text{refB}} = 3.3\text{ V}$; $V_{\text{I}} = 3.3\text{ V}$; $V_{\text{M}} = 1.15\text{ V}$				
		$C_{\text{L}} = 15\text{ pF}$	-	0.3	5.19	ns
		$C_{\text{L}} = 30\text{ pF}$	-	0.5	5.29	ns
		$C_{\text{L}} = 50\text{ pF}$	-	0.7	5.49	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An				
		$V_{\text{refA}} = V_{\text{I(EN)}} = 1.8\text{ V}$; $V_{\text{refB}} = 3.3\text{ V}$; $V_{\text{I}} = 3.3\text{ V}$; $V_{\text{M}} = 1.15\text{ V}$				
		$C_{\text{L}} = 15\text{ pF}$	-	0.5	4.5	ns
		$C_{\text{L}} = 30\text{ pF}$	-	0.7	4.7	ns
		$C_{\text{L}} = 50\text{ pF}$	-	0.9	4.9	ns
t_{PLZ}	LOW to OFF-state propagation delay	EN to An or Bn				
		$V_{\text{refA}} = V_{\text{I(EN)}} = 1.8\text{ V}$; $V_{\text{refB}} = 3.3\text{ V}$; $V_{\text{M}} = 1.15\text{ V}$				
		$C_{\text{L}} = 15\text{ pF}$	-	11	15	ns
		$C_{\text{L}} = 30\text{ pF}$	-	12	16.5	ns
		$C_{\text{L}} = 50\text{ pF}$	-	13	18	ns
t_{PZL}	OFF-state to LOW propagation delay	EN to An or Bn				
		$V_{\text{refA}} = V_{\text{I(EN)}} = 1.8\text{ V}$; $V_{\text{refB}} = 3.3\text{ V}$; $V_{\text{M}} = 1.15\text{ V}$				
		$C_{\text{L}} = 15\text{ pF}$	-	23	37	ns
		$C_{\text{L}} = 30\text{ pF}$	-	30	40	ns
		$C_{\text{L}} = 50\text{ pF}$	-	33	45	ns
f_{max}	maximum frequency	$V_{\text{refA}} = V_{\text{I(EN)}} = 1.8\text{ V}$; $V_{\text{refB}} = 3.3\text{ V}$; $V_{\text{I}} = 3.3\text{ V}$; $V_{\text{M}} = 1.15\text{ V}$				
		$C_{\text{L}} = 15\text{ pF}$	-	140	-	MHz
		$C_{\text{L}} = 30\text{ pF}$	-	110	-	MHz
		$C_{\text{L}} = 50\text{ pF}$	-	80	-	MHz
Translating down (3.3 V to 1.2 V)						
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An				
		$V_{\text{refA}} = V_{\text{I(EN)}} = 1.2\text{ V}$; $V_{\text{refB}} = 3.3\text{ V}$; $V_{\text{I}} = 3.3\text{ V}$; $V_{\text{M}} = 0.85\text{ V}$				
		$C_{\text{L}} = 15\text{ pF}$	-	0.3	3.8	ns
		$C_{\text{L}} = 30\text{ pF}$	-	0.5	3.9	ns
		$C_{\text{L}} = 50\text{ pF}$	-	0.8	4.1	ns

4-bit bidirectional multi-voltage level translator; open-drain; push-pull

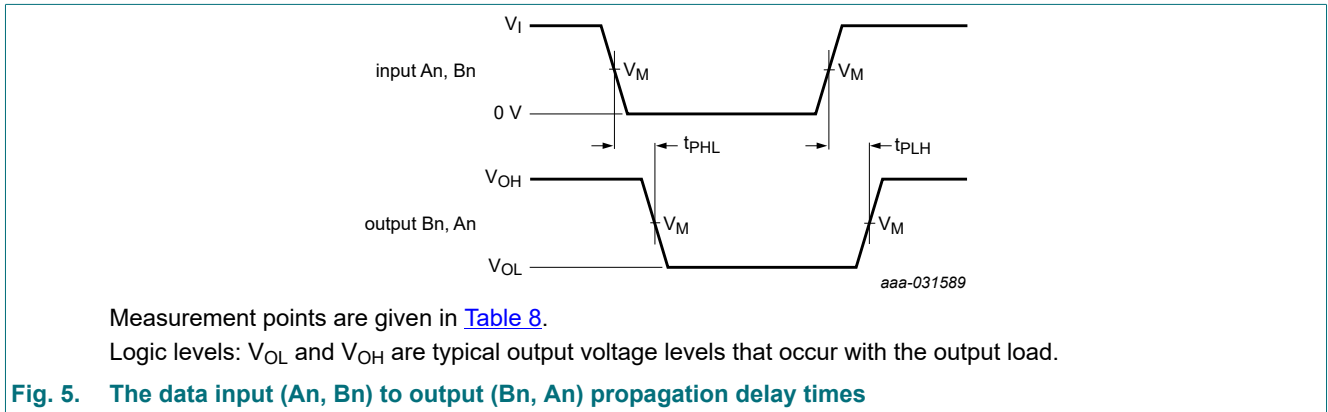
Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
t _{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An				
		V _{refA} = V _{I(EN)} = 1.2 V; V _{refB} = 3.3 V; V _I = 3.3 V; V _M = 0.85 V				
		C _L = 15 pF	-	0.6	4.3	ns
		C _L = 30 pF	-	0.7	4.5	ns
		C _L = 50 pF	-	0.9	4.7	ns
f _{max}	maximum frequency	V _{refA} = V _{I(EN)} = 1.2 V; V _{refB} = 3.3 V; V _I = 3.3 V; V _M = 0.85 V				
		C _L = 15 pF	-	120	-	MHz
		C _L = 30 pF	-	100	-	MHz
		C _L = 50 pF	-	80	-	MHz
Translating up (1.8 V to 3.3 V)						
t _{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An				
		V _{refA} = V _{I(EN)} = 1.8 V; V _{refB} = 3.3 V; V _I = 1.8 V; V _M = 0.9 V				
		C _L = 15 pF	-	0.2	5.1	ns
		C _L = 30 pF	-	0.4	5.3	ns
		C _L = 50 pF	-	0.6	5.7	ns
t _{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An				
		V _{refA} = V _{I(EN)} = 1.8 V; V _{refB} = 3.3 V; V _I = 1.8 V; V _M = 0.9 V				
		C _L = 15 pF	-	0.7	5.3	ns
		C _L = 30 pF	-	1	6.4	ns
		C _L = 50 pF	-	1.3	6.7	ns
t _{PLZ}	LOW to OFF-state propagation delay	EN to An or Bn				
		V _{refA} = V _{I(EN)} = 1.8 V; V _{refB} = 3.3 V; V _M = 0.9 V				
		C _L = 15 pF	-	11	15	ns
		C _L = 30 pF	-	12	16.5	ns
		C _L = 50 pF	-	13	18	ns
t _{PZL}	OFF-state to LOW propagation delay	EN to An or Bn				
		V _{refA} = V _{I(EN)} = 1.8 V; V _{refB} = 3.3 V; V _M = 0.9 V				
		C _L = 15 pF	-	23	37	ns
		C _L = 30 pF	-	30	40	ns
		C _L = 50 pF	-	33	45	ns
f _{max}	maximum frequency	V _{refA} = V _{I(EN)} = 1.8 V; V _{refB} = 3.3 V; V _I = 1.8 V; V _M = 0.9 V; R _L = 100 Ω				
		C _L = 15 pF	-	140	-	MHz
		C _L = 30 pF	-	140	-	MHz
		C _L = 50 pF	-	90	-	MHz

4-bit bidirectional multi-voltage level translator; open-drain; push-pull

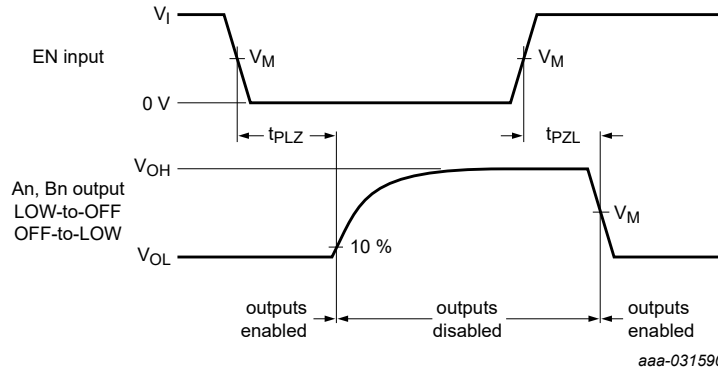
Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Translating up (1.2 V to 1.8 V)						
t _{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An				
		V _{refA} = V _{I(EN)} = 1.2 V; V _{refB} = 1.8 V; V _I = 1.2 V; V _M = 0.6 V				
		C _L = 15 pF	-	0.2	6.85	ns
		C _L = 30 pF	-	0.4	7.05	ns
t _{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An				
		V _{refA} = V _{I(EN)} = 1.2 V; V _{refB} = 1.8 V; V _I = 1.2 V; V _M = 0.6 V				
		C _L = 15 pF	-	1	5.4	ns
		C _L = 30 pF	-	1.3	6.5	ns
f _{max}	maximum frequency	V _{refA} = V _{I(EN)} = 1.2 V; V _{refB} = 1.8 V; V _I = 1.2 V; V _M = 0.6 V; R _L = 100 Ω				
		C _L = 15 pF	-	140	-	MHz
		C _L = 30 pF	-	130	-	MHz
		C _L = 50 pF	-	100	-	MHz

[1] All typical values are measured at T_{amb} = 25 °C.

11.1. Waveforms and test circuit



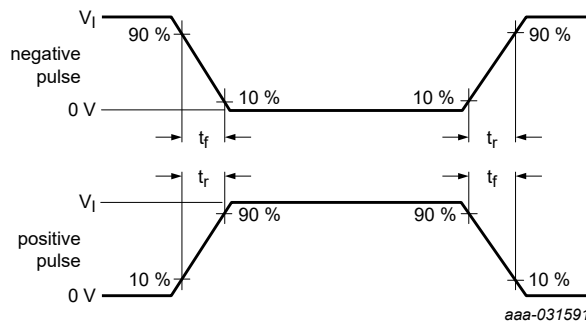
4-bit bidirectional multi-voltage level translator; open-drain; push-pull



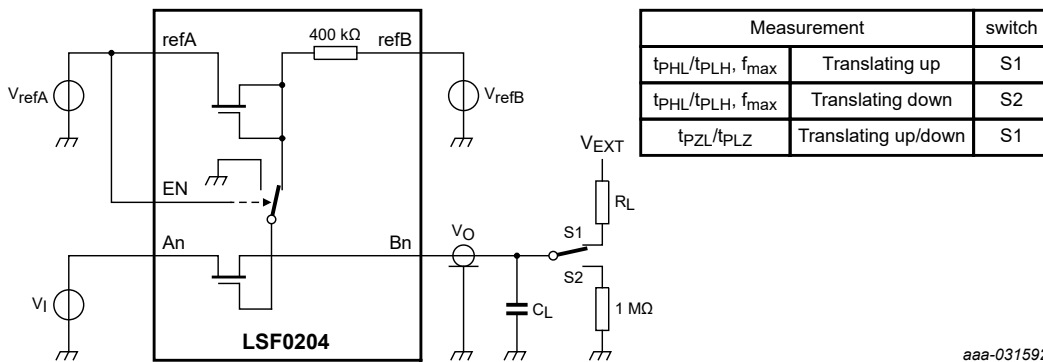
Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The enable (EN) to output (An, Bn) propagation delay times



a. V_I source waveform



b. Test circuit

Test data is given in [Table 8](#); The An and Bn pins may be exchanged.

All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz; $Z_O = 50 \Omega$.

Definitions test circuit: C_L = Load capacitance including jig and probe capacitance; R_L = Load resistance; S1/S2 = Test selection switch.

Fig. 7. Test circuit for measuring switching times

Table 8. Test data

Input	Load		V_{EXT}		
	C_L	R_L			
t_r, t_f		$t_{PLH}, t_{PHL}, t_{PLZ}, t_{PZL}$	f_{max}	$t_{PLH}, t_{PHL}, f_{max}$	t_{PLZ}, t_{PZL} [1]
≤ 2 ns	15 pF, 30 pF, 50 pF	500 Ω	100 Ω	V_{refB}	V_{refA}, V_{refB}

[1] For measuring t_{PLZ}, t_{PZL} (translating up) $V_{EXT} = V_{refB}$.
 For measuring t_{PLZ}, t_{PZL} (translating down) $V_{EXT} = V_{refA}$.

12. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

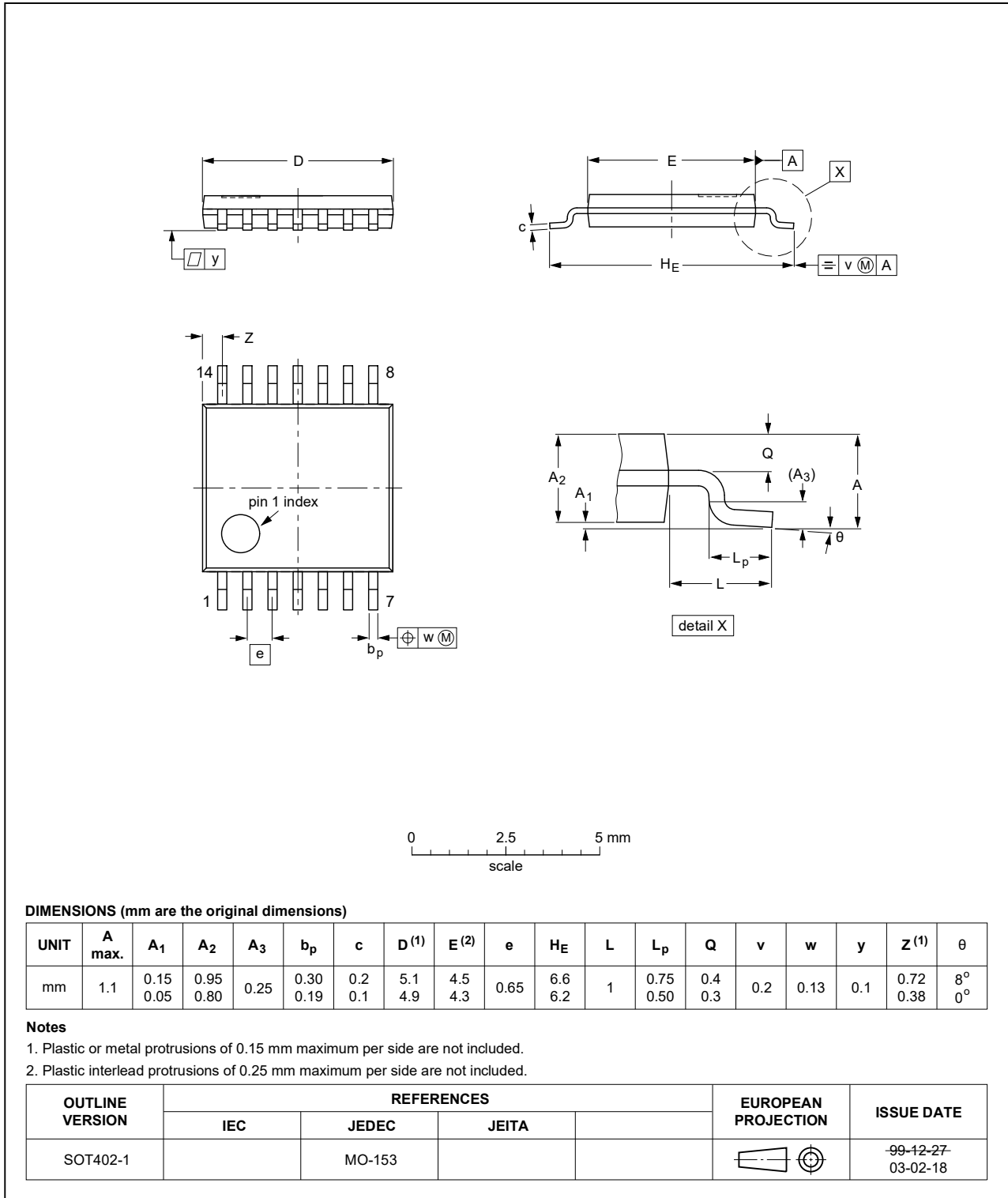


Fig. 8. Package outline SOT402-1 (TSSOP14)

4-bit bidirectional multi-voltage level translator; open-drain; push-pull

XQFN12: plastic, extremely thin quad flat package; no leads;
12 terminals; body 1.70 x 2.00 x 0.50 mm

SOT1174-1

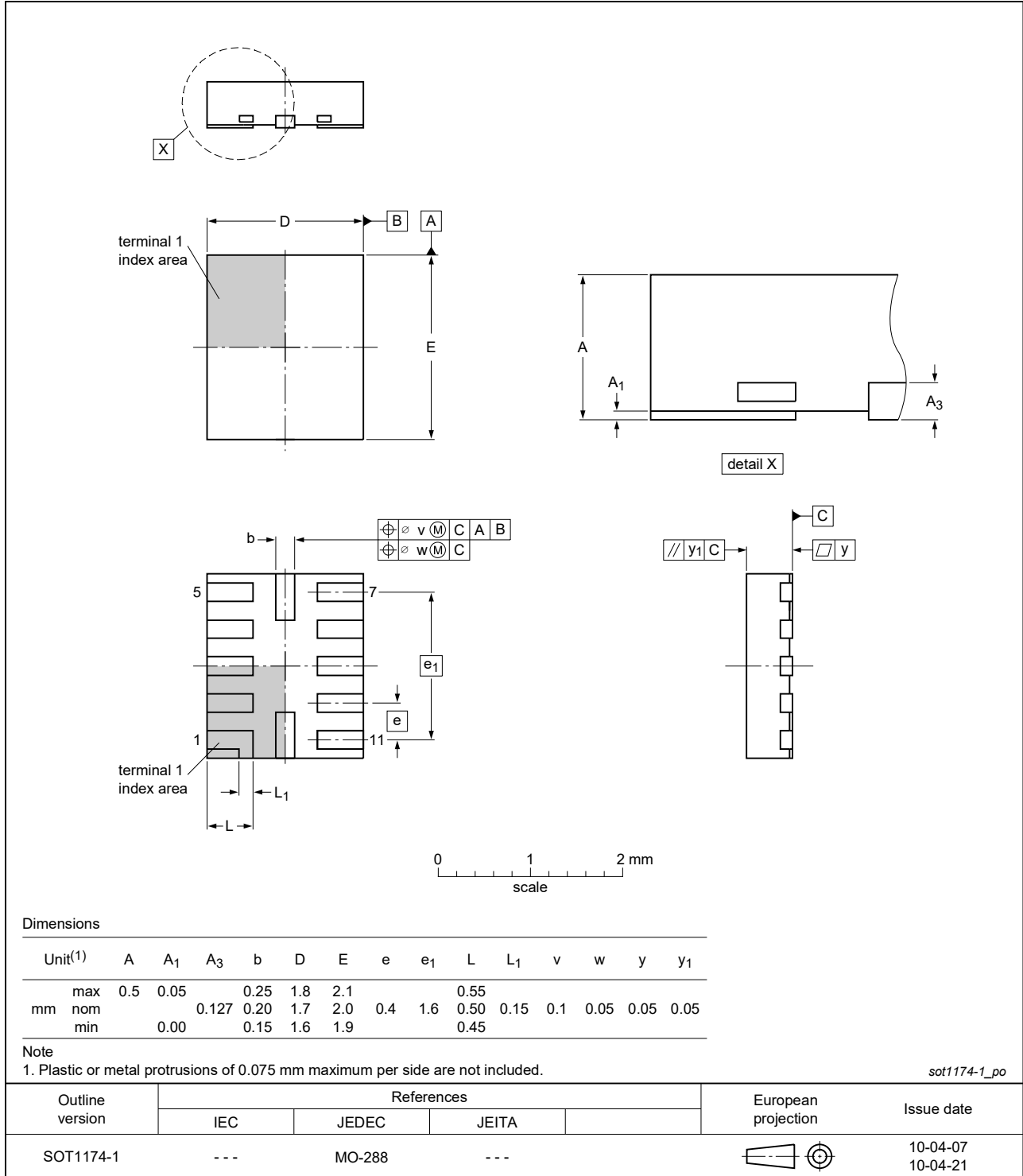


Fig. 9. Package outline SOT1174-1 (XQFN12)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LSF0204 v.1	20200518	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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