MP44011

Boundary-Mode PFC Controller with Harmonic Injection

The Future of Analog IC Technology

DESCRIPTION

The MP44011 is a boundary-conduction–mode PFC controller with an internal-harmonic–injection function. It provides simple and high-performance active power-factor correction with minimal external components.

Compared against traditional boundary-conduction–mode PFC controllers, the harmonic-injection function makes the part suitable for LED lighting applications.

In LED lighting applications with two-stage structures, the harmonic-injection function can effectively reduce bus capacitance between the AC/DC and the DC/DC stage. In addition, harmonic injection can reduce the transformer size to save board space and BOM cost.

Also, the benefits of a harmonic-injection function also apply to general boost or flyback PFC applications.

The MP44011 is derived from the MP44010, except with a harmonic-injection function.

The MP44011 is available in an 8-pin SOIC package.

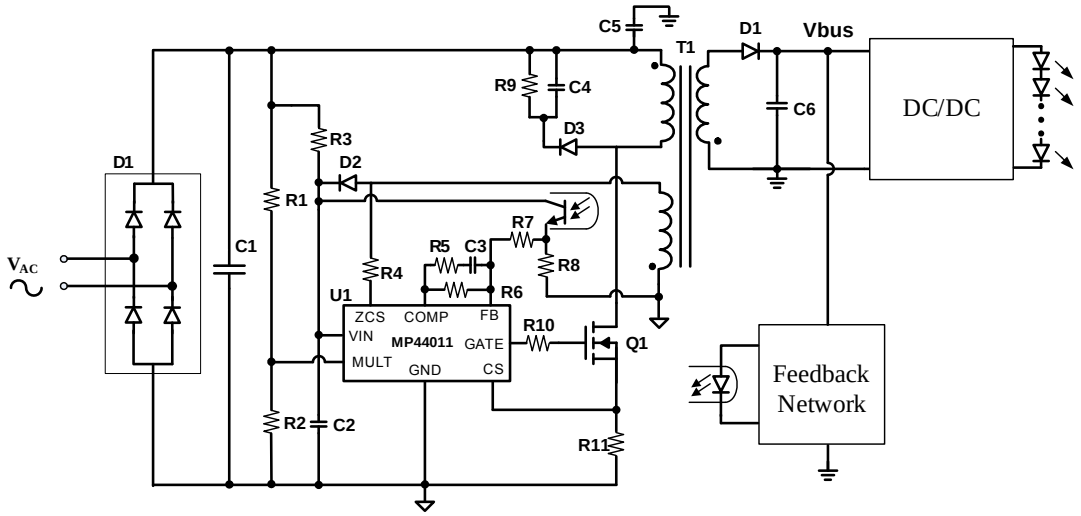
FEATURES

- Boundary-Conduction–Mode PFC Controller for Pre-Regulation
- Reduced Bus Capacitance
- Reduced Transformer Size
- Internal Harmonic-Injection Function
- Precise Adjustable-Output Over-Voltage Protection
- Ultra-Low Start-Up Current
- Very Low Quiescent Current
- On-Chip Filter for Current-Sense Pin
- Disable Function
- Available in SOIC-8

APPLICATIONS

- LED Lighting Driver
- General PFC Pre-Regulators

TYPICAL APPLICATION

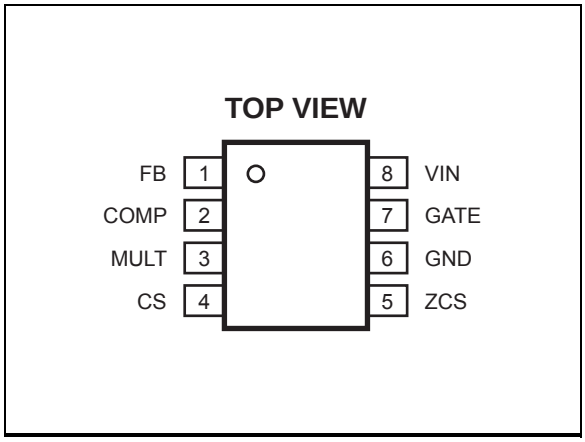


ORDERING INFORMATION

Part Number	Package	Top Marking	Junction Temperature (T_J)
MP44011HS*	SOIC8	MP44011	-40°C to +125°C

* For Tape & Reel, add suffix –Z (e.g. MP44011HS–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP44011HS–LF–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN}).....-0.5V to +23V
Analog Inputs and Outputs .....-0.3V to +6.5V
ZCS Maximum Current .....-50mA to +10mA
Power Dissipation (T_A=25°C) (2)
SOIC8 ..... 1.4W
Junction Temperature……...150°C
Lead Temperature (Solder).....260°C
Storage Temperature..... -55°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage (V_{IN}).....13.4V to 22V
Analog Inputs and Outputs .....-0.3V to +6V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC8	90	45 ... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, T_A =T_J= 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating Range	V_{IN}	After turn on	10.7		22	V
Turn-On Threshold	$V_{IN\ on}$		11	12.4	13.4	V
Turn-Off Threshold	$V_{IN\ off}$		8.7	9.8	10.7	V
Hysteretic Voltage	$V_{IN\ hys}$		2.2		3	V
Zener Voltage	V_z	I_{IN}=5mA	22	25	28	V
Supply Current						
Start-Up Current	$I_{startup}$	V_{IN}=11V		15	40	µA
Quiescent Current	I_q	No switch		0.46	0.65	mA
Operating Current	I_{IN}	F_s =70kHz, C_O=1nF		1.6	2.5	mA
Multiplier						
Input Bias Current	I_{MULT}				-1	µA
Linear Operation Range	V_{MULT}		0 to 3			V
Output Max. Slope	$\Delta V_{CS}/\Delta V_{MULT}$		1.62	1.85		V/V
Gain[5]	K			0.6	0.82	1/V
Error Amplifier						
Feedback Voltage	V_{FB}		2.465	2.5	2.535	V
Feedback Voltage Line Regulation	V_{FB_LR}	VIN=10.7V to 22V		2	5	mV
Feedback Bias Current	I_{FB}				0.2	µA
Open Loop Voltage Gain[6]	G_V		60	80		dB
Gain-Bandwidth Product[6]	GB			1		MHz
Source Current	I_{COMP_source}		-5	-4	-2	mA
Sink Current	I_{COMP_sink}		2.5	5.5		mA
Upper Clamp Voltage	V_{COMP_H}		5.3	6	6.6	V
Lower Clamp Voltage	V_{COMP_L}		2	2.2	2.4	V
Current Sense Comparator						
Input Bias Current	I_{CS}				-1	µA
Delay	t_{DT}			300	450	ns
Current Sense Clamp Voltage	$V_{CS\ Clamp}$		1.6	1.72	1.83	V
Current Sense Offset	V_{CS_Offset}	V_{MULT}=0V		30		mV
		V_{MULT}=2.5V		5		mV
Zero Current Sensor						
Upper Clamp Voltage	$V_{ZCSclamp\ H}$	I_{ZCS}=2.5mA	7.2	7.8		V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 15V, T_A = T_J=25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Lower Clamp Voltage	$V_{ZCSclamp\ L}$	I_{ZCS}=-2.5mA	0.3	0.55	0.8	V
Zero Current Sensing Threshold	$V_{ZCS\ H}$	V_{ZCS} rising		2.1	2.3	V
	$V_{ZCS\ L}$	V_{ZCS} falling	1.15	1.35		V
ZCS_EN Threshold	$V_{ZCS\ EN\ R}$	V_{ZCS} rising		310		mV
ZCS_EN Hysteresis	$V_{ZCS\ EN\ hys}$			120		mV
Source Current Capability	$I_{ZCS\ source}$				-3	mA
Restart Current After Disable	$I_{ZCS\ res}$			-85	-60	µA
Re-Starter						
Re-Start Time	t_{start}		80	175	280	µs
Over-Voltage						
Dynamic OVP Current	I_{OVP}		30	40	50	µA
Hysteresis	$I_{OVP\ Hys}$			30		µA
Static OVP Threshold	V_{OVP}		2	2.2	2.4	V
Gate Driver						
Dropout Voltage	V_{OH}	$I_{GDsource}$=20mA		2.4	3	V
		$I_{GDsource}$=200mA		4.8	5.4	V
	V_{OL}	I_{GDsink}=200mA		1.2	1.5	V
Voltage Fall Time	t_f			30	70	ns
Voltage Rise Time	t_r			40	80	ns
Max Output Drive Voltage	$V_{D\ max}$		12	13.5	15	V
Source Current Capability	$I_{Gate\ source}$			-350		mA
Sink Current Capability	$I_{Gate\ sink}$			600		mA
UVLO Saturation Voltage	$V_{Saturation}$	V_{IN}=0 to V_{IN_ON}, $I_{Gate\ sink}$=10mA			0.3	V

Note:

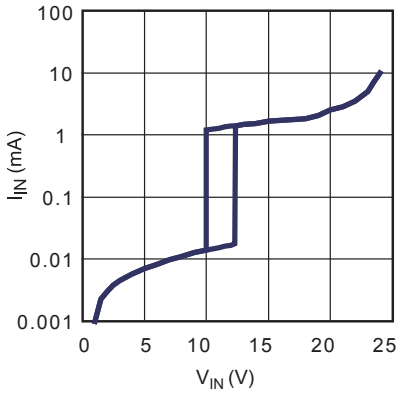
5) The multiplier output is given by: $V_{cs}=K \cdot V_{MUTL} \cdot (V_{COMP}-2.5)$

6) Guaranteed by design.

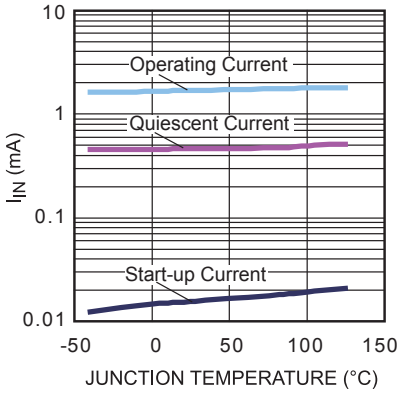
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 15V, T_A = 25°C, unless otherwise noted.

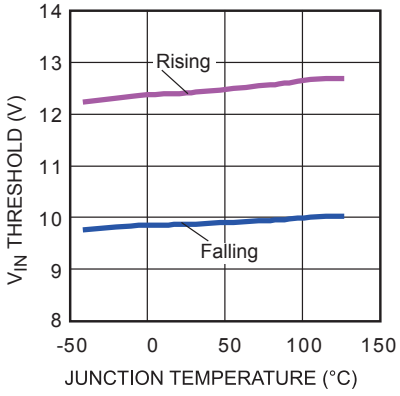
Supply Current vs. Supply Voltage



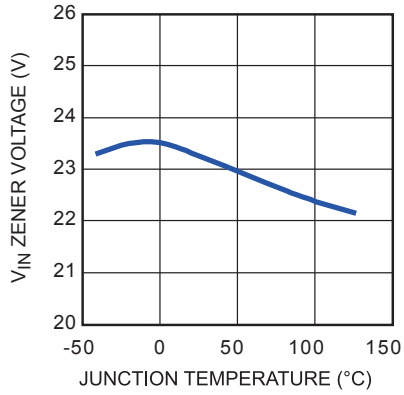
Supply Current vs. T_J



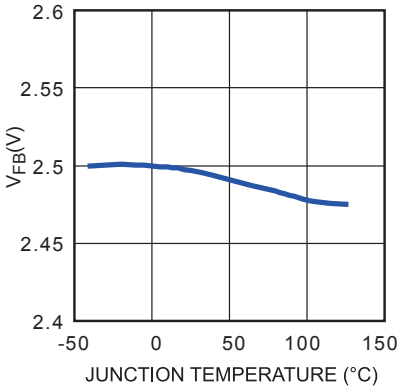
Start-up & UVLO vs. T_J



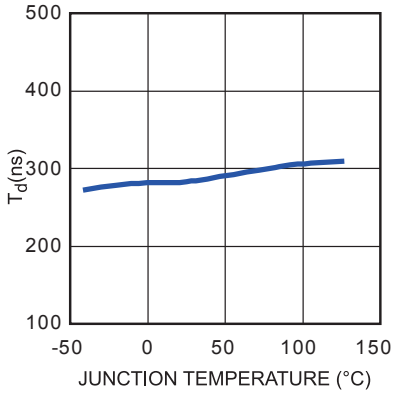
V_{IN} Zener Voltage vs. T_J



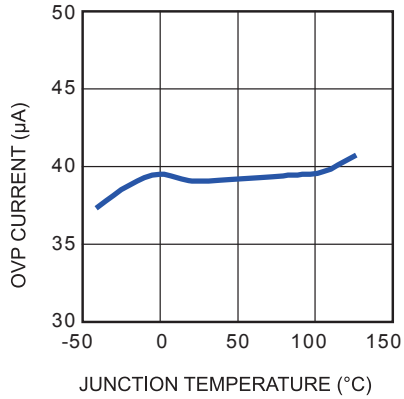
Feedback Reference vs. T_J



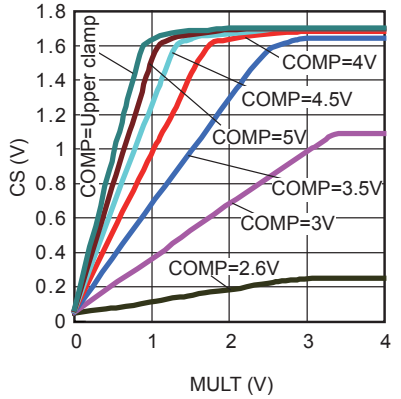
Delay-to-output vs. T_J



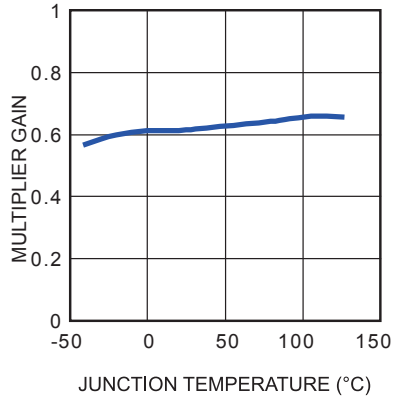
OVP Current vs. T_J



Multiplier Characteristic



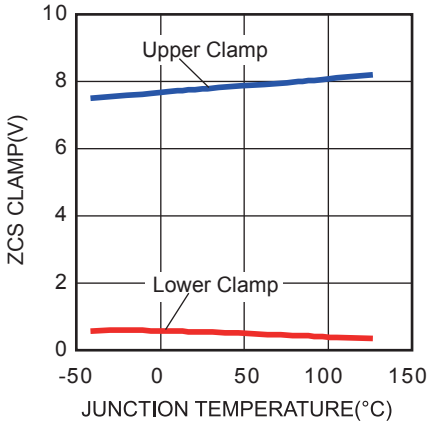
Multiplier Gain vs. T_J



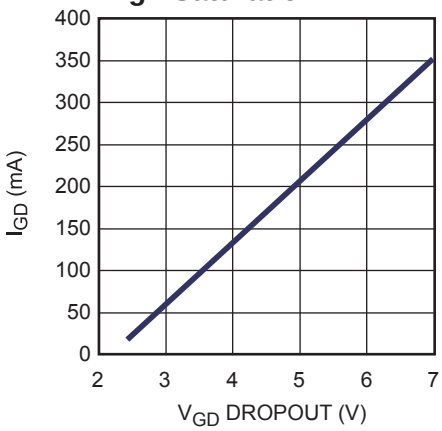
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

V_{IN} = 15V, T_A = 25°C, unless otherwise noted.

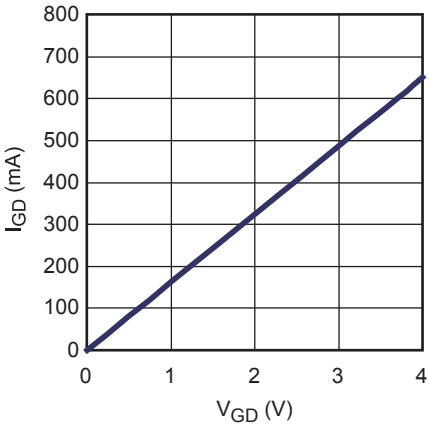
ZCS Clamp Levels vs. T_J



Gate-drive Output High Saturation



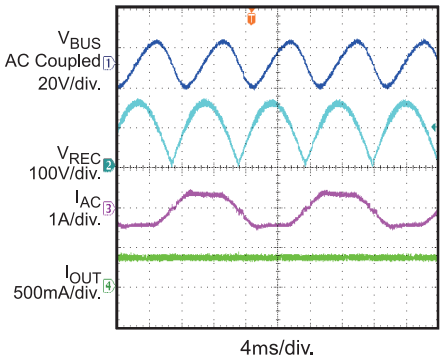
Gate-drive Output Low Saturation



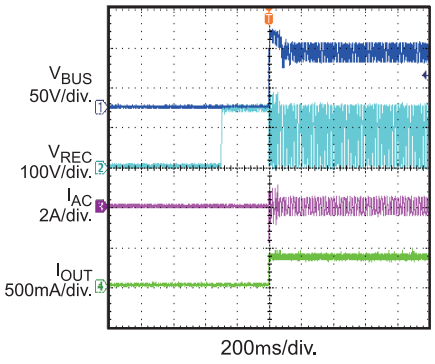
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

Performance waveforms are generated on the evaluation board built with design example. V_{AC}=110V, V_{bus}=70V, I_{OUT}=350mA, P_{OUT}=30W, T_A=25°C, unless otherwise noted.

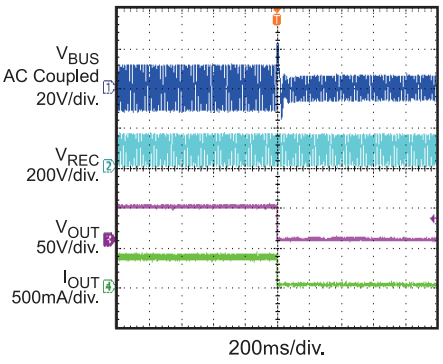
Steady State



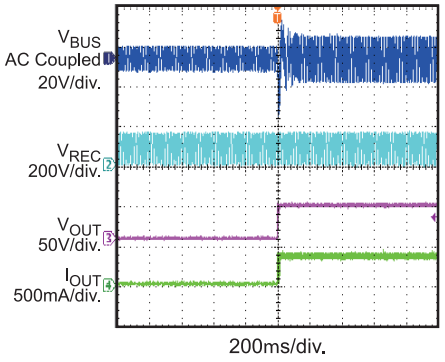
Start Up



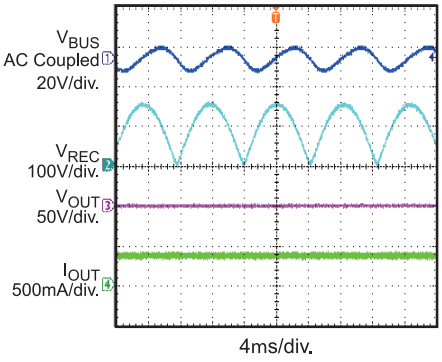
Short Entry LED1 + to LED1 -



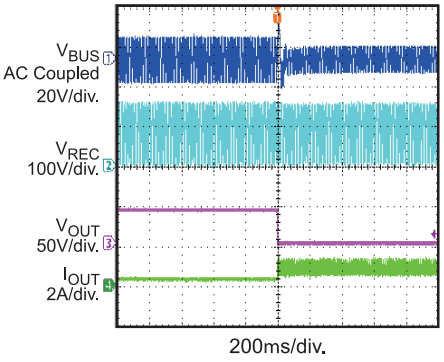
Short Recovery LED1 + to LED1 -



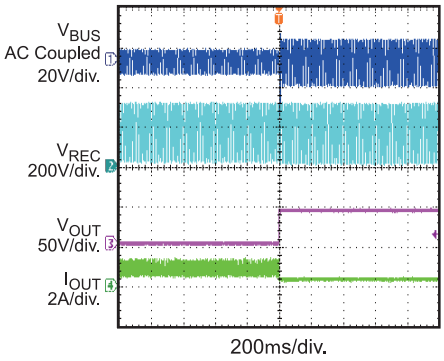
Short Steady State LED1 + to LED1 -



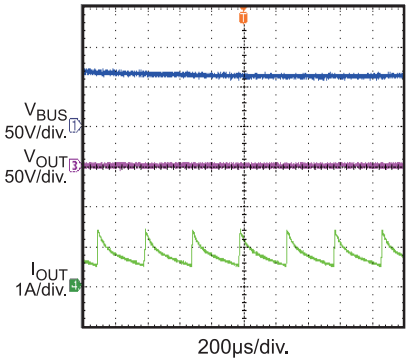
Short Entry LED1 + to GND



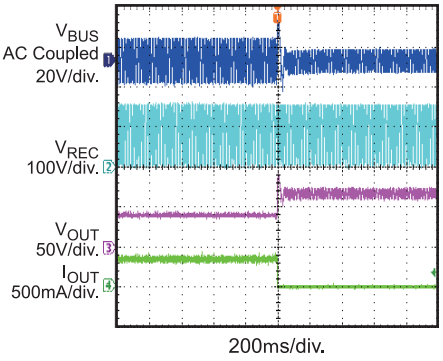
Short Recovery LED1 + to GND



Short Steady State LED1 + to GND



Open One Channel LED



PIN FUNCTIONS

Pin #	Name	Description
1	FB	Feedback. Connect to the output voltage through a resistor divider.
2	COMP	Error Amplifier Output. Connect a compensation network between this pin and the FB pin.
3	MULT	Multiplier Input. Connect to the rectified main voltage through a resistor divider to provide the sinusoidal reference for the current control loop. Also senses input AC voltage and injects constant ratio harmonics
4	CS	Current Sense. Senses the current through the MOSFET using a resistor. Provides internal sinusoidal reference when compared with the output of the internal multiplier to determine MOSFET's turn-off. On-chip R/C filter reduces high-frequency noise on this pin.
5	ZCS	Current-Zero–Crossing Sense. A negative going-edge triggers the MOSFET to turn on.
6	GND	Ground.
7	GATE	Gate Driver Output. The large gate-driver current can drive the gate of the low-cost high-power MOSFET in the system. The pin voltage is clamped to 15V in case this pin is supplied with a high VCC.
8	VIN	Supply Voltage. Powers both the signal block and gate driver. Use a bypass capacitor from this pin to ground to reduce the noise.

BLOCK DIAGRAM

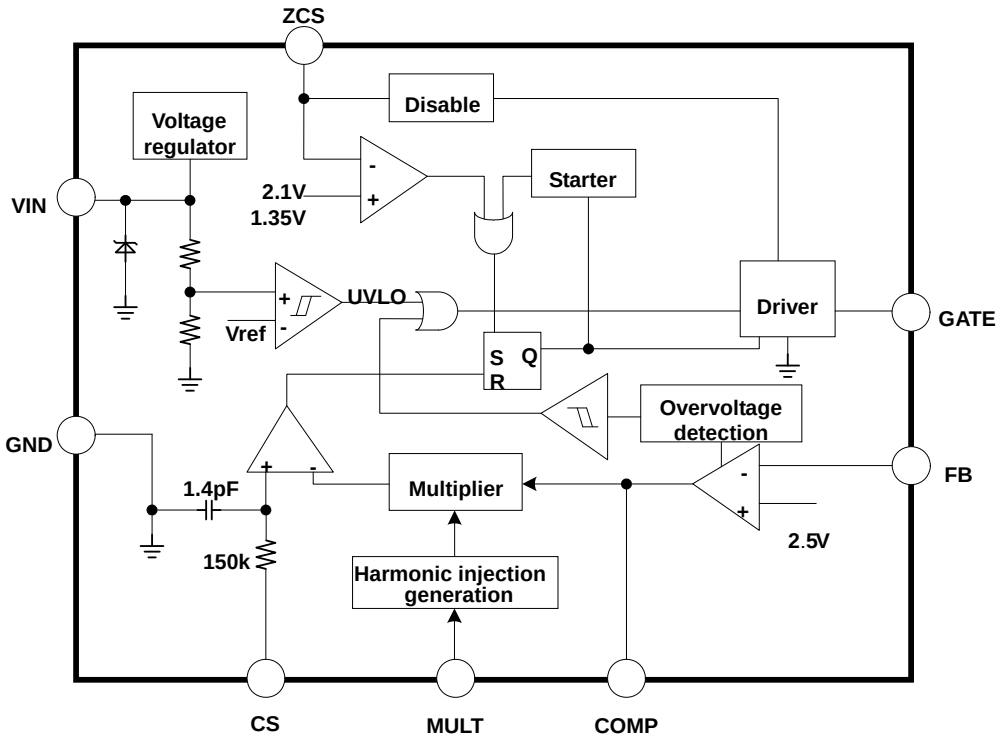


Figure 1: Functional Block Diagram

APPLICATIONS

The MP44011 is a boundary-conduction–mode PFC controller with internal harmonic injection that is optimized for LED lighting drivers.

Output Voltage Regulation

The FB pin senses the output voltage through a resistor divider from the output voltage to ground. An accurate on-chip reference voltage and a high-performance error amplifier accurately regulate the output voltage.

Over-Voltage Protection

MP44011 offers two of over-voltage protection methods: dynamic and static. These two methods ensure that the circuit operates in a reliably safe region.

When the load is very low, the output voltage tends to stay steadily above the nominal value. Under this condition, the error amplifier output saturates low. When the error amplifier output falls below 2.2V, the static OVP triggers and blocks the gate driver to turn off the external power MOSFET and enter an idle state. Normal operation resumes until the error amplifier output goes back into the regulated region.

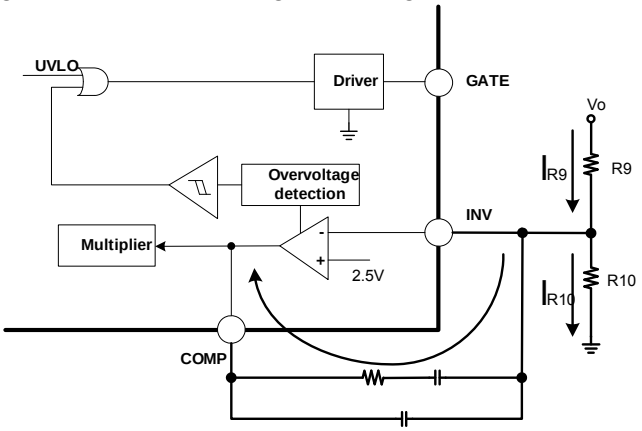


Figure 2: OVP Detector Block

For the boost PFC application, MP44011 implements OVP by monitoring the current through the COMP pin.

In steady-state operation, the current flows through the high-side feedback resistor (R9) and low-side feedback resistor (R10) are:

$$I_{R9} = \frac{V_O - V_{FB}}{R9} = I_{R10} = \frac{V_{FB}}{R10}$$

If there is an abrupt rise on the output (ΔV_O), the voltage on FB pin remains at the reference value as the compensation network between FB pin and COMP pin features a long time-constant for a high power factor (PF). The current through R10 remains equal to V_{FB}/R10, but the current through R9 becomes:

$$I'_{R9} = \frac{V_O + \Delta V_O - V_{FB}}{R9}$$

The current must flow into the COMP pin. At the same time, the chip internally monitors the current. If the current rises to 35μA, the output voltage of the multiplier decreases, thus reducing the the energy delivered to output. If the current rises to about 40μA, the dynamic OVP triggers. Then gate driver is blocked to turn off the external power MOSFET and the MP44011 enters an idle state. The device will remain in this state until the current falls below 10μA. Then the internal starter is re-enabled and allows switching to restart.

Disable Function

Pulling the zero current sensing (ZCS) pin lower than 190mV disables to MP44011 in order to further reduce the quiescent current when the PFC pre-regulator needs to be shutdown. After releasing the ZCS pin, it will stay at lower clamp voltage if there is no external voltage from the auxiliary winding.

Boundary Conduction Mode

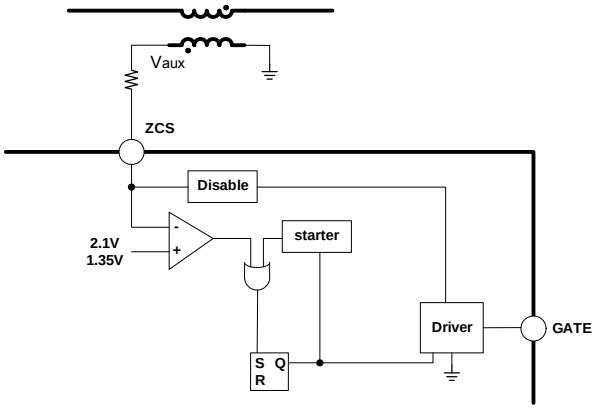


Figure 3: ZCS, Triggering, and Disable Block

When the inductor current reaches zero, the inductor voltage reverses. Then the ZCS generates the turn-on signal for the MOSFET by sensing the falling edge of the voltage on the auxiliary winding coupled with the inductor. If the ZCS voltage goes higher than 2.1V, the comparator waits until the voltage falls below 1.35V. If the voltage falls below 1.35V, the MP44011 turns on the MOSFET. The 7.8V high clamp and 0.55V low clamp protect the ZCS pin. The internal timer generates a MOSFET turn-on signal if the driver signal is low for more than 175μs, and can turn on the MOSFET during start-up since there is no ZCD signal is generated during this period.

Zero-Crossing Compensation

The MP44011 offers a 30mV voltage offset for the multiplier output near the line votlage's zero-crossing that can force the circuit to process more energy at the bottom of the line voltage. This function reduces the total harmonic distortion (THD) of the current.

To prevent excess energy consumption, this offset reduces as the instantaneous line voltage increases so that the offset is negligible near the top of the line voltage.

Harmonic Injection Function

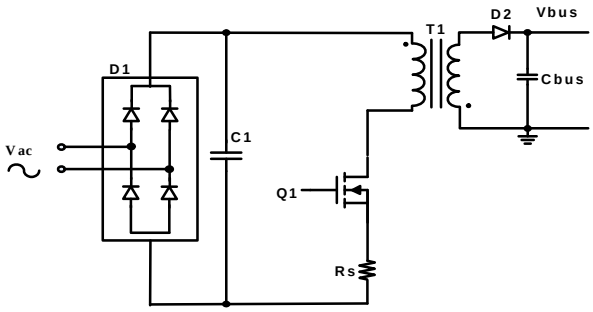


Figure 4: Flyback PFC Main Circuit

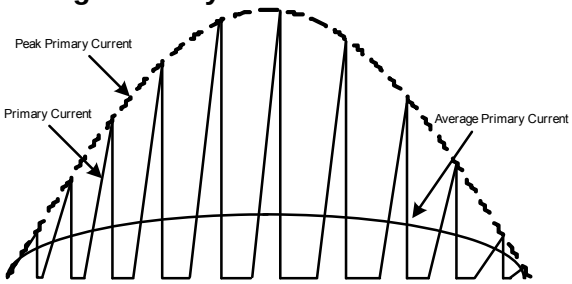


Figure 5: Primary Current Waveform of Traditional BCM Flyback PFC

The flyback PFC application exemplifies the harmonic injection function for this document. For a traditional BCM flyback PFC, the transformer acts like two coupled inductors where the current will not flow through both windings at the same time; the current is discontinuous. The primary current rises from the zero crossing and the secondary current returns to zero for every switching cycle. The average input current is related to both the peak primary current and the duty cycle.

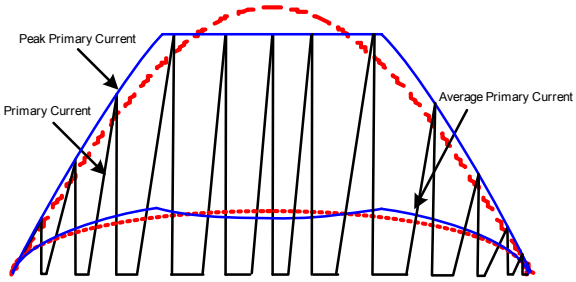


Figure 6: Primary Current Waveform of Flyback PFC with the MP44011

For the MP44011, the MULT pin senses the AC input line and injects constant ratio harmonics into sensed line voltage, so the peak primary current reference has a choppy sinusoidal signal. As a result, the peak primary current flowing through the transformer is sharply reduced, and the circuit can use a smaller transformer core that will not saturate.

In addition, harmonic injection into the input current reduces the input power fluctuation: This results in a smaller output voltage ripple on the output capacitor, and allows for the use of smaller capacitors. Therefore, the MP44011's internal harmonic injection function can reduce both bus capacitor values and transformer size.

However, there is a trade-off between smaller core and performance: a smaller core can have more winding layers and therefore greater leakage inductance. This leakage reduces efficiency and increase device voltage stress..

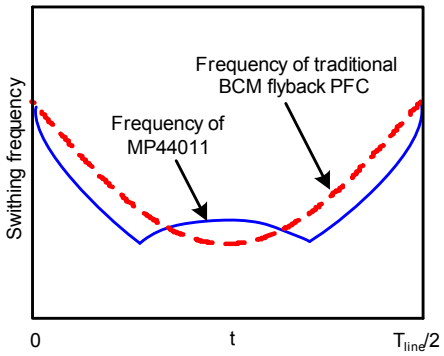


Figure 7: Switching Frequency

Even with the same transformer core as used for a traditional BCM PFC, the efficiency improves with harmonic injection.

With harmonic injection, the minimum frequency occurs not at the top of the line but at the line's choppy regions. Compared with traditional BCM PFC, the frequency at the top of the line increases.

Power Factor Correction

The MP44011 senses the inductor current through the current sense pin and compares it to the choppy sinusoid signal which is generated from the multiplier output. When the external power MOSFET turns on, the primary inductor current rises linearly. When it reaches the choppy sinusoid signal, the external power MOSFET turns off and the secondary diode turns on. Then the secondary inductor current begins to fall. When the secondary inductor current reaches zero, the power MOSFET turns on again, which causes the primary inductor current to start rise . The power circuit works in boundary conduction mode and inductor current's signal envelope has a choppy sinusoidal shape. The average current also has a choppy sinusoidal shape. This control method can achieve a high power factor.

Layout Guide

For boundary-mode PFC operation, the output feeds back to the FB pin for comparison with the reference voltage. Therefore, a constant reference voltage is very important for an accurate output. Use short traces to connect the FB pin to the feedback resistors.

A rectified AC voltage and COMP voltage generates the multiplier output, which generates the inductor current envelope. Place a small ceramic capacitor from the MULT pin to S-GND and place compensation components close to the COMP pin and S-GND to improve noise immunity.

For zero-current sensing, place R5 close to the ZCS pin to prevent noise caused by long wire.

For inductor current sensing, keep the trace from the current-sensing resistor to the CS pin pin as short as possible—even though there is an on-chip filter on the CS pin—to prevent falsely turning off MOSFET. If the design bars the use of a short trace, add an external filter from the sense resistor to the CS pin. To prevent noise from P-GND, limit the connection between P-GND and S-GND to one point.

To keep the chip operational with a stable VIN voltage, keep the VIN capacitor as close to the VIN pin to limit voltage fluctuations.

DESIGN EXAMPLE FOR FLYBACK PFC WITH MP44011

1. Design Specifications:

Input voltage range: V_{AC}=85V-265V

Typical mains frequency: f_L=50Hz

DC output voltage: V_{OUT}=70V

Maximum output power: P_{OUT}=30W

Maximum $2f_L$ output ripple:

ΔV_O=28V peak-to-peak

Minimum switching frequency: f_{min}=40kHz

Harmonic injection ratio: K_2=0.75

Reflected voltage: V_R=210V

Leakage inductance overvoltage: ΔV=100V

Expected efficiency: η=85%

2. Preliminary Calculations:

Minimum Input Peak Voltage:

$$V_{PKmin}=V_{ACmin}\times\sqrt{2}=120V$$

Maximum Input Peak Voltage:

$$V_{PKmax}=V_{ACmax}\times\sqrt{2}=375V$$

Maximum Input Power: $P_{IN}=P_{OUT}/\eta=35.3W$

Peak-to-Reflected Voltage Ratio:

$$K_v=V_{PKmin}/V_R=0.57$$

Characteristic functions value:

$$F2(K_V)=\frac{0.5+1.4\cdot10^{-3}\cdot K_V}{1+0.815\cdot K_V}$$

$$F3(K_V)=\frac{0.424+5.7\cdot10^{-4}K_V}{1+0.862\cdot K_V}$$

$$F4(K_V)=\frac{0.25-1.5\cdot10^{-3}\cdot K_V}{1+1.074\cdot K_V}$$

2.1 Peak Primary Current

$$I_{PKp}=\frac{2K_1\cdot P_{in}}{V_{PKmin}\cdot F2(K_V)}=1.51A$$

For MP44011, the coefficient K_1 is the peak primary-current ratio compared with the traditional CRM PFC. Here, K_1=0.87.

2.2 RMS Primary Current:

$$I_{RMSp}=I_{PKp}\cdot\sqrt{\frac{F2(K_V\cdot K_2)}{3}}=0.53A$$

2.3 Peak Secondary Current:

$$I_{PKs}=\frac{2\cdot P_{OUT}}{V_{OUT}\cdot K_V\cdot F2(K_V)}=4.29A$$

2.4 RMS Secondary Current:

$$I_{RMSs}=I_{PKs}\cdot\sqrt{\frac{F3(K_V)}{3}}=1.03A$$

Power Stage Design

3. Diode Bridge

The maximum input RMS current is:

$$I_{AC\_max}=\frac{P_{in}}{V_{AC\_min}}=0.42(A)$$

To provide a sufficient margin, select GBU406 (600V/4A).

4. Input Capacitor

By setting the coefficient r to 0.1, obtain the input capacitance by using the equation below:

$$C_{in}=\frac{I_{AC\_max}}{2\pi\cdot f_{min}\cdot r\cdot V_{AC\_min}}=0.19\times10^{-6}(F)$$

Use a 0.22μF tantalum capacitor with a 630V voltage rating as the input capacitor to provide high-frequency energy during switching cycle.

5. Transformer

Calculate the primary Inductance using the following:

$$L_p=\frac{V_{PKmin}\cdot K_2}{(1+K_2\cdot K_V)\cdot f_{min}\cdot I_{PKp}}=1.0mH$$

The turn ratio is:

$$n=\frac{V_R}{V_{OUT}}=3$$

Then A_p is:

$$A_p=A_e \cdot A_w=\frac{L_P \cdot I_{PKp} \cdot I_{RMSp}}{B_{max} \cdot K_c \cdot j}=1.27\times10^{-9}mm^4$$

Where:

A_e is the effective area of the core section;

A_w is the effective area of the core window;

B_{max} is the max swing of the magnetic flux density (generally B_{max}=0.3~0.4T);

K_c is the window coefficient, which is about 0.3 in design;

j is the current density of the wire, which is typically 4-6A/mm^2.

The EE25 core is selected according to A_p.

The primary inductor turn number is:

$$N_p=\frac{L_p \cdot I_{PKp}}{B_{max} \cdot A_e}=110$$

The needed air gap is:

$$\sigma=\frac{N_p^2 \cdot A_e \cdot \mu}{L_P}=6.08\cdot10^{-4}m$$

And the secondary winding turn number is:

$$N_s=\frac{N_p}{n}=36$$

6. MOSFET

The maximum drain voltage is:

$$V_{DSmax}=V_{PKmax}+V_R+\Delta V=685V$$

The maximum RMS MOSFET current is:

$$I_{Qrms\_max}=I_{RMSp}=0.53\,A$$

And the pulse-drain current is:

$$I_{Q\_pulse}>I_{PKp}=1.51A$$

The FQPF8N80C (800V/8A) meets the power requirement of the design.

7. Secondary Diode

The maximum RMS current of the output diode is:

$$I_{Drms\_max}=I_{RMSs}=1.03A$$

And the maximum reverse voltage is:

$$V_{Dmax}=\frac{V_{PKmax}}{n}+V_{OUT}=194V$$

UF3004 (400V/3A) meets the design criteria.

8. Output Capacitor

The output capacitor is selected only based on output voltage ripple

$$C_{OUT}=\frac{1}{2\cdot\pi\cdot f_L}\cdot\frac{F4(K_V)}{F2(K_V)}\cdot\frac{I_{OUT}}{\Delta V_O}\cdot K_3=38\mu F$$

Where K_3=0.85.

The cap (47μF/100V) is selected as the bus capacitor.

9. Sense Resistor

Assuming a peak value of 2.5V (@V_{AC_max}=265V) on the multiplier input, the peak value at the minimum line voltage is $V_{MULTpkmin}$=2.5 × 85/265=0.8V which is multiplied by the maximum slope of the multiplier, 1.62, giving a 1.32V peak on the current sense. So the sense resistor will not exceed:

$$R_{sen}\le\frac{1.32}{I_{PKp}}=0.87\Omega$$

Considering the power consumption, select a 0.4Ω sense resistor.

The first stage of flyback PFC design is complete. Our evaluation board adds two channels of DC/DC using the MP4689 to constitute a system for the LED driver. For MP4689 applications, please find MP4689 datasheet for details.

Figure 8 shows the application schematic with power stage design. The typical performance and circuit waveforms are shown in the typical performance characteristics section. For more possible applications of this device, please refer to related Evaluation Board Datasheets.

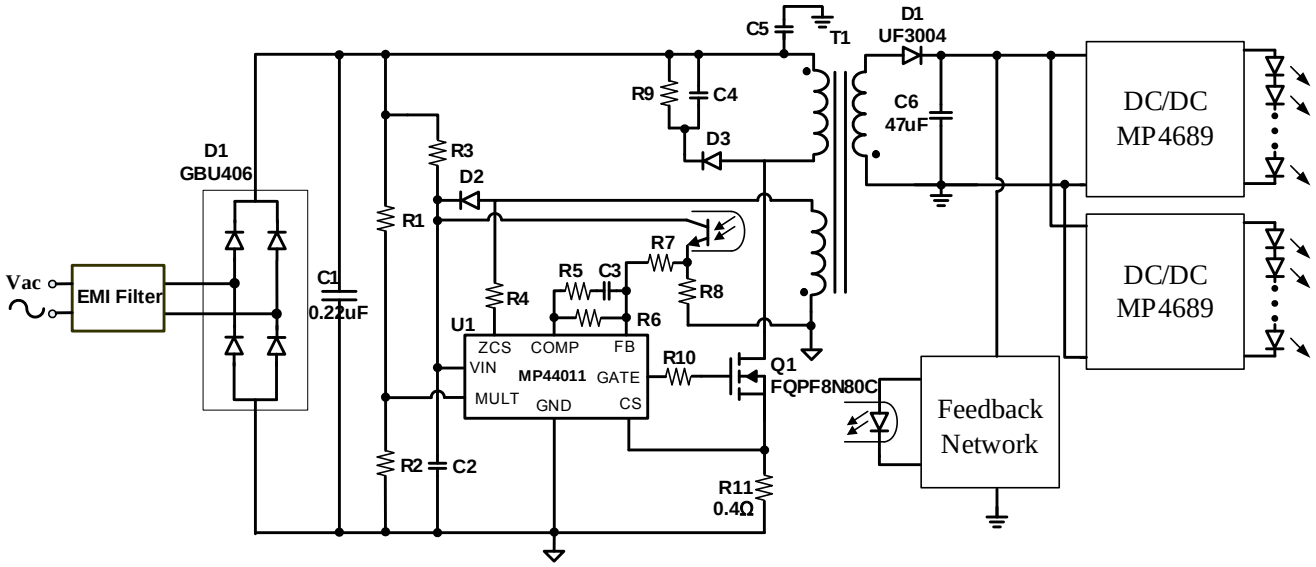
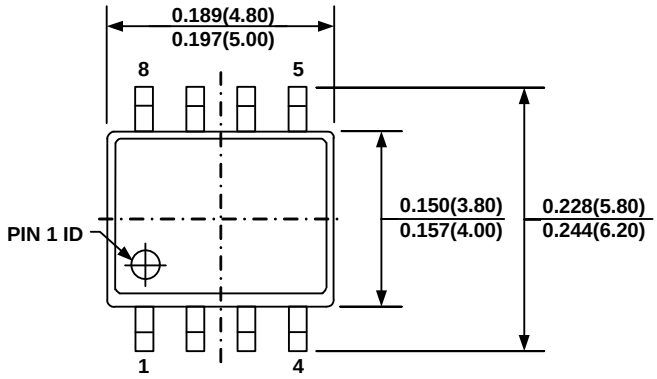


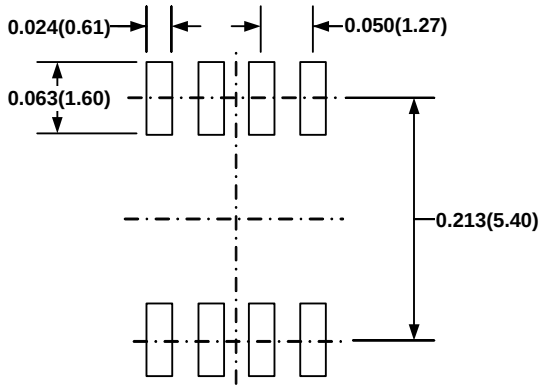
Figure 8: Design Example of 30W LED Lighting with MP44011

PACKAGE INFORMATION

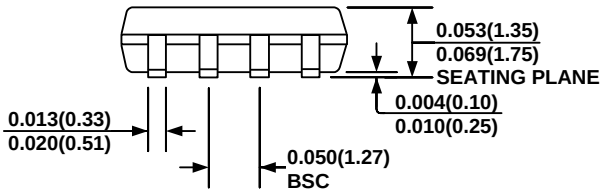
SOIC8



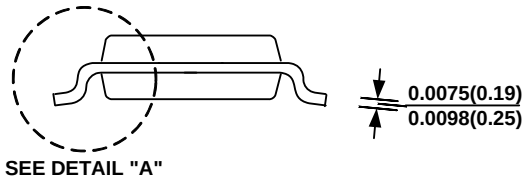
TOP VIEW



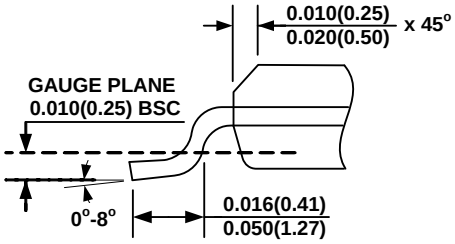
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.